Application Note, DS1, Jan. 2003

# VINETIC

## Voice and Internet Enhanced Telephony Interface Circuit

## Transversal Offset Current Compensation

Wired Communications

Infineon technologies

Never stop thinking.

**Application Note**

| **Revision History:** | **2003-01-14** | DS1 |
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# 1 Scope

This application note describes the offset compensation procedure for the VINETIC. It is applicable for the following members of the VINETIC product family:

- PEB 3304 V1.3
- PEB 3314 V1.3
- PEB 3324 V1.3
- PEB 3322 V1.3
- PEB 3308 V1.3
- PEB 3318 V1.3

The VINETIC offers an offset compensation for the transversal current. If the described offset compensation procedure is used, accuracies can be improved for:

- Programmable DC line feeding (battery function)
- Programmable ring trip and off-hook detection (supervision)
- Line testing functions (testing)

# 2 Introduction

The SLIC senses the transversal current flowing on the analog tip/ring interface. The SLIC current sense signal comprises both AC and DC current information. The VINETIC processes the AC and DC current information in separate functional units. The transversal DC current information shows an inherent offset value due to the SLIC sensor, filters and AD converter. This document describes a method of improving the accuracy of the DC transversal current sensing. The described method only influences the processing of the DC transversal current information and is not relevant for the processing of the AC transversal current (voice signal). It is recommended to apply the described method for offset current compensation in order to improve the accuracies of DC feeding, off-hook detection and line testing functions.

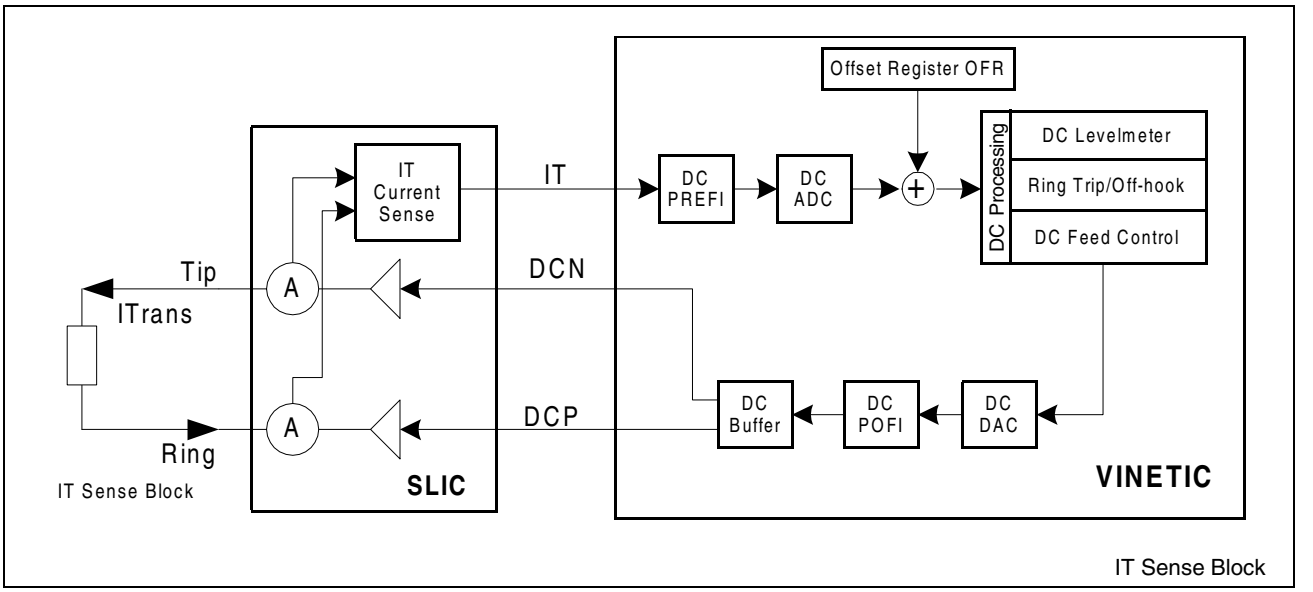



**Figure 1 Block Diagram of Transversal Current Sensing**

The transversal line current $I_{Trans}$ is sensed in the SLIC, then gets fed back via IT pin to the VINETIC and is A/D converted within the VINETIC. The digital value is further processed within the DC Feed Control unit, the off-hook/ring trip detection unit and the levelmeter unit. Both the SLIC current sensing as well as the A/D conversion with the required low path filtering causes an offset. That means the representation of the IT current which is processed within the VINETIC deviates from the actual transversal current ($I_{Trans}$) flowing in tip/ring.

As can be seen from **Figure 1** the VINETIC offers an offset register OFR, which can be used to eliminate the described offset value. The content of the offset register gets added to the value from the A/D converter. By writing an appropriate value into register OFR, the offset caused by the SLIC, the filter and the A/D converter can be compensated.

# 3 Procedure for IT Offset Current Compensation

The VINETIC offers an operating mode “Active with HIRT”[1)] which allows to switch off the SLIC buffers which normally drive the line. In this mode the SLIC output buffers are feeding no voltage to the line and therefore no transversal current is flowing. The integrated level metering allows to measure the IT current. When measuring the IT current when the VINETIC is in “Active with HIRT” operating mode, the measured current represents the offset current.

There are two methods to get the appropriate value for the offset register OFR. A simple one and a more accurate/more robust one which uses the integration function of the integrated levelmeter.

1) HIRT = High Impedance on Tip and Ring

## 3.1 Simple Method for Offset Current Compensation

This method puts the line into “Active with HIRT” operating mode, reverses the polarity, reads out the levelmeter result register and writes this value to the Offset Register OFR.

Programming Sequence:

1. Reset value of offset register: OFR[15:0] = $0000_H$
2. Set levelmeter select to IT: LMCR:LMSEL[3:0] = $0101_B$
3. Set DC levelmeter gain to 1: LMCR:DC-AD16 = 0
4. Switch off DC levelmeter rectifier: LMCR:LM-RECT = 0
5. Set Reverse Polarity mode: BCR2:REV-POL = 1
6. Set Operating Mode “Active with HIRT”: short command e.g. $5230_H$ for channel 0
7. Allow line to settle: wait about 100 ms (depends also on the line termination on tip/ring)
8. Read out levelmeter result register LMRES
9. Write value read from LMRES into register OFR
10. Restore original settings: REV-POL, DC-AD16, LM-RECT, operating mode

## 3.2 Method for Offset Current Compensation with DC Levelmeter Integrator

This method uses the DC Levelmeter integrator to get the value for offset register OFR. The DC levelmeter integrator sums up the levelmeter input value for a defined period of time. Disturbances and noise are therefore filtered and reduced. As the offset value typically is a small value which is sensitive towards noise and disturbances, this method is more robust and is recommended to be used. For a more detailed description of how to use the DC levelmeter function of the VINETIC, please refer also to the description in “System Reference” manual of the VINETIC (chapter “Advanced Integrated Test and Diagnostic Functions”).

Programming sequence:

1. Reset value of offset register: OFR[15:0] = $0000_H$
2. Set levelmeter select to IT: LMCR:LMSEL[3:0] = $0101_B$
3. Set the levelmeter integration period. An integer multiple of the mains supply period would give a good suppression of mains influence (e.g. 20 ms for 50 Hz).
   The levelmeter integration period is set in CRAM (Coefficient RAM) address $48_H$.There are two DC levelmeter samples per ms, therefore:
   50 Hz would result in 40 DC levelmeter samples ($0666_H$ at CRAM address $48_H$)
   60 Hz would result in 33 DC levelmeter samples ($07AE_H$ at CRAM address $48_H$)

4. Set DC levelmeter gain LMDC. A proper value for offset compensation would be 1. DC levelmeter gain factor LMDC is set at CRAM address $68_H$. A value of 1 would mean a coefficient of $4000_H$ at CRAM address $68_H$.

*Note:*

1. *If the levelmeter integration result is either $7FFF_H$ or $8000_H$ (overflow condition), the measurement should be repeated with a decreased value of LMDC gain. For setting of LMDC gain see also "System Reference" manual chapter "DC Level Metering".*
2. *The CRAM coefficients are really active only if BCR2:CRAM-EN is set to 1. This method cannot be used if ROM coefficients are used.*

5. Reset DC levelmeter rectifier: LMCR:LM-RECT = 0
6. Select single levelmeter integration: LMCR:LM-ONCE = 1
7. Set DC path gain DCgain to 1: LMCR:DC-AD16 = 0
8. Set Normal Polarity mode: BCR2:REV-POL = 0
9. Set Operating Mode "Active with HIRT": short command e.g. $5230_H$ for channel 0
10. Allow line to settle: wait about 100 ms (depends also on the line termination on tip/ring)
11. Start levelmeter integration: set LMCR:LM-EN = 0, wait at least 500 µs and set LMCR:LM-EN = 1. The DC levelmeter integration is started when bit LMCR: LM-EN is changed from 0 -> 1.
12. Wait for end of DC levelmeter integration, which is indicated by SRS1:LM-OK = 1. It is possible to enable an interrupt for the transition of SRS1:LM-OK 0-> 1 (interrupt mask register MR-SRS1:M-LM-OK).
    If polling is used to detect SRS1:LM-OK 0->1, it necessary to start polling of SRS1:LM-OK after a delay time of at least 1 ms after setting LMCR:LM-EN 0->1. Otherwise LM-OK might be still set to 1 from a previous levelmeter integration.
13. Read out levelmeter result register LMRES
14. Calculate offset value with formula:

$$\mathrm{OffsetValue} = \frac{\mathrm{LMRES}}{\mathrm{Nsamples} \times \mathrm{LMDC} \times \mathrm{DCgain}}$$

    LMRES: result in levelmeter result register
    Nsamples: number of DC levelmeter samples
    LMDC: gain of DC levelmeter integrator
    DCgain: programmable gain in DC path

*Note: When doing the calculation, please note that the result in register LMRES represents a 16 bit 2´s complement. A value of e.g. $ABCD_H$ would equal -21555.*

15. Write 2´s complement of calculated value into register OFR.
16. Restore original settings: CRAM settings (ring frequency/integration period, LMDC), DC-AD16, REV-POL, LM-RECT, LM-ONCE, operating mode

**Example:**

Levelmeter samples (Nsamples): 40

LM-ADC-16 = 0: DCgain = 1

LMDC = 1 (CRAM address $68_H = 4000_H$)

LMRES = $A279_H$= -23943

$$\text{OffsetValue} = \frac{\text{LMRES}}{\text{Nsamples} \times \text{LMDC} \times \text{DCgain}} = \frac{-23943}{40 \times 1 \times 1} = -599 = \text{FDA9}_H$$

The value of $FDA9_H$ interpreted as a 2´s complement equals $-0256_H$. In order to compensate the transversal current offset, a value of $0256_H$ has to be written to register OFR.

*Note: Instead of using an integration period either suitable for 50 or 60 Hz main frequency suppression, an integration period of 100 ms might be chosen. This would fit for both 50 and 60 Hz suppression (either 5 or 6 periods). An integration time of 100 ms is set with a value of $0148_H$ at CRAM address $48_H$. Nsamples would be 200. In order not to cause an overflow in the result register LMRES, LMDC should be set to 1/8 (0800H at CRAM address $68_H$).*

# 4 Examples for Offset Current Compensation

The following three examples show typical measurements in order to demonstrate the influence of transversal offset current compensation.

## 4.1 Off-hook Threshold in Power Down Resistive Mode

Power Down Resistive operating mode is used while the phone is on-hook. Line feed voltage is supplied by the SLIC via two 5 kΩ resistors. The transversal line current is monitored to detect off-hook condition. As the off-hook current is very small because of the 2*5 kΩ feeding, the effect of the offset current might be quite considerable.

Assumption: programmed off-hook threshold for Power Down Resistive Mode: 4 mA.

Without offset current compensation the actual off-hook threshold was measured with 4.25 mA. After offset current compensation, off-hook was detected with 4.06 mA.

## 4.2 Ring Trip Threshold in Ringing/Ring Pause Mode

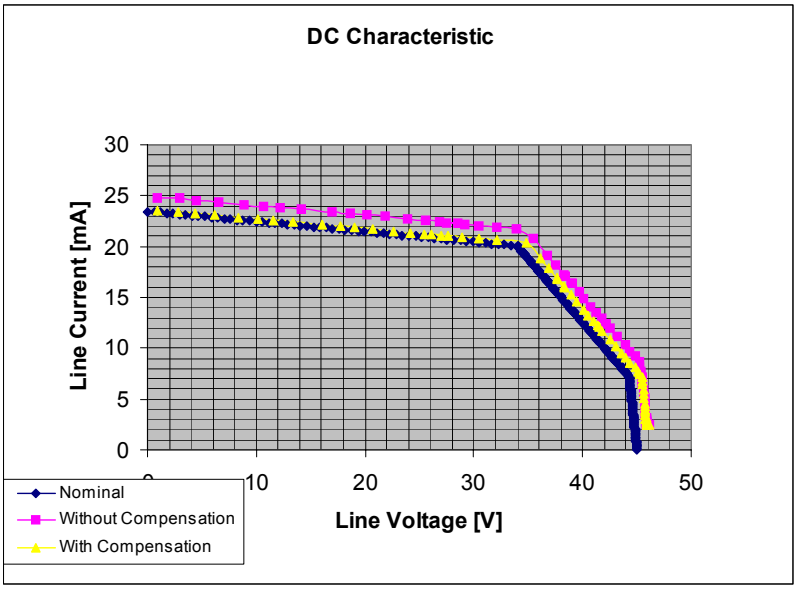
Programmed ring trip threshold: 12 mA.

Measured ring trip threshold without offset current compensation: 14.3 mA.

Improved ring trip threshold after offset current compensation: 12.4 mA.

## 4.3 DC Feed Characteristic

The **Figure 2** shows the difference between a typical DC feed characteristic with and without offset current compensation.




| | Nominal | Without Compensation | With Compensation | |
|---|---|---|---|---|
| **Ri** | 9999 | 10481 | 10250 | Ohm |
| **I0** | 23,5 | 25,0 | 23,7 | mA |
| **Ik1** | 20,1 | 21,7 | 20,3 | mA |
| **Vk1** | 34,0 | 34,7 | 34,8 | V |
| **Rk12** | 800 | 792 | 805 | Ohm |
| **RV** | 100 | 105 | 102 | Ohm |
| **Vlim** | 45,0 | 46,2 | 46,2 | V |

Note: A description of the DC feeding characteristic parameters can be found in „System Reference“ manual of VINETIC

DC_char

**Figure 2 DC Feeding Characteristic with and without Transversal Offset Current Compensation**