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VINETIC®

Voice and Internet Enhanced Telephony Interface Circuit

VINETIC®-2CPE (PEB 3332), Version 2.1
VINETIC®-1CPE (PEB 3331), Version 2.1
SLIC-DC (PEF 4268), Version 1.2
SLIC-E (PEF 4265 T), Version 2.1
TSLIC-E (PEF 4365 T), Version 2.1

Preliminary

Hardware Design Guide

Rev. 2.0

Communication Solutions

infineon

Never stop thinking

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VINETIC® Voice and Internet Enhanced Telephony Interface Circuit
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Previous Version:

Page	Subjects (major changes since last revision)
Page 24	SLIC-E added in Chapter 3
Page 28	Value of Line Testing resistors are changed
Page 33	Chapter 4.3 and Chapter 4.4 are modified to include information for SLIC-E
Page 40	Chapter 5.4 is added for SLIC-E
Page 43	In Figure 28 VCMAB, ITACA, ITACB were not correct connected
Page 48	Table 6 value for Line Testing resistors are changed
Page 20	Internal PCM connection is added

Table of Contents

List of Figures

List of Tables

Preface

The VINETIC®-2CPE/-1CPE Hardware Design Guide serves as a reference document for the design of applications using the VINETIC®-2CPE Version 2.1 or VINETIC®-1CPE Version 2.1 together with the SLIC-DC Version 2.1 and SLIC-E Version 2.1. The VINETIC® Chip Set Family allows easy integration of analog line POTS (Plain Old Telephony System) functions with additional enhanced DSP features.

This document is intended to help the reader become familiar with the VINETIC®-2CPE/-1CPE Version 2.1 devices and to accelerate the development process. This VINETIC®-2CPE/-1CPE Hardware Design Guide provides design and layout guidelines for achieving optimum performance for a POTS application. Following these guidelines helps to ensure a reliable design.

To simplify matters, the following synonyms are used:

VINETIC®:

Synonym used for the CODEC versions VINETIC®-2CPE/-1CPE Version 2.1.

SLIC:

Synonym used for the SLIC-DC Version 1.2 and the SLIC-E Version 2.1.

Attention: TSLIC-E (PEF 4365) is a dual channel version of the SLIC-E (PEF 4265) with identical technical specifications for each channel. Therefore, whenever SLIC-E is mentioned in the specification, TSLIC-E can also be deployed.

In order to simplify the usage of channel specific pin names within this document, in many cases only the short form for the pin names is used without endings indicating the specific channel A or B (_A, _B).

Organization of this Document

Chapter 1: General Design Overview

General overview for system design with the VINETIC®-CPE Chip Set.

Chapter 2: Design Guidelines for VINETIC®-2CPE/-1CPE

Schematic design practices are identified to prevent most common signal and noise issues. This includes signal termination, analog circuitry, and pull-up /-down resistors.

Chapter 3: Design Guidelines for SLICs

Schematic design practices are identified to prevent most common signal and noise issues. This includes analog circuitry, packages and component values.

Chapter 4: Power Supply and Grounding

This chapter deals with the concept of power and ground planes. It provides hints for decoupling and filtering. Information about power-on sequencing and avoiding unwanted loop antenna effects when using a chassis ground plane is also included.

Chapter 5: Layout Guide

Details on placement and routing rules as well as rules for power and ground planes are described. The instructions of this document should be carried out to ensure a proper design with good performance.

Chapter 6: Transition Guide VINETIC®-2CPE Version 1.4 to Version 2.1

Differences in hardware between VINETIC®-2CPE Version 1.4 and VINETIC®-2CPE Version 2.1 are explained.

Chapter 7: Summary and Design Checklist

A short checklist describes the most important hardware and layout related details.

1 General Design Overview

Designing a POTS interface either on a Customer Premises Equipment (CPE) or for other voice communication systems, the Infineon chip set utilizes a single or dual-channel codec/DSP circuit (VINETIC®-2CPE/-1CPE) together with a high-voltage line interface circuit (SLIC-DC).

The VINETIC®-2CPE includes 2 analog line channels which connect to the SLICs, one PCM interface and the Parallel/Serial Control Host Interface to connect to the host controller.

Figure 1 is a simplified block diagram showing the interface topology of a typical POTS CPE application using Infineons VINETIC®-CPE devices. The VINETIC®-1CPE includes only one analog line channel connected to the SLIC.

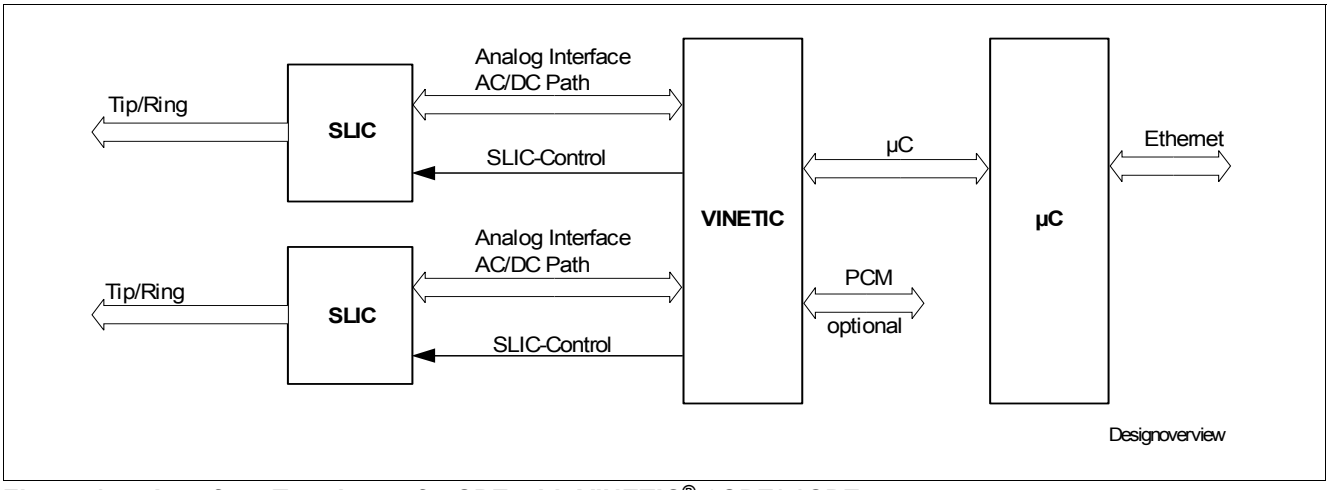


Figure 1 Interface Topology of a CPE with VINETIC®-2CPE/-1CPE

One or two analog channel groups can be supported via the Parallel/Serial Control Host Interface to provide packetized voice data (RTP format). This allows easy support of packetized voice applications like VoIP.

The interface between the VINETIC®-2CPE/-1CPE and the SLIC is an interface with separate receive and transmit links (AC/DC) for each channel. Additional lines of the interface control the line status, for example ringing.

2 Design Guidelines for VINETIC®-2CPE/-1CPE

This chapter describes the design guidelines for the VINETIC®-2CPE/-1CPE. The design guidelines for the SLIC are described in **Chapter 3**. The VINETIC®-2CPE/-1CPE offers the selection of different host interfaces, one PCM interface, up to two analog interfaces, one JTAG interface and eight GPIOs (only with the PG-TQFP-100 package). These interfaces are described in detail in the following chapters.

The parallel/serial host interface is only +3.3 V tolerant. When a controller delivers +5.0 V signals level shifter must be placed in between both devices.

2.1 Interface Configurations

Two different packages are available for the VINETIC®-2CPE/-1CPE devices, the PG-TQFP-64 and the PG-TQFP-100 package. The smaller package PG-TQFP-64 only supports the serial host interface (SPI- interface). All other host interface modes are only possible with the PG-TQFP-100 package.

2.1.1 Serial Micro Controller Interface Type: SCI + PCM

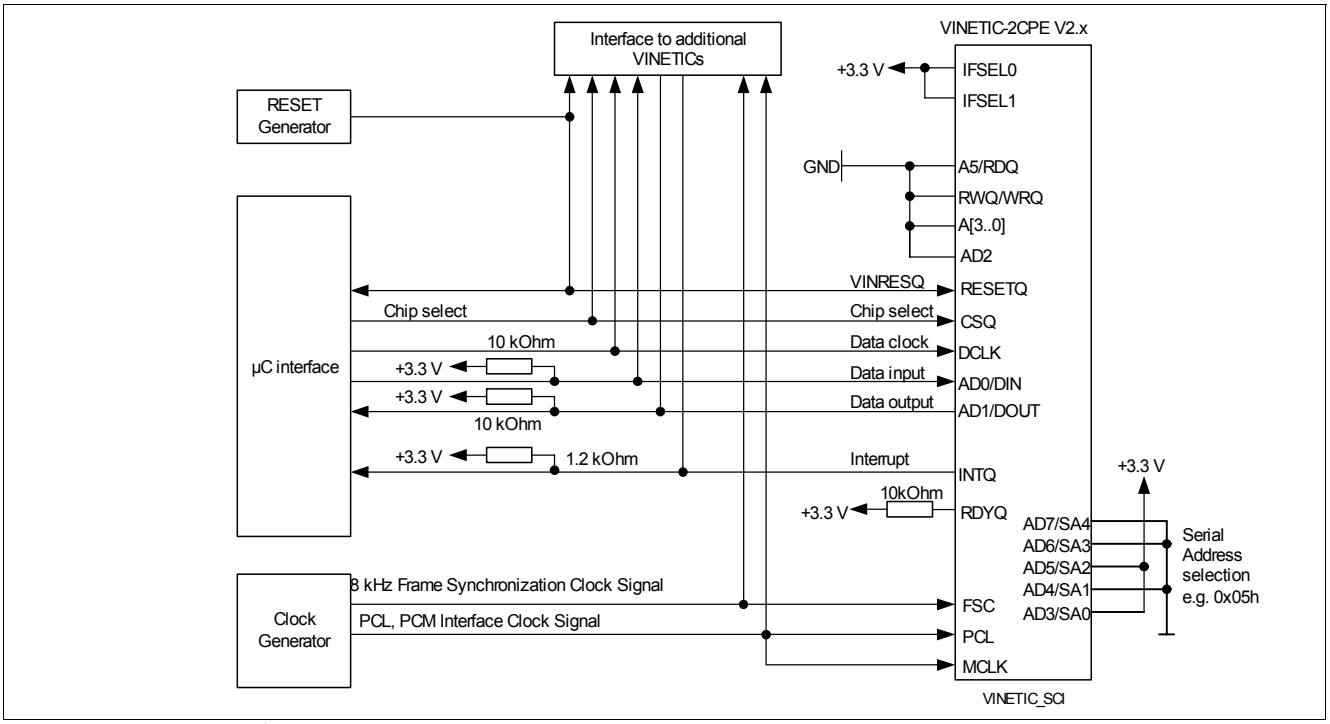


Figure 2 VINETIC®-2CPE/-1CPE in SCI/SPI Mode

The serial synchronous interface SCI/SPI is selected by connecting the IFSEL pins (IFSEL[1:0]) to the following logic levels:

IFSEL1[1)] = 1

IFSEL0 = 1

It is required that each VINETIC®-2CPE/-1CPE in the PG-TQFP-64 needs a dedicated CSQ line, as the internal address line is $1F_H$ due to internal pull-ups (SA0..SA4 are not available for PG-TQFP-64 package). The address must be transfered in every command. The internal pull-ups are only active in the PG-TQFP-64 package. Address selection in the PG-TQFP-100 package is accessable. In the PG-TQFP-100 package these pull ups are disabled!

1)IFSEL[1:0] is not supported with the package PG-TQFP-64 of the VINETIC®-2CPE/-1CPE.

For example when the address 05_H should be selected, the address selection is set via

AD7/SA4 = 0

AD6/SA3 = 0

AD5/SA2 = 1

AD4/SA1 = 0

AD3/SA0 = 1

The signals can be directly connected to +3.3 V or GND.

The CSQ, DCLK, DIN, and DOUT of several VINETIC®-2CPE/-1CPE devices can be mutually connected to share the same serial host interface when the device is used with the PG-TQFP-100 package. When the device in the PG-TQFP-64 package is used, then only DCLK, DIN and DOUT can be connected.

The interrupt line (INTQ) is active low and is an open drain output. Several VINETIC®-2CPE/-1CPE devices can be connected using a pull-up resistor of for example 1.2 kΩ.

Figure 2 shows pull-up resistors for DIN, DOUT, INTQ and RDYQ. The DIN and DOUT lines are only driven (high or low) by the VINETIC®-2CPE/-1CPE or the host controller during data transmission. Hence pull-ups prevent floating lines at pins DOUT, DIN, INTQ and RDYQ. The frequency for A4/DCLK can be within a range of 0 kHz and 8.192 MHz.

It must be ensured that the chip select line has high level after reset. If the chip select line can be floating (GPIO of the host controller is input after reset) a pull-up resistor of 2.2 kΩ must be provided.

Unused data, address and control lines must be connected to GND (see Table 10 Host Interface pins in **[1]**).

2.1.2 Parallel Interface Type: 8-bit INTEL Multiplexed Mode + PCM

The block diagram in **Figure 3** shows how to connect an Intel micro controller interface to the VINETIC®-2CPE/-1CPE. To fulfill the timing of the chip select signal an additional circuitry, as described in **Chapter 2.2**, may be necessary.

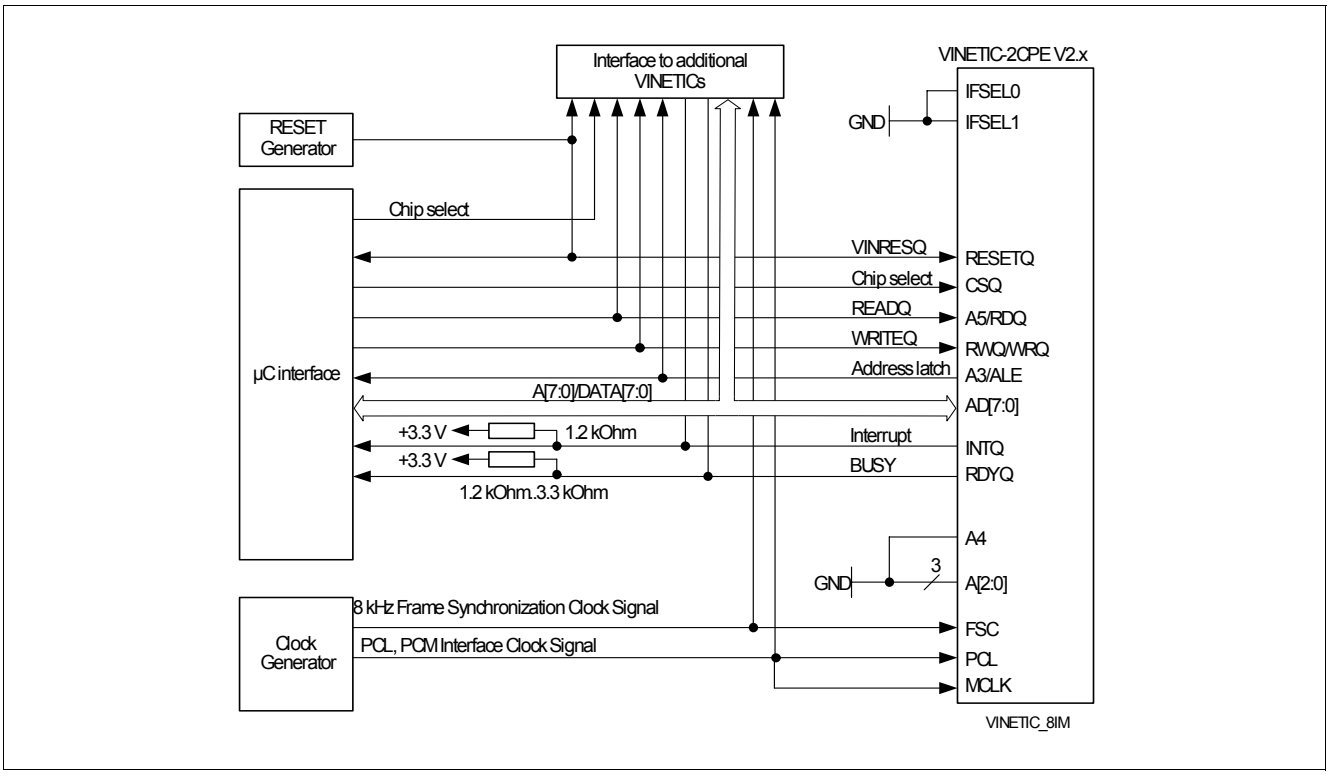


Figure 3 Parallel Interface Type: 8-bit INTEL Multiplexed Mode + PCM

The 8-bit INTEL multiplexed mode is selected by connecting the IFSEL pins (IFSEL[1:0]) to the following logic levels:

IFSEL1[1)] = 0

IFSEL0 = 0

The interrupt and ready outputs are open-drain. Several VINETIC®-2CPE/-1CPE devices can be connected with each other using pull-ups of 1.2 kΩ.

It must be ensured that the chip select line has high level after reset. If the chip select line can be floating (GPIO of the host controller is input after reset) a pull-up resistor of 1.2 kΩ must be provided.

Unused data, address and control lines must be connected to GND (see Table 10 Host Interface Pins in **[1]**).

The default byte ordering in the Intel mode at the data bus is low byte before high byte (little endian).

2.1.3 Parallel Interface Type: 8-bit INTEL Demultiplexed Mode + PCM

The block diagram in **Figure 4** shows how to connect an Intel micro controller interface to the VINETIC®-2CPE/-1CPE. To fulfill the timing of the chip select signal an additional circuitry, as described in **Chapter 2.2**, may be necessary.

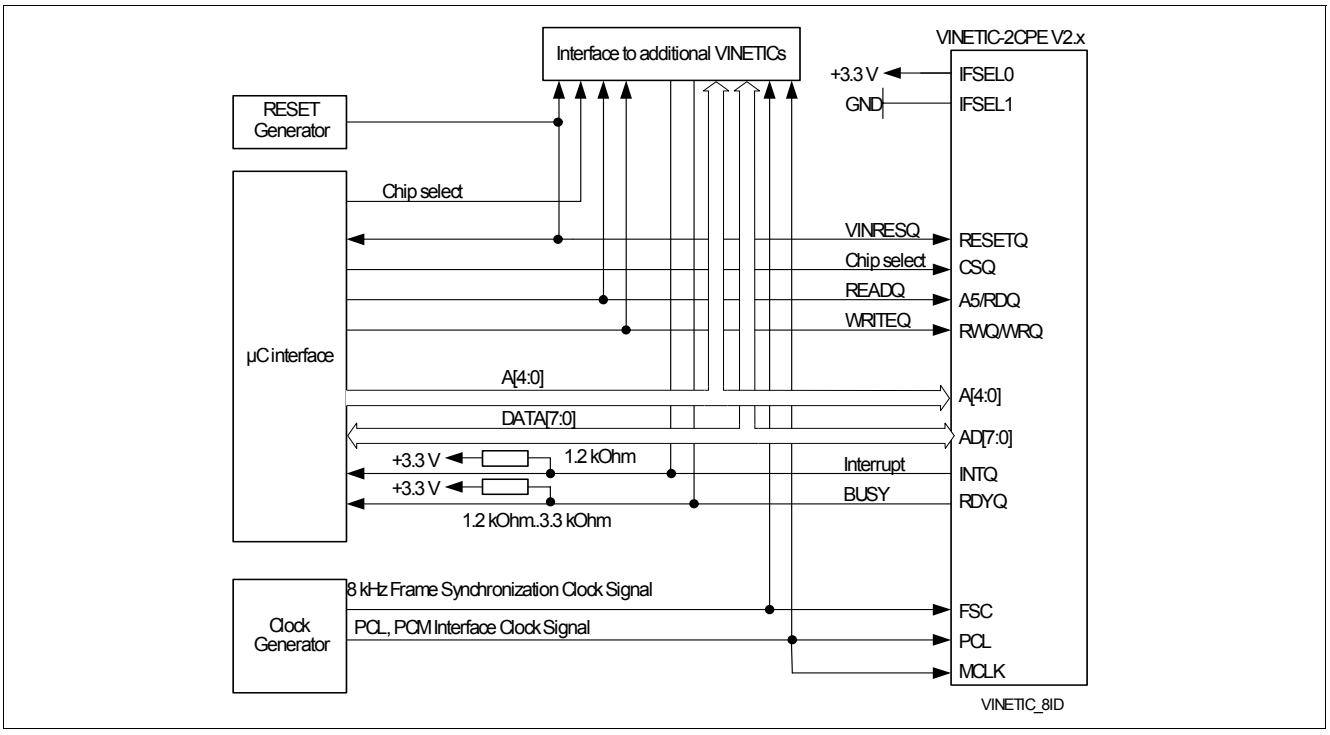


Figure 4 Parallel Interface Type: 8-bit INTEL Demultiplexed Mode + PCM

The 8-bit INTEL demultiplexed mode is selected by connecting the IFSEL pins (IFSEL[3:0]) to the following logic levels:

IFSEL1[1)] = 0

IFSEL0 = 1

The interrupt and ready outputs are open-drain. Several VINETIC®-2CPE/-1CPE devices can be connected using pull-ups of 1.2 kΩ.

In Intel demultiplexed mode, the VINETIC®-2CPE/-1CPE has five address lines. They may be connected to the addresses A[4:0].

1)IFSEL[1:0] is not supported by the package PG-TQFP-64 of the VINETIC®-2CPE/-1CPE.

It must be ensured that the chip select line has high level after reset. If the chip select line can be floating (GPIO of the host controller is input after reset) a pull-up resistor of 1.2 kΩ must be provided.

The default byte ordering in the Intel mode at the data bus is low byte before high byte (little endian).

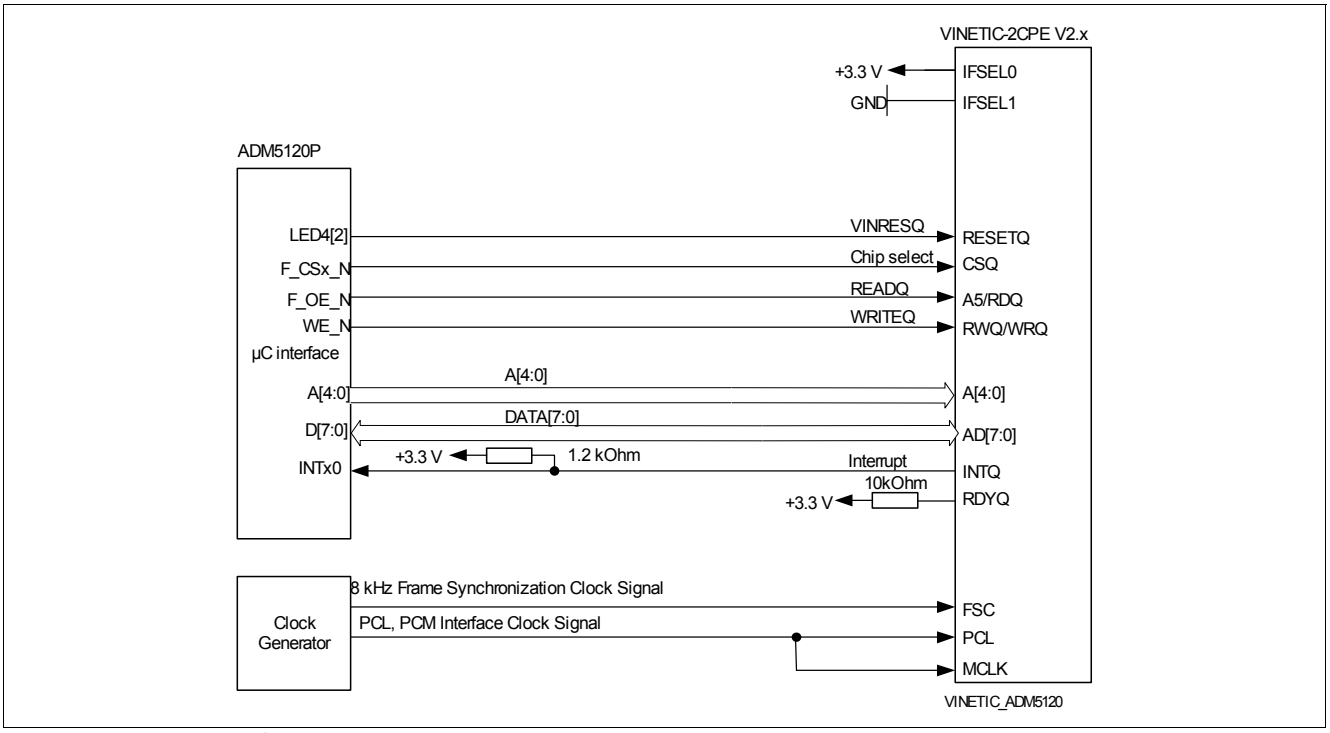


Figure 5 VINETIC®-2CPE/-1CPE Connected to ADM5120

2.1.4 Parallel Interface Type: 8-bit MOTOROLA Mode + PCM

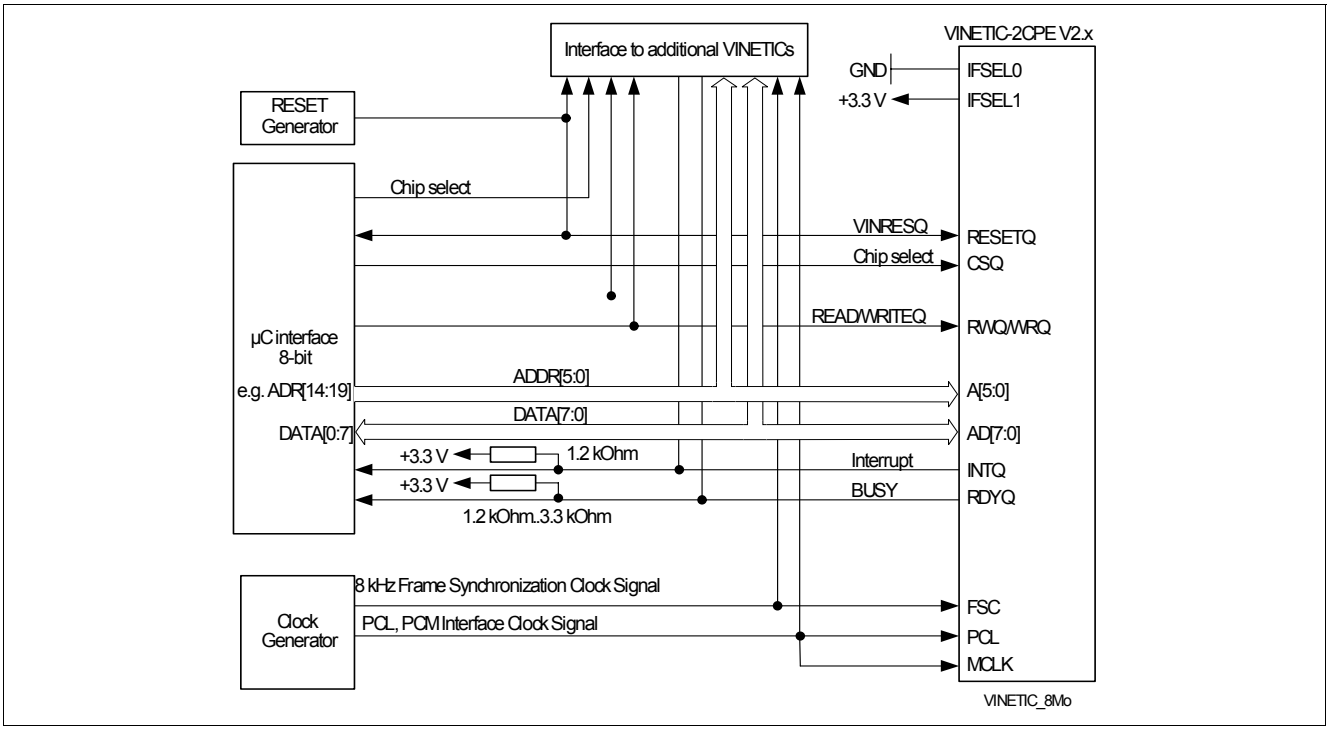


Figure 6 Parallel Interface Type: 8-bit MOTOROLA Mode + PCM

The 8-bit MOTOROLA mode is selected by connecting the IFSEL pins (IFSEL[3:0]) to the following logic levels:

IFSEL1[1)] = 1

IFSEL0 = 0

The interrupt and ready outputs are open-drain. Several VINETIC®-2CPE/-1CPE devices can be connected using pull-ups of 1.2 kΩ.

It must be ensured that the chip select line has high level after reset. If the chip select line can be floating (GPIO of the host controller is input after reset) a pull-up resistor of 1.2 kΩ must be provided.

Data Bus Interface

The Motorola processors have a different mode in comparison to Intel processors. When a Motorola processor is connected the data lines must be swapped according to **Table 1**. Little endian and big endian are different modes with respect to the sequence of the data bytes.

Little-endian: Low-order byte is stored at the lower address and high-order byte is stored at the higher address.

Big-endian: High-order byte is stored at the lower address and the low-order byte at the higher address.

The VINETIC®-2CPE/-1CPE has an 8-bit interface, although the internal architecture is 16-bit.

The reset behavior for the Motorola Interface is big-endian mode, therefore in the Motorola interface mode the low byte must be transfered before the high byte. The reset behavior for all other interfaces is little-endian.

The default byte ordering in the Motorola mode at the data bus is high byte before low byte (big endian).

1)IFSEL[1:0] is not supported by the package PG-TQFP-64 of the VINETIC®-2CPE/-1CPE.

Table 1 Data Bus Connection in 8-bit MOTOROLA Mode

Motorola Data Pin	VINETIC® Data Pin
D0 (MSB)	AD7 (MSB)
D1	AD6
D2	AD5
D3	AD4
D4	AD3
D5	AD2
D6	AD1
D7 (LSB)	AD0 (LSB)

Address Interface

The address lines must be swapped in the Motorola mode as well. For example, when the host controller has the address lines ADDR[20:0] then A[0] of VINETIC®-2CPE/-1CPE must be connected to ADDR[20], A[1] is connected to ADDR[19] and accordingly for the remaining address pins.

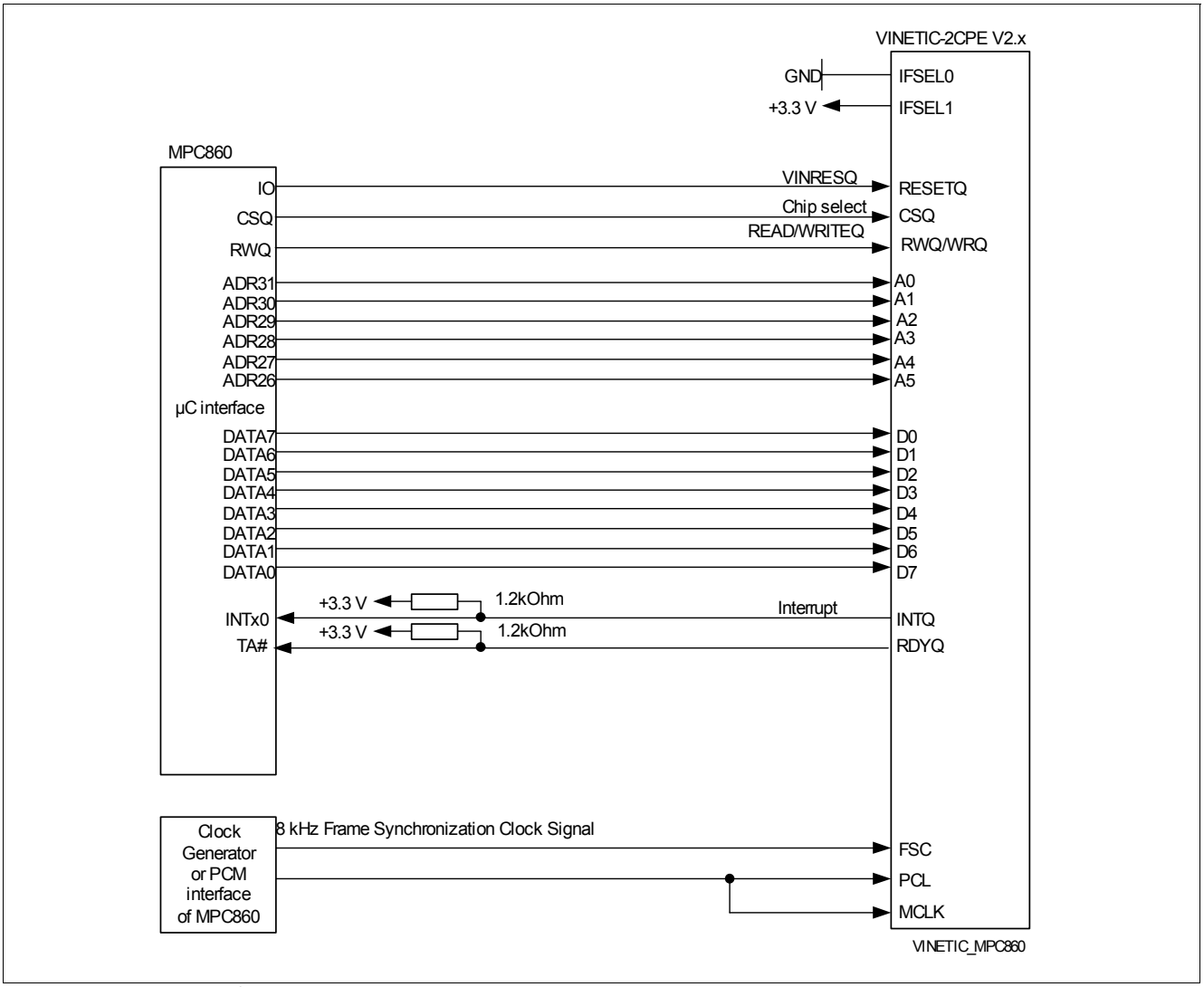


Figure 7 VINETIC®-2CPE/-1CPE Connected to MPC860

2.2 Additional Circuitry for the Chip Select Signal

When the address setup time can not be fulfilled in the INTEL modes by the host controller a circuitry shown in **Figure 8** is recommended to be inserted between the host controller and the VINETIC®-2CPE/-1CPE. The timing is described in figures 14..19 in **[1]**.

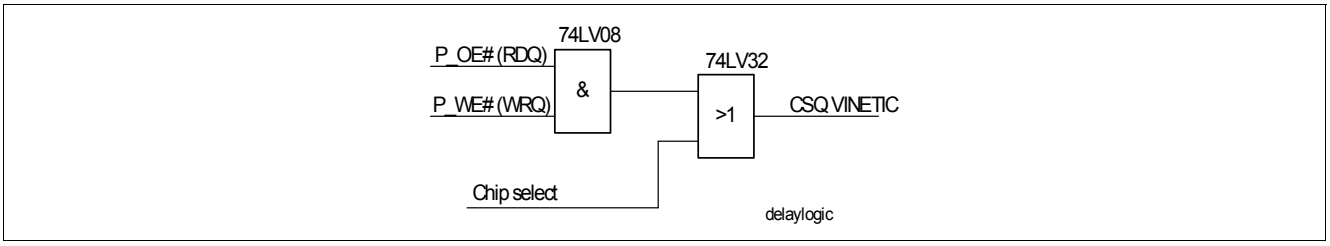


Figure 8 Additional Chip Select Logic for some Host Controllers

2.3 RDYQ Signal

The VINETIC®-2CPE/-1CPE Version 2.1 RDYQ open-drain output signal, with an external pull-up 1.2...3.3 kΩ resistor, is recommended to be connected to the Motorola PowerQUICC Family External Bus Interface, Transfer Cycle Termination, Transfer Acknowledge (*TA) input pin. When the signal is not used, the software must ensure that the access time is always long enough. The VINETIC®-2CPE/-1CPE pulls the signal low after it is finished reading or writing the data. The host controller can then finish the access and disable the chip select signal. This is the indication for the VINETIC®-2CPE/-1CPE to disable the RDYQ signal (high level).

2.4 Reset

The VINETIC®-2CPE/-1CPE has no internal power-on reset function. It has one active low reset input pin called RESETQ. After power-on of the system the RESETQ has to be pulled low for at least 20 µs. RESETQ has a spike rejection that will safely suppress spikes with a duration of 2 µs.

Before deactivation of the RESETQ signal all power supplies (+1.5 V and +3.3 V) for the VINETIC®-2CPE/-1CPE and the clocks (FSC, PCLK and MCLK) have to be stable (see **Chapter 2.5**). No power-on sequence must be performed for the VDD15[1)] and VDD33[2)] supply voltages. It is mandatory to apply the signal voltages after the VDD15 and VDD33 voltages are supplied and stable.

After deactivation of the RESETQ signal (rising edge) the VINETIC® internal PLL starts off synchronization and after the PLL is locked the internal reset routine starts. After completion of the reset routine the host controller access to the VINETIC®-2CPE/-1CPE is possible. The internal reset routine will take approx. 2 ms.

2.5 Clock Distribution

For the VINETIC®-2CPE/-1CPE Version 2.1 or newer the following three clocks must always be provided, regardless of the PCM interface being used or not:

- PCL
- FSC (8 kHz)
- MCLK

The FSC, PCL and MCLK must always be provided, even when the PCM interface is not used. All three clocks have to be synchronous, stable and phase locked (see chapter 4.3.2. in **[1]**). An internal PLL generates all internal clocks from the MCLK and FSC.

1) VDD15, VDD15_A, VDD15_B, VDD15_AB
2) VDD33, VDD33_A, VDD33_B

The PCL and MCLK can be used from 512 kHz up to 8.192 MHz in steps of 512 kHz. The data rate of the PCM interface is identical to PCL if used in single clocking mode, or half the PCL frequency if used in double clocking mode.

There are two main applications with different ways to generate the clocks for the VINETIC®-2CPE/-1CPE:

- Application with a central distributed clock, for example an application with PCM interface.
- Local clock generation for the VINETIC®-2CPE/-1CPE in CPE designs with POTS functions, for example.

2.5.1 Application with Distributed Clocks (e.g. via PCM)

In systems like CPE applications with PCM interface there is a central clock distribution unit. The clock distribution can either be done inside a connected device within the application or an external PLL is used to synchronize to a reference clock, for example a modem with ISDN interface. If the reference clock distribution fails or is unstable the clock must be switched to a free running stable clock. This is done in front of the external PLL. The PLL has to generate the stable clock in a way that the PLL unit does not generate a glitch. Such a glitch would increase the jitter (or even lock-out the PLL). The PLL generates all clocks for the VINETIC®-2CPE/-1CPE, that means the FSC, PCL and the MCLK. Sometimes the external PLL has an output to show the status of the PLL. The resynchronization of the external PLL must be done very smoothly to generate synchronization of the VINETIC®. It must be ensured that the PCL and MCLK clocks always have the correct number of clock periods in a FSC frame.

The PCM interface clock PCL must be directly connected to the master clock MCLK.

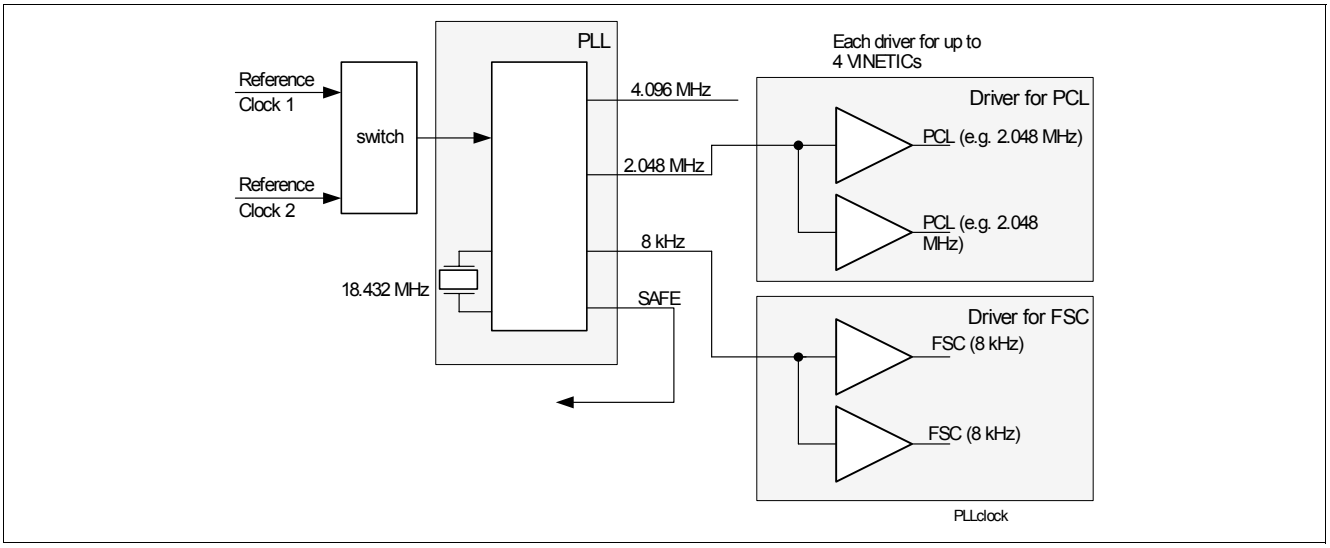


Figure 9 PLL for Generation of PCM Clocks from one of two Reference Clocks

In **Figure 9** for example the external PLL from Cypress CY26049-36 is shown. The reference input frequency of the PLL is 8 kHz and it delivers 8 kHz, 2.048 MHz and 4.096 MHz. It has a status output called SAFE. When the PLL is locked the SAFE output is high. The block switch has three functions: it checks both reference clocks, switches to one of them and divides the clocks to 8 kHz, which is the reference signal for the PLL.

When the SAFE output of the PLL detects an unsynchronous clock signal the VINETIC®-2CPE/-1CPE must be reset so that the clocks become stable again.

2.5.2 Local Clock Generation

In systems where no reference clock is available (for example a crystal oscillator with a synchronous divider or a crystal with a ripple counter are used), the PCL and the frame signal FSC must be locally generated. **Figure 10** shows a clock distribution with a crystal oscillator and a synchronous divider. The maximum frequency of this

generator is 8.192 MHz and the minimum frequency is 2.048 MHz and depends on the circuit used. With ripple counter other frequencies can be realized (see **Figure 11**).

Figure 10 and **Figure 11** show only two examples of how to set up a clock distribution block for the VINETIC®-2CPE/-1CPE.

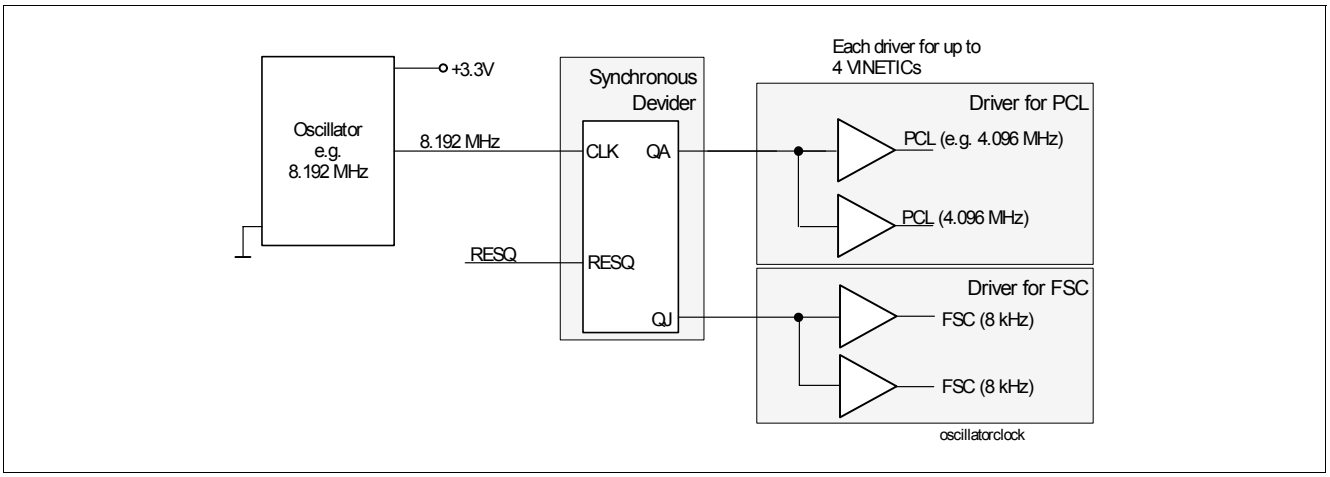
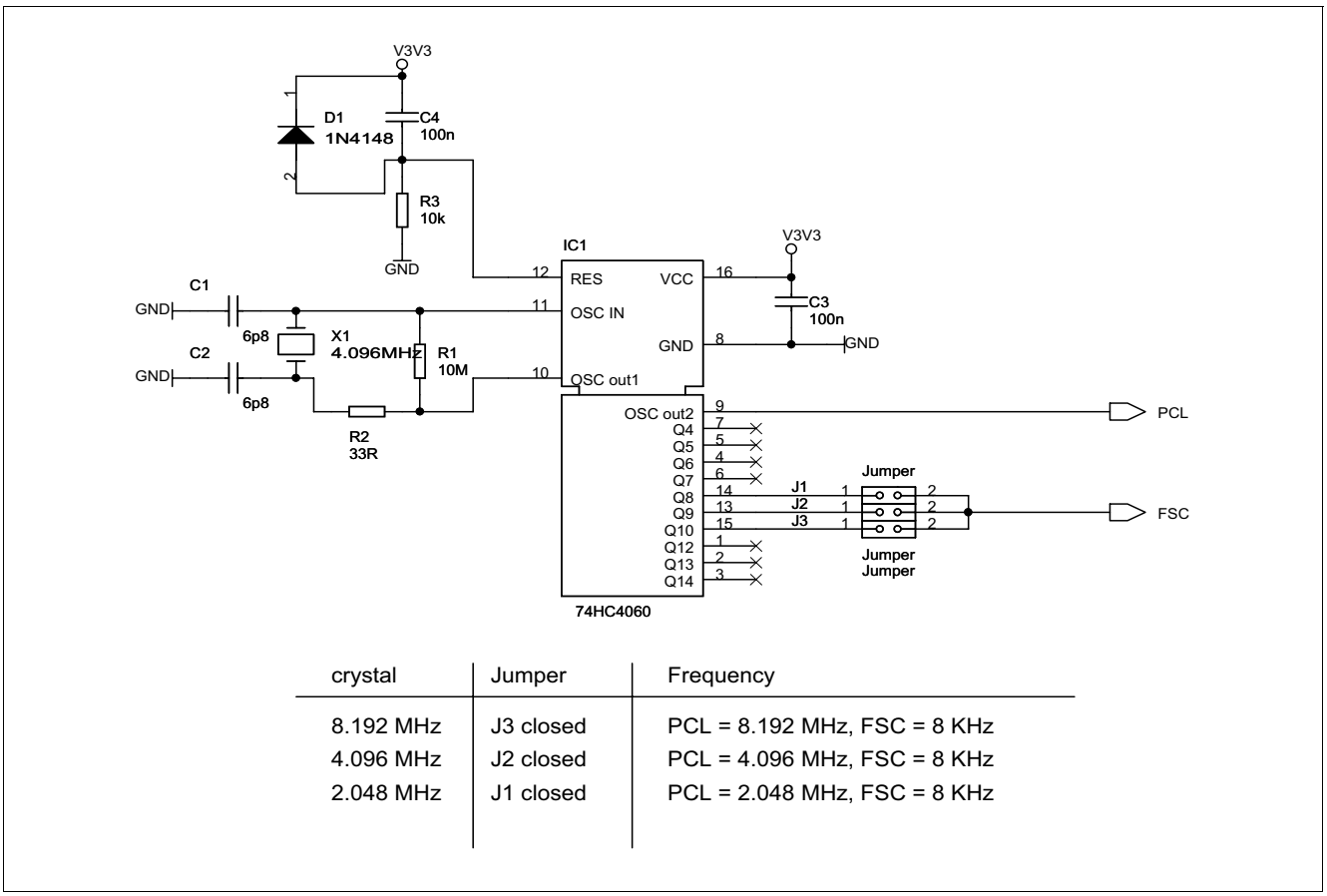


Figure 10 Clock Distribution by Crystal Oscillator and Synchronous Divider



crystal	Jumper	Frequency
8.192 MHz	J3 closed	PCL = 8.192 MHz, FSC = 8 KHz
4.096 MHz	J2 closed	PCL = 4.096 MHz, FSC = 8 KHz
2.048 MHz	J1 closed	PCL = 2.048 MHz, FSC = 8 KHz

Figure 11 Clock Distribution by Crystal and Ripple Counter

2.6 PCM Interface

One external PCM highway is available on the VINETIC®-2CPE/-1CPE. A second highway is internally available and cross connected to the external PCM interface (external DX = internal DX1 and it is connected to internal DR2; external DR = internal DR1 and it is connected to internal DX2), see **Figure 12**. In the case of the PCM highway B is used, the pin DR (input of PCM highway) is output of the internal highway B. This feature must be taken into account that the data is corrupt when the same timeslot on the internal highway B and on the external highway is used. Therefore, both highway signals DR and DX needs a pull-up resistor, because both pins are internally connected to open-drain output drivers.

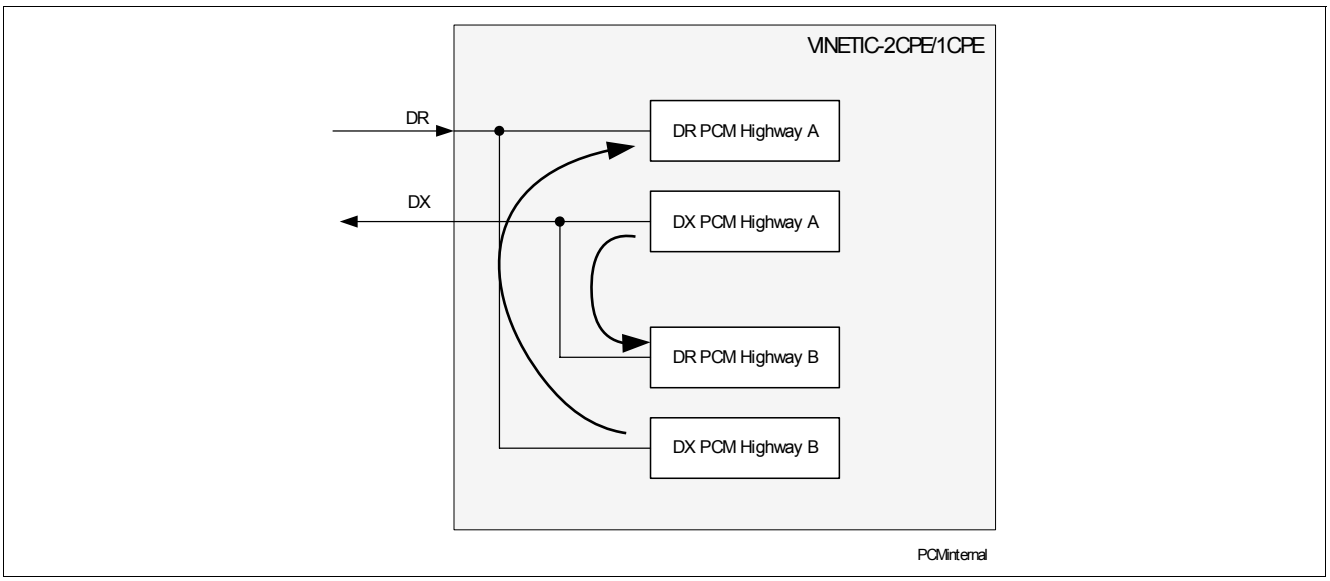


Figure 12 Internal PCM-Highway Connection

The highway is clocked by PCL[1)] (only multiples of 512 kHz are allowed) and FSC (8 kHz) inputs.

The FSC and PCL signals must always be synchronous and in phase. The rising edges of the FSC and the PCL must be aligned, too.

For the timing characteristics of the PCM Interface clocks, about possible PCM data clocks (PCL) and the maximum possible number of time slots that can be assigned to one PCM highway, please refer to the PCM Interface" chapter of **[2]**.

The PCM highway offers a time slot control pin (TC1Q). This pin is intended to control an external buffer device when a PCM highway needs to be multiplexed. The TC1Q pin is open drain. When the pin is used to control external buffer devices, a pull-up resistor needs to be used (e.g. of 2.2 kΩ).

1) Valid PCL clock rates are f = n x 512 kHz (1 ≤ n ≤ 16).

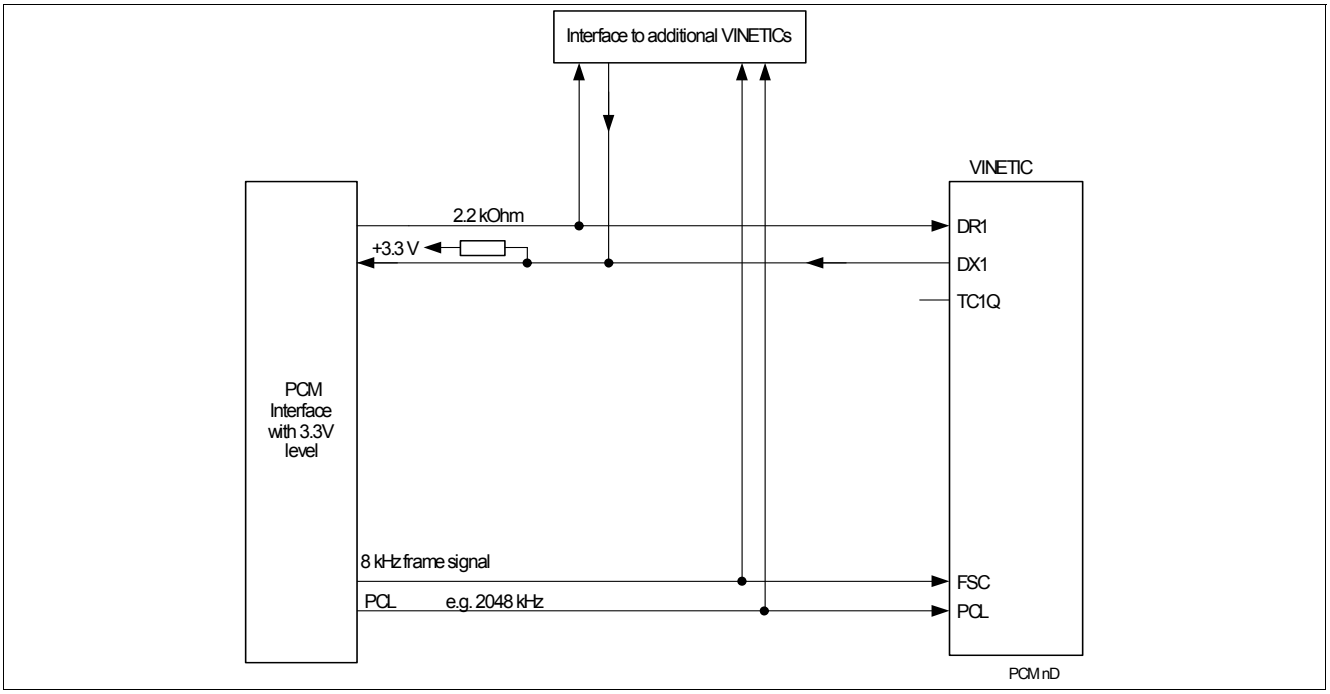


Figure 13 PCM Highway and no Driver at +3.3 V PCM Highway

The PCM highway output DX1 should also be tied high to +3.3 V using a 2.2 kΩ pull-up resistor. The PCM highway input DR1 should also be tied high to +3.3 V using 2.2 kΩ pull-up resistors.

Since the DR1 and DX1 are I/O pins to enable the cross-connection of the 2 internal PCM highways the DR1 and DX1 pins, if not used, should be connected via a pull-down-resistor (for example 1 kΩ) to GND to make sure that nothing is floating. When a transmit timeslot of the PCM highway B (DX2) is enabled, the data is output on the input pin DR1. In this case the system must be set this timeslot to tristate on the external PCM highway.

Note: Do not leave these pins floating.

The VINETIC®-2CPE/-1CPE has +3.3 V tolerant IOs only. As many PCM highways are +5 V systems in such a case a driver has to be placed as a level shifter between both “worlds”. The driver in the receive direction is of a different type than in transmit direction, due to the needed power supplies. In the direction from VINETIC®-2CPE/-1CPE to the PCM highway a SN74LS125 with +5 V power supply and in the direction from PCM highway to VINETIC®-2CPE/-1CPE a SN74LVT125 with +3.3 V power supply can be used.

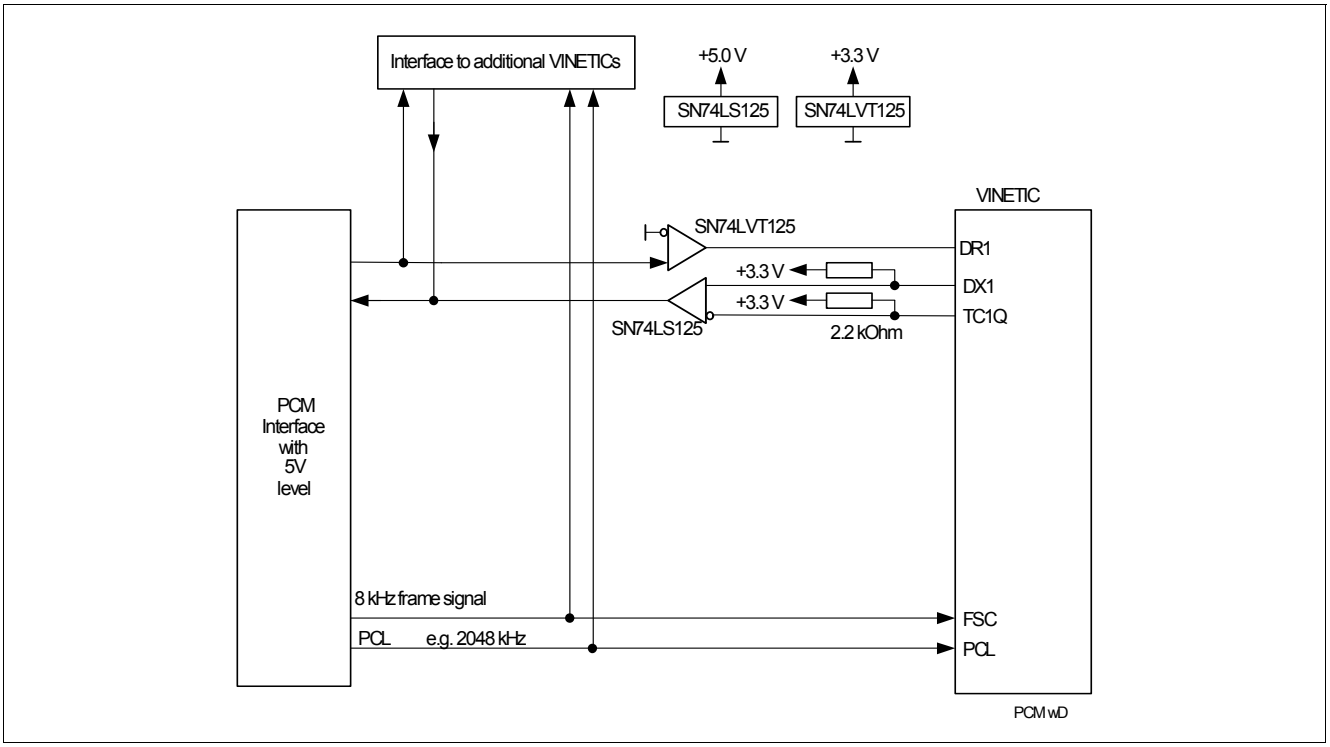


Figure 14 PCM Interface with Driver at +5 V PCM Highway

2.7 JTAG

The VINETIC®-2CPE/-1CPE offers a JTAG Interface for Boundary Scan support.

The JTAG Interface comprises the pins TRSTQ, TDI, TDO, TMS, and TCK. These pins must be connected to a defined potential via 10 kΩ resistor (pull-up/pull-down) when the JTAG Interface is used.

The TRSTQ needs a reset signal (active low) before the JTAG interface can be used. The boundary scan test equipment must support the JTAG reset signal.

When the JTAG Interface is not used, all JTAG related input pins must be tied to GND (TMS, TCK, TDI and TRSTQ). The JTAG output TDO must be left open when JTAG is not used.

2.8 GPIOs

The VINETIC®-2CPE/-1CPE in the PG-TQFP-100 package offers digital general purpose GPIO pins. If a GPIO pin is not used, it should be connected to ground via a 10 kΩ resistor. In order to ensure that it is never configured as an output, this pin can directly be connected to ground.

2.9 Analog Interfaces

The VINETIC®-2CPE/-1CPE has up to 2 analog interfaces, each one including an AC loop, a DC loop and a control interface. The AC path is used for the typical Codec functionalities: voice AD and DA conversion, impedance matching, gain adjustement, hybrid and ringing.

The DC loop provides the DC Feeding (48 V open loop voltage).

The analog interface has two channel specific input pins for line testing and two control lines with ternary logic to set the mode of the SLIC.

2.9.1 Signal Interfaces

The AC and DC paths include all types of signals like voice, ringing and feeding, and also the howler tone. In receive direction, the voltage information is transferred via the differential interface DCP/DCN and ACP/ACN, whereas in transmit direction the transversal current IT carries the line current information. An RC network serves for current/voltage conversion and AC/DC separation.

2.9.2 Control Interfaces

The various SLIC operating modes are controlled by the ternary interfaces C1 and C2.

3 Design Guidelines for SLICs

This chapter describes the external components at SLIC-DC. For the circuitry of the DC/DC converter please refer to [7].

3.1 VINETIC®-SLIC Interface

3.1.1 Signal Interfaces

AC and DC paths are formed by feeding voltages to the line and measuring line currents. In receive direction, the voltage information is transferred via the differential interface pins DCP/DCN and ACP/ACN, whereas in transmit direction pin IT contains the line current information. An RC network serves for current/voltage conversion and AC/DC separation.

3.1.2 Influence of External Components

Figure 15 shows the 6 external components of the VINETIC®-SLIC interface.

There are 6 external components between VINETIC® and SLIC. They have an influence on the CRAM coefficients calculated by the coefficient calculation program VINETICOS. The SLIC scales down the transversal line current by a factor of 50 wheres the resistor at the pin IT transforms it into a voltage. The SLIC pin IT carries the scaled current reflected by the SLIC. The VINETIC® measures the voltage at the input pin IT, and the feedback voltage is transferred back to the SLIC through the DCP-DCN pins. A filter capacitor is designed differentially between DCP and DCN for optimizing the noise performance.

3.1.2.1 External Components between SLIC and VINETIC®

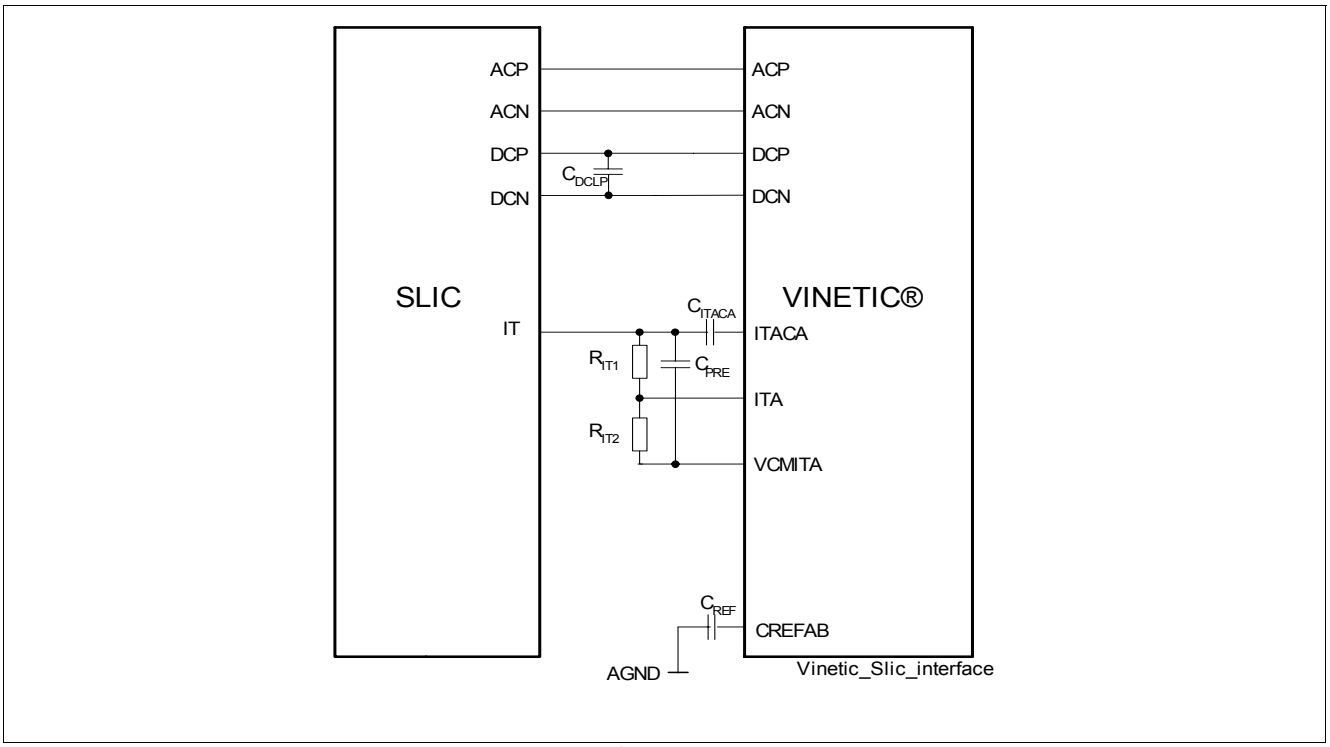


Figure 15 Interface between SLIC and VINETIC®

The recommended values of these components are:

C_{DCLP} = 100 nF, 6.3 V, 10%

C_{ITAC} = 1 µF, 10 V, 10 %

C_{REF} = 68 nF, 10 V, 20 %

C_{PRE} = 4.7 nF,10 V, 5 %

R_{IT1} = 499 Ω, 1 %

R_{IT2} = 499 Ω, 1 %

The SLIC senses the transversal line current, scales it down and outputs it at pin IT.

The relationship between the scaled current I_{IT} and the actual line currents in Tip (I_T) and Ring (I_R) line is given by:

$$I_{IT} = (I_T + I_R)/100 = I_{TRANS} / 50 \quad (1)$$

$$I_{TRANS} = (I_T + I_R)/2 \quad (2)$$

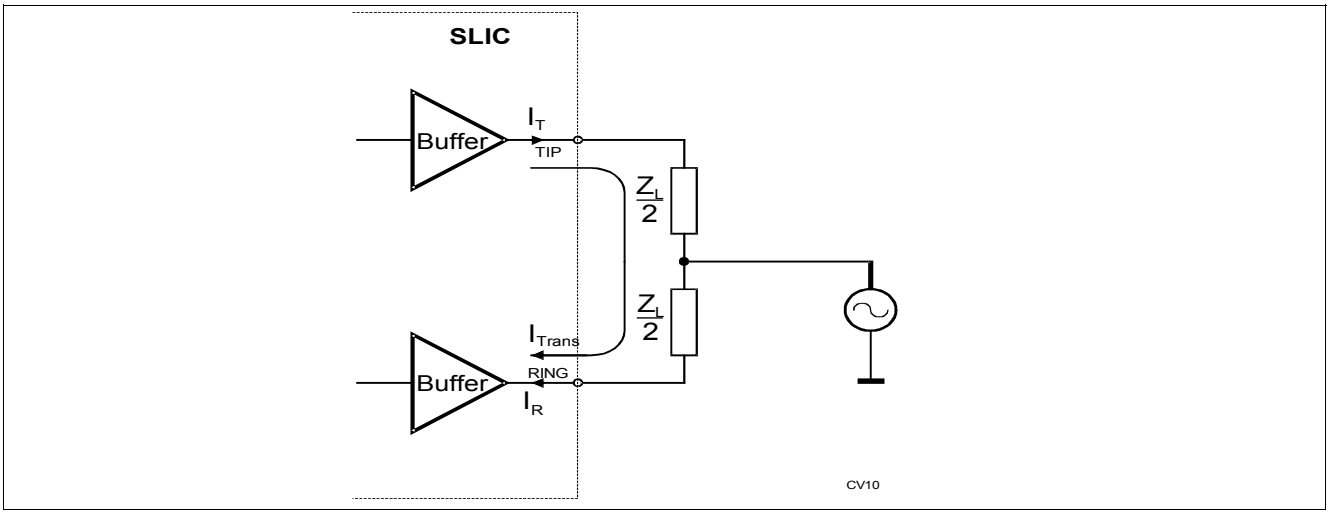


Figure 16 Transversal Currents

I_{IT} represents the transversal line current.

The pin IT of SLIC-DC is a current output. The resistors R_{IT1} and R_{IT2} are used to convert this current into a voltage.

The potential V_{IT} at the IT pin of the VINETIC® is described as:

$$V_{IT} = \text{VCMITx} - I_{IT} * R_{IT2} = \text{VCMITx} - (I_T + I_R)/100 * R_{IT2} \quad (3)$$

VCMITx stands for VCMITA or VCMITB and is a virtual ground supplied by the VINETIC® (typically 0.75 V).

The voltage at V_{IT} input of the VINETIC® represents the transversal current on the line. This value is used to control the DC feeding loop.

The capacitor in front of the ITAC input separates the AC from the DC component. The voltage at ITAC goes into the AC control loop.

$$V_{ITAC} = I_{IT} * (R_{IT1} + R_{IT2}) = (I_T + I_R)/100 * (R_{IT1} + R_{IT2}) \quad (4)$$

If R_{IT1} and R_{IT2} deviate from the default values (R_{IT1} = 499 Ω, R_{IT2} = 499 Ω), all programmed voice levels in transmit direction would deviate from the calculated ones. Return loss and transhybrid loss will also be influenced if R_{IT1} and R_{IT2} deviate from the default values.

As VINETICOS calculates with R_{IT1} = 499 Ω and R_{IT2} = 499 Ω, it is definitely required to use the recommended values and **not to change** these values. Recommend tolerance for R_{IT1} and R_{IT2} is 1%.

3.1.2.2 C_{ITAC}

Recommended value: 1 µF

This capacitor is in series to the ITAC input pin of the VINETIC®. It separates the AC from the DC component of transversal current I_{TRANS}. C_{ITAC} and the input impedance of the AC input filter build a highpass filter with a cut-off frequency of roughly 10 Hz.

As VINETICOS calculates the AC coefficients based on a value of 1 µF, it is recommended not to change this value.

3.1.2.3 C_{PRE}

Recommended Value: 4.7 nF

This capacitor is in parallel to the resistors R_{IT1} and R_{IT2} and builds a lowpass filter with a cut-off frequency of 33.8 kHz. The lowpass reduces the out of band noise from the SLIC and ensures stability to the impedance loops.

3.1.2.4 C_{REF}

Recommended value: 68 nF

This capacitor is used for filtering the internal bandgap reference voltage.

The minimum value used should be 68 nF.

3.1.2.5 C_{DCLP}

Recommended value: 100 nF

This external noise filter capacitor is placed in the DCP/DCN lines. It must be placed with very short traces to the SLIC.

3.2 Tip-Ring Interface: C_{STAB}, R_{STAB}, R_{PROT} and C_{EMC}

Optional - recommended values in noisy environment:

C_{EMC}: 100 pF

C_{STAB}: 15 nF

R_{STAB}: 20 Ω for SLIC-DC and 30 Ω for SLIC-E

R_{PROT}: 20 Ω (value depending on protection scheme)

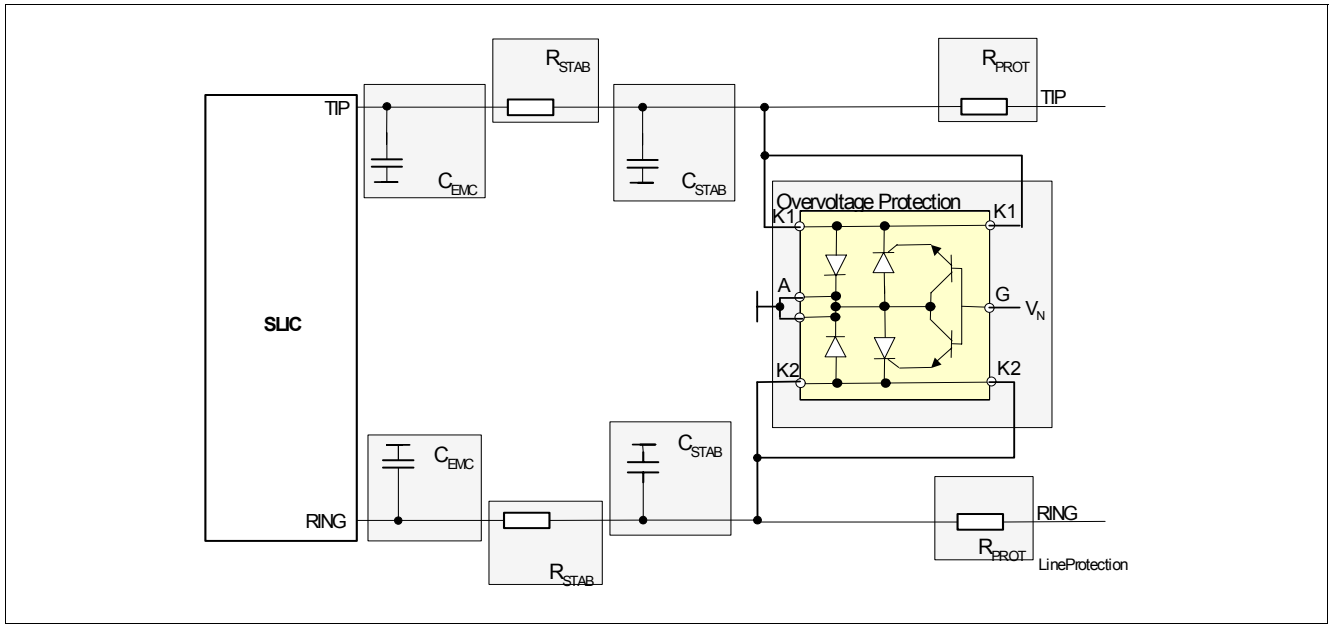


Figure 17 Tip-Ring Interface

3.2.1 C_{STAB}

The proposed capacitors help to ensure stability for all line conditions and also contribute to EMC immunity. 15 nF/100 V caps are recommended. Increasing the value up to 25 nF should be uncritical. VINETICOS also calculates and plots the input impedance up to 1 MHz. There will be an error message, if the real part of the input impedance is negative. This is a criterion for the stability of the system. For negative values the stability cannot be guaranteed for all line conditions (for example a short cut). This error message must not be ignored.

Increasing C_{STAB} results in better out of band noise performance and higher stability margin for complex AC impedances (for example impedance for Germany). It also causes worse stability for pure resistive AC impedances.

A changed value for C_{STAB} has to be taken into account when calculating coefficients with VINETICOS. The SLIC circuitry definition of VINETICOS allows changing of C_{STAB} value.

The maximum stress for the capacitor occurs when the over-voltage protector (thyristor) fires. Because the capacitor in the stability network is connected to GND by the very low impedance track over the thyristor, the capacitor will discharge to GND.

3.2.2 R_{STAB}

Recommended value: 20 Ω for SLIC-DC

Recommended value: 30 Ω for SLIC-E

The value for R_{STAB} can be increased up to 40 Ω. A minimum value of 20 Ω (30 Ω for SLIC-E) is required to guarantee system stability. The actual value for R_{STAB} has to be taken into account when calculating coefficients with VINETICOS. The SLIC circuitry definition of VINETICOS allows changing of R_{STAB} value.

Changing R_{STAB} also influences the pole frequency of the RC filter (R_{STAB}, C_{STAB}).

If R_{STAB} is increased, the out of band noise performance and the stability for pure resistive AC impedances will be improved. Increasing R_{STAB} also means to increase the voltage drop caused by line feeding. This might be an issue in power critical applications.

The tolerance matching of the two R_{STAB} resistors in Tip and Ring line also influences the longitudinal balance performance.

3.2.3 R_{PROT}

Recommended value: 20 Ω (actual value depending on protection scheme)

The value for R_{PROT} can be changed up to 50 Ω. This value has to be taken into account when calculating coefficients with VINETICOS. The SLIC circuitry definition of VINETICOS allows changing of R_{PROT} value.

The function of R_{PROT} is to limit the current into the protection device in case of a foreign voltage contact (lightning, power contact). R_{PROT} and C_{STAB} also form a lowpass filter which helps to improve EMC behavior. By changing R_{PROT} the characteristic of this filter is changed, too.

R_{PROT} also influences the stability of the impedance matching loop but this can be compensated by changing R_{STAB}.

The pins TIP and RING of SLIC-DC has internal 10 Ω. This value has to be taken into account when calulating the value of R_{PROT}. VINETICOS calculates with this internal resistor value of 10 Ω.

To increase R_{PROT} means to decrease the current in case of a foreign voltage contact and to increase the voltage drop caused by the line feeding (might be an issue in power critical applications). R_{PROT} should be rated for lightning surge currents and also should act as a fuseable resistor in order to open the line in case of a power contact.

The tolerance matching of the two R_{PROT} resistors in Tip and Ring line also influences the longitudinal balance performance.

Note: In order to be able and flexible to meet worldwide AC impedance requirements it is recommended to have R_{STAB} + R_{PROT} > 50 Ω for SLIC-E, T-SLIC-E and R_{STAB} + R_{PROT} > 40 Ω for SLIC-DC.

3.2.4 Capacitors for Enhanced EMC Requirements C_{EMC}

To fulfill the EMC requirements in noisy environments, two additional 100 pF/100 V capacitors at TIP/RING are recommended at the TIP and RING pins at the SLIC. These capacitors and optional and must be placed directly at the pins to GND. The traces from the pins to the capacitors have to be as short as possible.

3.3 Additional Protection Devices at the Line

In general, gate-triggered devices are recommended for overvoltage protection of the SLIC. These gate-triggered thyristors are “programmable”. Gate programmable devices track the substrate voltage of the SLIC. By connecting the gates of these battery tracking devices to the supply rails, overvoltages are limited to the supply rails of the SLIC.

Capacitors must be placed on the gate pin of the thyristor to provide the current for the thyristor to trigger when the fault condition on the line appears. These thyristors are switching very fast (a few nanoseconds). The current required for this fast thyristor switching must be provided by the gate capacitors.

*Note: Suitable protection circuits for SLIC-DC V1.2 can be found in detail in **[9]**. Suitable protection circuits for the SLIC-E can be found in **[10]**.*

3.4 External Circuitry for GR-909 Support

A resistive voltage divider at the Tip and Ring line is necessary to support GR-909 measurements. The requirements for the resistors depend on the foreign line peak voltage and the allowed leakage current. To calculate the correct resistor values, the analog inputs of the VINETIC® only allows a voltage between VCMITx ±0.7 V. The resistors[1)] must be able to withstand the peak power and voltage during overvoltage protection mode. Derived from overvoltage and longitudinal balance standards, they require both high power rating and good matching (± 1.0 % or better, depending on application).

1) These resistors are only required if GR-909 measurements need to be supported. In case no GR-909 support is required, these resistors are not needed.

The line testing network is typically connected to the TIP, RING and VCMITA or VCMITB respectively of the VINETIC®-2CPE/-1CPE (see **Figure 18**).

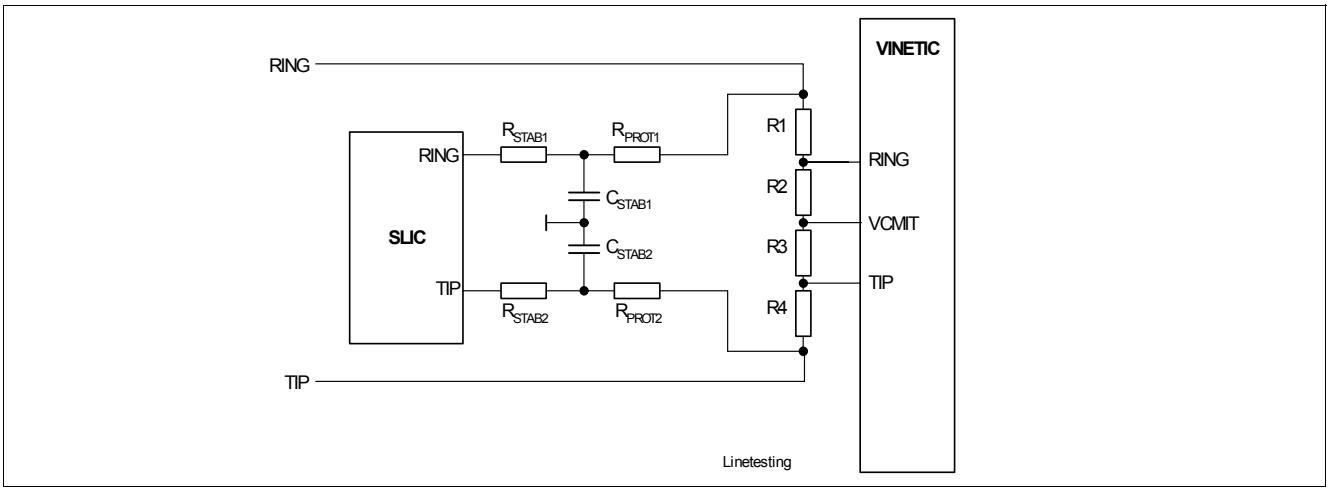


Figure 18 Line Testing Resistors at RING/TIP

Recommended resistor values are:

R1 = 1.5 MΩ

R2 = 3.3 kΩ

R3 = 3.3 kΩ

R4 = 1.5 MΩ

4 Power Supply and Grounding

4.1 General Overview of Power and Ground Planes

Usually four different supply areas are distinguished: the analog and the digital power planes and the signal ground and chassis ground planes.

General rules for power and ground planes are:

- Provide sufficient power and ground planes to have low-impedance current paths.
- Avoid power distribution using traces. This will add additional impedance, which can lead to a significant voltage drop.
- Split power planes to minimize the number of PCB layers.
- Avoid slots in the ground plane. This is fundamental for areas where high-frequency or sensitive analog signals are crossing over.
- Route high-speed signals above a continuous, unsplitted ground plane.
- The ground of the over-voltage protector should have a very low ohmic connection to the ground of the SLIC device.
- In two layer designs the ground planes at both sides must be connected with many vias.

4.1.1 Analog Power Plane

In mixed signal designs, it is essential to eliminate signal crosstalk and digital noise disturbers in the analog section of the PCB.

The analog power planes for the VINETIC®/SLIC section extend from the SLIC to the VINETIC®-2CPE/-1CPE analog Interface, including the complete circuitry between VINETIC®-2CPE/-1CPE and SLIC.

The following specific recommendations apply to the design and layout of the analog power planes with the VINETIC®-2CPE/-1CPE Chip Set Family:

- Divide the +3.3 V and the +1.5 V power plane into a minimum of two sections (as shown in **Figure 20**) to separate the digital (VDD15, VDD33) from the analog power supply (VDD15A, VDD15B, VDD15AB, VDD33AB).
- When dividing power planes, it is possible to save additional layers. Simply create cut-out regions in the dedicated power supply layer to form several copper areas.
- Join the analog and digital sections at multiple points by 0 Ω resistors, ferrite-beads or inductors, depending on the need for additional filtering.
- It is acceptable to supply all VINETIC®-2CPE/-1CPE and SLIC devices from one analog power plane. This analog plane can be multiple times connected to the digital power plane. Each junction must provide a low-impedance connection and additional filtering if necessary. It is also possible to have a small analog power plane for each device.
- Place high-frequency bypass capacitors (100 nF, 10 nF) near the supply pins of the devices. The Reference Schematics show the minimum decoupling requirements of each device.
- Place bulk capacitors (10 µF and higher) close to the appropriate devices to reduce distortions from transients. Choosing low ESR types (at analog power supplies).
- The battery power supply V_S can be routed in traces width 15 mil (1 mil = 0.0254 mm). This power supply does not need a plane. It is recommended to filter the supply by a 100 nF capacitor.
- In designs with SLIC-DC the power supply signals V_S and analog ground need seperate traces for each channel. The ground and V_S signals are connected at a star point placed near the power supply input at the bulk capacitor.

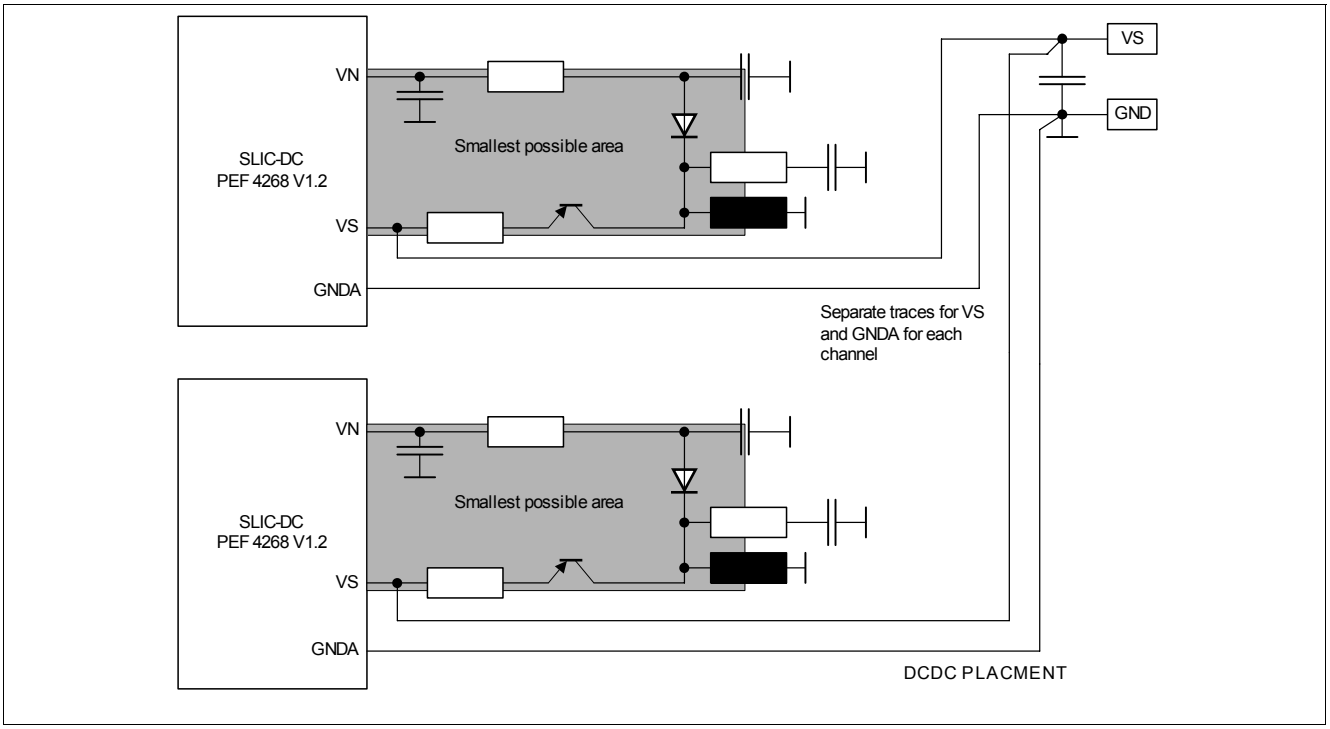


Figure 19 DC/DC Component Placement

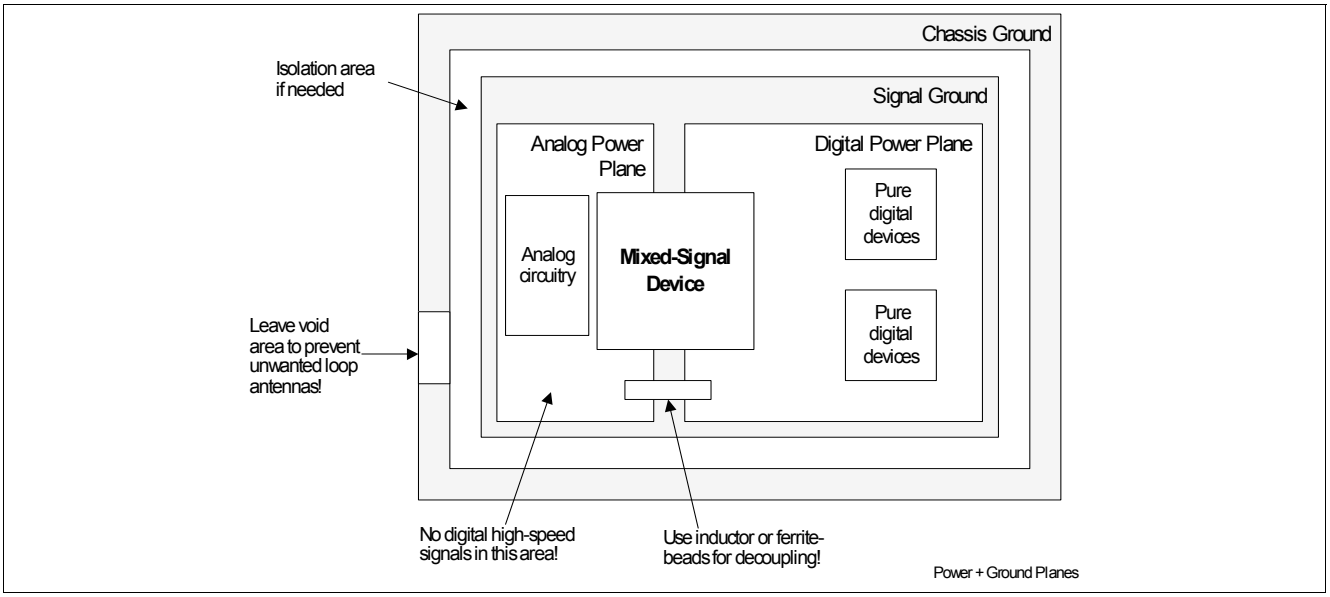


Figure 20 Analog Power Plane

4.1.2 Digital Power Plane

The digital power plane spans the area from the board edges, where the backplane connectors are located, to the digital parts of the VINETIC®-2CPE/-1CPE. The digital power plane supplies all digital parts of the VINETIC®-2CPE/-1CPE Chip Set Family (VDD15, VDD33). The analog parts should be decoupled from the digital power plane.

Some recommendations for the digital power plane include:

- For good capacitive coupling and resulting reduction in high-frequency voltage ripple, have a signal ground plane in a layer adjacent to a digital supply plane.

- When dividing the digital power plane, it is not necessary to add layers. Create cut-out regions in the dedicated power supply layer to form several copper areas.
- Place high-frequency bypass capacitors (100 nF, 10 nF) near the supply pins of the devices. The Reference Schematics show the minimum decoupling requirements.
- Place bulk capacitors (10 µF and higher) close to the appropriate devices. Choosing low ESR types provides reduced distortions.

4.1.3 Signal Ground Plane

It is recommended that the signal ground is a continuous, unsplitted plane. Under the SLIC device footprint and directly under the protection elements this plane might be omitted.

Note: The most important rule is to use a continuous, unslotted signal ground plane in the high-speed digital area.

Use at least one dedicated layer as a ground plane. This also improves signal integrity as no impedance changes for signal lines will occur.

All devices must be connected to one single GND. It is not recommended to split this into digital and analog grounds. If the GND plane is split for some other reason, it is important that the VINETIC®-2CPE/-1CPE's GND pins be connected to a large GND area, which itself is connected to GND by a low impedance path to GND, in order to avoid ground bouncing. Additionally no high-speed digital signals must cross this slot, as this increases EMI. The GND of the VINETIC®-2CPE/-1CPE's host controller interface must be connected as a large area to avoid ground bouncing.

4.1.4 Chassis Ground Plane

A chassis ground plane is used for EMC requirements and for protection purposes. Place this plane directly next to the signal ground plane to ensure an excellent capacitive coupling between both planes. An external chassis should be connected to the plane in multiple places.

The chassis ground plane extends from the board edges to the protection part of the SLICs. The complete board perimeter should be included in this chassis ground plane.

4.1.5 Avoiding Loop Antenna Effect

When laying out ground planes, it is vitally important to avoid loop antenna effects. A loop antenna could easily catch some unwanted noise and impair the complete system performance.

- Implement all ground planes as solid rectangular areas.
- Avoid creating loops with ground planes around other ground planes. The only exception is the chassis ground plane as it must run around the board perimeter.

By layout, ensure that the chassis ground loop is left at one point. The cut-out of the left gap must be large enough to avoid loop antenna effect.

4.2 VINETIC® Supply

The VINETIC®-2CPE/-1CPE chip requires two supply voltages: +3.3 V and +1.5 V. The +1.5 V supply voltage needs to be applied to the VINETIC®-2CPE/-1CPE before the +3.3 V supply is applied. A simultaneous ramp-up of the two VINETIC®-2CPE/-1CPE supply voltages is allowed. The tolerance of both supply voltages is ±5%.

The minimum capacitance value for blocking is 500 µF in sum at all power supply pins.

The following supply voltages are used to supply digital sections in the VINETIC®-2CPE/-1CPE:

- VDD33: Digital Supply I/O Pads (+3.3 V)
- VDD15: Power Supply digital parts (+1.5 V)

The following supply voltages are used to supply analog sections in the VINETIC®-2CPE/-1CPE:

- VDD33xx: Analog Supply Channel xx (+3.3 V)
- VDD15xx: Analog Supply Channel xx (+1.5 V)
- VDD33x: Analog Supply Channel x (+3.3 v)
- VDD15x: Analog Supply Channel x (+1.5 V)

The analog supply voltages must be kept separated and connected at a central point in the design. It is not required to locally generate the analog supply voltages for the VINETIC®-2CPE/-1CPE. The +3.3 V analog supply of the VINETIC®-2CPE/-1CPE can be connected to the +3.3 V digital supply via LC-filters or ferrite-beads (140 Ω@100 MHz, 0.55 ΩDC, 200 mA) or via 0 Ω-resistors, if possible.

The power supply pins of the PLL of the VINETIC®-2CPE/-1CPE are described in **Chapter 4.4.2** .

For the maximum power consumption of the VINETIC®-2CPE/-1CPE, see **[2]**.

4.3 SLIC Supply

4.3.1 SLIC-DC

The SLIC-DC device generates all the required high voltages from a single +9 V up to +40 V DC power supply. A 100 nF ceramic capacitor must be placed directly at the VS pin.

A good blocking of the supply voltage VS is required in order to maintain a minimum voltage of VS = 9 V for SLIC-DC V1.2 at all operating conditions. The highest power consumption appears during ring trip. In some cases, the fast ring trip feature of the VINETIC®-2CPE has to be used.

4.3.2 SLIC-E

The SLIC device requires up to four supply voltages : V_{DD}, V_{BATL}, V_{BATH} and V_{HR}. The SLIC-E offers the possibility to be operated at two different negative battery supply voltages and utilize an auxiliary positive supply for internal ringing.

The power rail V_{DD} can be +3.3 V or +5.0 V. The VDD supply of the SLIC-E is an analog supply voltage and must be separated from the digital supply on the board. This V_{DD} analog voltage must be connected to the analog power supply rail of the board. A 100 nF ceramic capacitor must be provided at the VDD pin.

If V_{BATL} is not used, the V_{BATL} pin of the SLIC must be connected to the V_{BATH} pin directly at the SLIC device.

If V_{HR} is used, the specified limits for the total supply voltage must not be exceeded.

To garantee the power up/down sequence, fast rectifier diodes (fast or ultra fast type) must be inserted between V_{BATL} and V_{BATH}. Please refer to **Chapter 4.4.3** and to the reference schematics for detailed information.

4.4 Supply Filtering

4.4.1 Decoupling of the VINETIC®-2CPE/-1CPE Supply Voltages

For the core supply pins (VDD15) of the VINETIC®-2CPE/-1CPE, four 100 nF ceramic capacitors and one large 470 µF ceramic capacitor are recommended.

For the digital interface supply pins (VDD33) of the VINETIC®-2CPE/-1CPE, four 100 nF ceramic capacitors and one large 47 µF ceramic capacitor are recommended.

For the analog +1.5 V supply pins (VDD15x, VDD15xx), a 100 nF decoupling capacitor is required on each supply pin (three capacitors). For the analog +3.3 V supply pins (VDD33x, VDD33xx), a 100 nF decoupling capacitor is required on each supply pin (two capacitors).

All blocking capacitors of the not used channel specific pins can be removed, when the VINETIC®-1CPE is used.

4.4.2 PLL Supply Voltage

Special treatment is required for the PLL supply voltage, as the PLL is sensitive to ripple peaks and to ground bouncing effects. The pins VDDP and GNDP must be connected with short lines directly to the planes. A blocking capacitor of 100 nF must be placed directly at the pins to filter high frequency power supply noise and the ground bouncing. For the value of the decoupling capacitor please refer to the VINETIC®-2CPE/-1CPE reference schematics.

4.4.3 Decoupling of the SLIC-E Supply Voltages

V_{BATH}, the substrate potential of SLIC-E, must always be the most negative pin. Otherwise, any other pin below V_{BATH} would possibly excite parasitic elements. As a consequence dangerous parasitic substrate currents can occur. The requirement V_{BATH} pin the most negative potential of the SLIC-E cannot be guaranteed in some situations (for example powering-up, overvoltages at the line). Thus the use of protection diodes in the power supply rails as shown in **Figure 22** and **Figure 23** is strongly recommended.

If a voltage on the Tip/Ring line appears that is more negative than the most negative SLIC supply voltage potential, the internal substrate diodes, which are normally reverse biased, start to conduct. If a decoupling capacitor is placed directly at the V_{BATH} pins of the SLIC device this capacitor is able to discharge through the SLIC onto the Tip/Ring line. The current flow from the capacitor through the SLIC towards the Tip/Ring line is uncontrolled. This situation is shown in **Figure 21**. Thus, do not place a decoupling capacitor directly on the SLIC battery power pins.

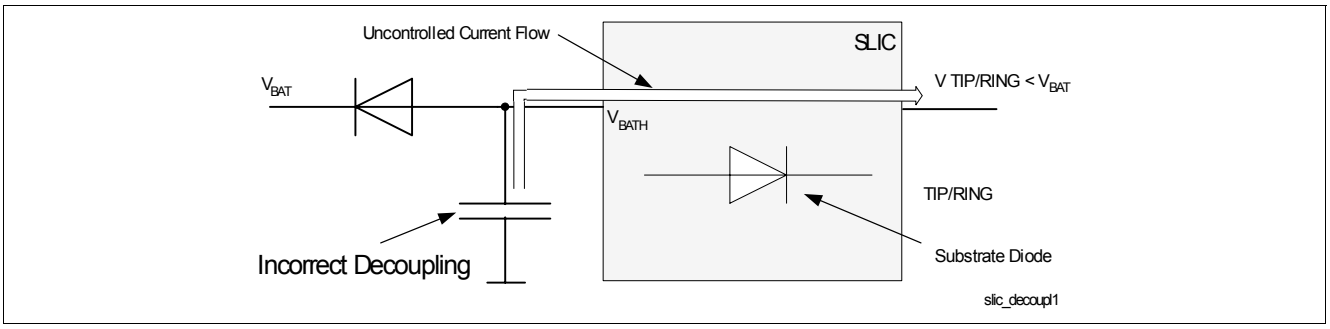


Figure 21 Incorrect SLIC Decoupling

Figure 22 and **Figure 23** show the correct SLIC decoupling. Fore more information please refer to the reference schematics in **Chapter 8**.

On DC/DC converters, large capacitors are placed on the output to reduce the switching noise. These large capacitors also should not be discharged into the SLIC. For this reason, series diodes are required between the power supply pins of the SLIC and the output of the DC/DC converters.

These external diodes must be provided for every single SLIC device.

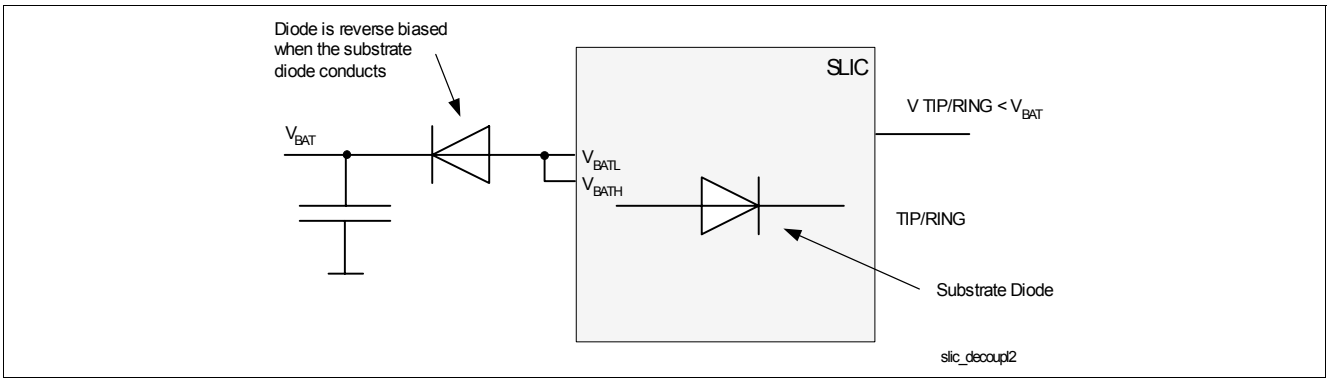


Figure 22 Correct SLIC Decoupling

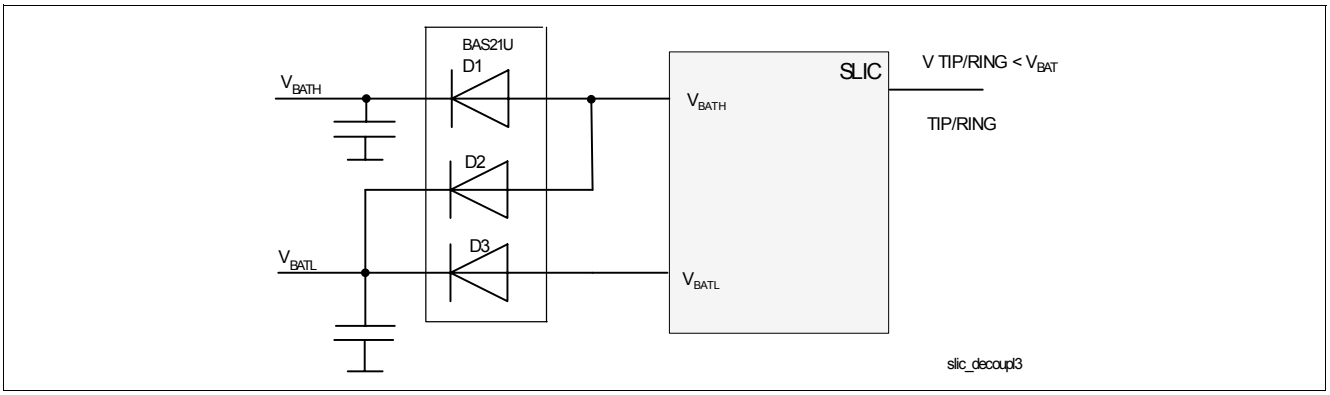


Figure 23 Correct SLIC Decoupling for two Battery Supplies

The diode D1 in the V_{BATH} power rail blocks any substrate current resulting from line potentials below V_{BATH}, whereas the other two diodes D2 and D3 (**Figure 23**) ensure that the SLIC pins is guaranteed the requirement $V_{BATL} > V_{BATH}$, regardless of the actual external supply voltage situation. Thus any critical behavior with respect to power-on sequence or missing supply voltages can be avoided. The SLIC power supply diodes must be fast or ultra fast types. The relevant diode parameter is the “reverse recovery time”. Diodes with reverse recovery times of less than 50 ns are suitable.

5 Layout Guide

This chapter serves as a guideline for the placing and routing processes during layouting. It gives an overview of recommended layer stacks and contains information about how to arrange components in order to guarantee a reliable operation of the system. Furthermore detailed information about the routing of signal paths in order to achieve best system performance is provided.

5.1 Layer Stack

It is very important to have a GND or other power layer underneath the surface layers (top and bottom).

It is good practice to have max. two adjacent signal layers[1)], which are then followed by a GND or power supply layer. For the top and bottom layers it is recommended to use only one signal layer which is followed by a GND or power supply layer.

The next picture shows the layer stack structure:

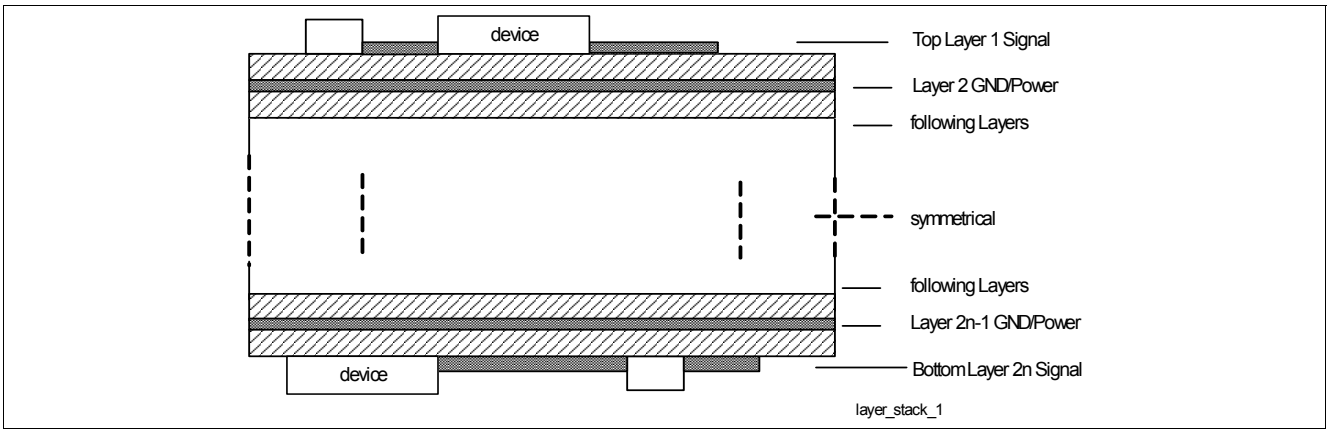


Figure 24 Layer Stack Setup

For TQFP-packages a 4-layer PCB is recommended, although a 2-layer board can be realized.

The number of layers has to be even and a symmetrical layer stack is recommended for reliable PCB production.

An example for a 4-layer stack:

- Signal/GND layer-1 at the component side
- GND
- Power
- Signal/GND layer-2 at the solder side

5.2 Layout Recommendations

In all figures of this chapter the analog channel specific decoupling capacitors are shown, whereas all decoupling capacitors for the digital power supplies are not shown.

5.2.1 Placement

The following placement hints are described with component references. These references are shown in the schematics in the Appendix.

- Place all components between SLIC and VINETIC® close to the VINETIC®.

1) If signal layers are adjacent it is strictly recommended to do routing in orthogonal directions, that means one signal layer has tracks mostly in x-directions, the other in y-direction. If parallel routing can not be avoided the distance has to be as far as possible.

- The VINETIC®-2CPE/-1CPE and SLIC have to be placed as close as possible to each other.
- Place decoupling capacitors as close as possible to the supply pin of the device package and associated ground pin.
- Place VINETIC® and SLIC device in such a way that tracks ACP, ACN, DCP, DCN, IT, ITAC are as short as possible.

The recommendations at the line side are:

- The analog components on the TIP/RING line of the SLIC should be placed close to the SLIC.
- The resistors R1_x, R3_x (R_{STAB}) and R2_x, R4_x (R_{PROT}) (shown in reference schematic in **Chapter 8**) should be placed close to the SLIC as possible.
- The capacitor C_{DCLP} (C17_x) need to be placed near the SLIC.
- The EMC capacitors C18_x, C19_x and C20_x need to be placed close to the SLIC pins as possible.

5.2.2 Routing

- One common ground layer, no separation between analog and digital grounds, is recommended.
- ACP/ACN tracks have to be routed in parallel and symmetrical with small distance; connections via holes should be avoided. A small area of ACP/ACN reduces EMI/EMR.
- ACP/ACN tracks need to be routed above a GND plane.
- DCP/DCN tracks have to be routed in parallel and symmetrical with small distance; connections via holes need to be avoided.
- The External Noise Filter capacitor in DCP/DCN (C17_x in **Figure 25**) is placed close to the SLIC with short traces.
- DCP/DCN tracks need to be routed and placed above a GND plane.
- Distances between the pair of ACN/ACP and the pair of DCN/DCP tracks have to be at least four times greater than the distance of ACN and ACP or DCN and DCP.
- The connection of GND, the battery voltages and all connections to the protection devices have to be low-impedance in order to avoid ground bouncing due to the high impulse currents in case of an overvoltage strike - wide tracks or planes are required. A width of at least 15 mil is recommended.
- No digital tracks have to cross or to be placed in parallel to the analog tracks between the VINETIC®-2CPE/-1CPE and the SLIC-DC. This includes especially the PCM interface signals and clock signals like FSC, PCL and MCLK. Further more host controller interfaces including the control signals are not to be routed through the analog section. It is recommended to route these tracks under the TQFP-package at an inner layer or at the bottom layer to avoid crosstalk to sensitive analog circuitry.
- For the FSC, PCL and MCLK signals an AC termination at the far end to ground is recommended at the VINETIC®-2CPE/-1CPE (receive side) to avoid ringing. The transmitter side recommends a serial termination.
- The connection from the GNDP pin of the VINETIC®-2CPE/-1CPE to the ferrite bead and to the GND plane must be as short as possible.

The recommendations at the line side are:

- Depending on the protection requirements, the track width from TIP/RING interface to the overvoltage protector must be chosen accordingly.In practice, a trace width of 16 mil is sufficient to meet the most surge requirements.
- The traces of the power supply rail V_S should be realized as planes. If planes are not possible, V_S needs wider traces (15 mil).

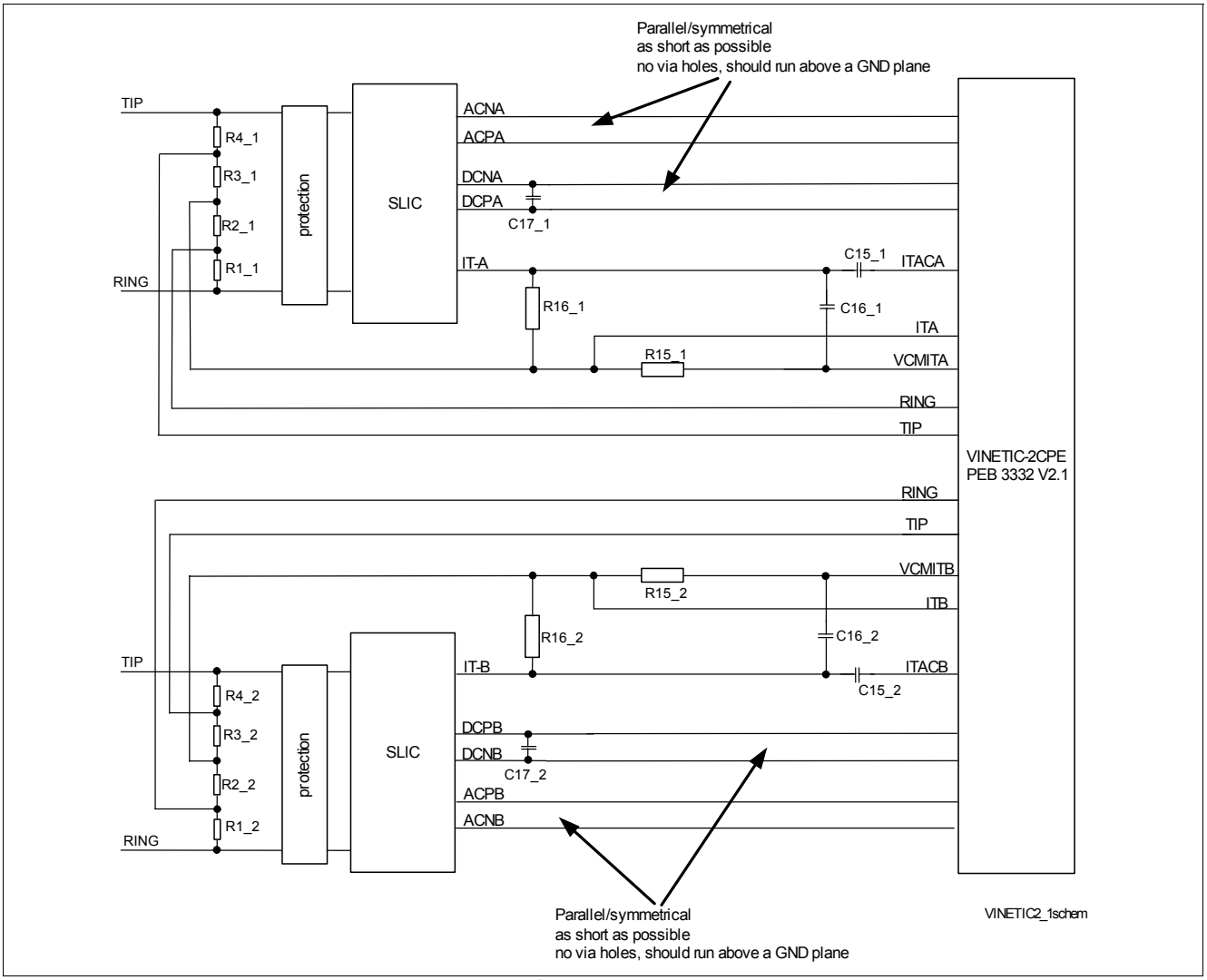


Figure 25 Connections between the VINETIC®-2CPE/-1CPE and the SLIC-DC with External Components

When only one channel of the VINETIC®-2CPE is to be used, the not used analog pins must be connected (VCMIT, IT, ITAC, RING and TIP).

In case of a VINETIC®-1CPE Version 2.1 (PEB 3331) is used the pins named ATEST must be connected together.

When a system is developed for one or two channels, the same layout can be used and no additional components may be needed. The board can be mounted differently to have the correct connection for a one channel solution. The same layout can be used, when no channel is used, or all ATEST pins must be connected together.

When the second channel is not used, the SLIC and some external components are not mounted. Other external components have to be modified. The mounting option and the values are shown in **Table 2**. The layout for both solutions is the same.

Table 2 Mounting Option for an unused Channel

Component	Value	
	2 Channel Solution	**1 Channel Solution (Channel B not used)**
C15_2	1 µF	0 Ω
C16_2	18 nF	Not mounted
C17_2	4.7 nF	Not mounted

Table 2 Mounting Option for an unused Channel (cont'd)

Component	Value	
	2 Channel Solution	**1 Channel Solution (Channel B not used)**
R15_2	499 Ω	0 Ω
R16_2	499 Ω	0 Ω
R1_2	1.5 MΩ	Not mounted
R2_2	3.3 kΩ	0 Ω
R3_2	3.3 kΩ	0 Ω
R4_2	1.5 MΩ	Not mounted

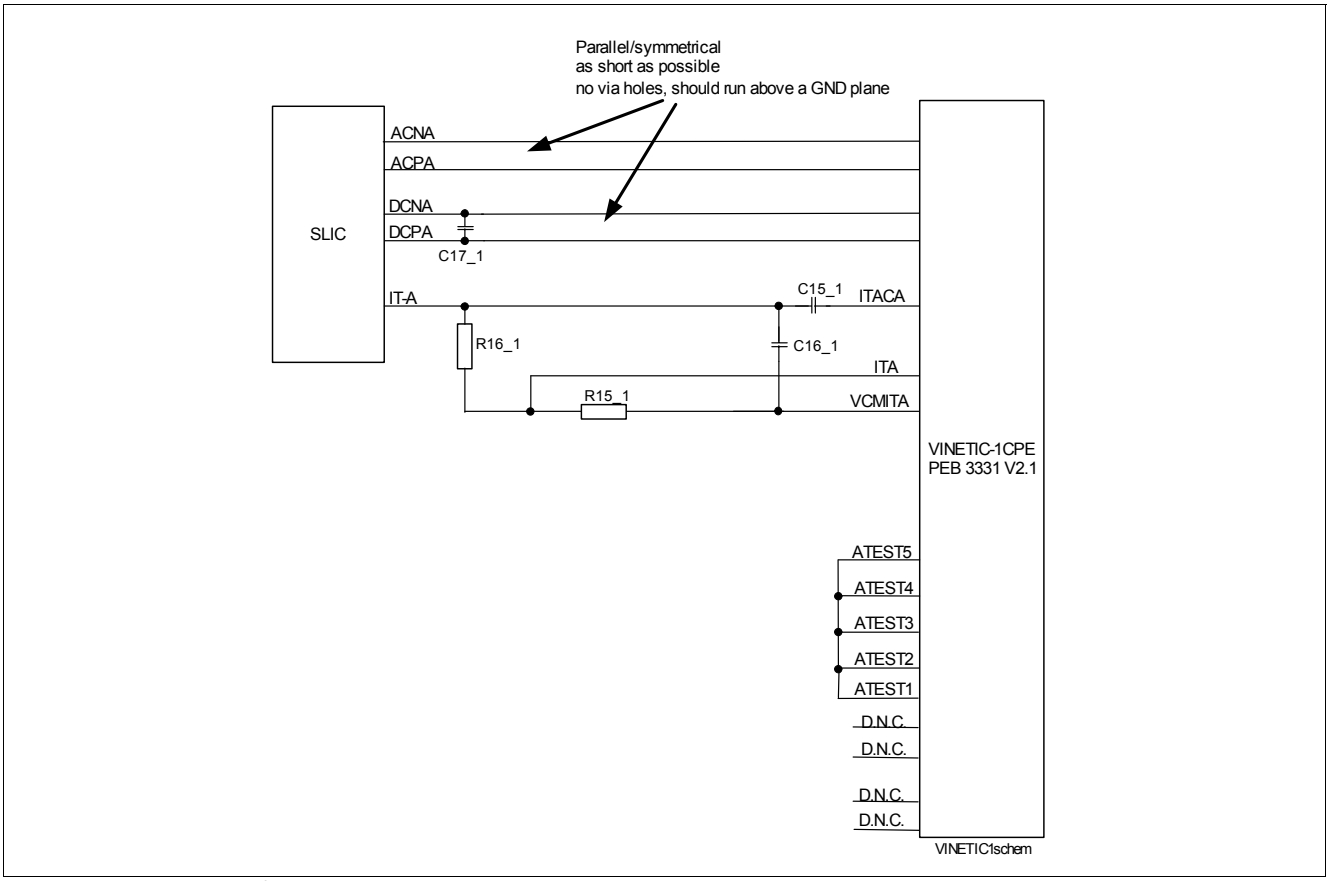


Figure 26 VINETIC®-1CPE Version 2.1 for one Channel

At the PEB 3331 the pins with the name ATEST must be connected together.

5.3 Layout Hints for the SLIC-DC

The SLIC-DC has a DC/DC converter as additional circuitry. This converter must be carefully handled in the layout. For the DC/DC converter layout the following rules have to be obeyed:

- The switching transistor needs a heat sink on the board. The heat sink must have an area of 100 mm^2.
- The value for the sense resistor R12_x in the reference schematics in **Chapter 8** depends on the ringing requirements of the application as well as on the switching coil used. For ringing requirements up to 5REN, a 0.15 Ω / 1W / 5% resistors is recommended. A value of 0.27 Ω / 0.5 W / 5% is recommended for applications with ringing loads up to 3REN ringing.

- The traces of the circuitry between SLIC-DC pin VN and the inductor (including the two 1 µF capacitors) must have a width of 15 mil.
- The two 1 µF capacitors at the V_N supply can be of types of X7R, but they must have a voltage rating of 100 V.
- The parts and the traces of the DC/DC part should not be placed near to the Tip and Ring lines, or should otherwise be routed in a separate layer.
- C_{DCLP} (C17_x) must be placed near to the SLIC-DC.

The decoupling capacitors are placed around the SLIC package at the component side. When the placement shown in **Figure 27** is used, the routing can be realized in the following way:

- The differential signals ACN/ACP and DCN/DCP are routed at the solder side.
- The digital host interface and the clock signals are routed at the component and solder side and far away from the analog signals.
- The control lines are routed at the component side (top side).
- The VS trace must be routed for each channel as a seperate trace and connected near the power supply at a blocking capacitor (star point).
- The analog ground must be routed for each channel as a seperate trace and connected near the power supply at a blocking capacitor (star point) of the board.
- The power supplies are placed in the two inner layers.

The pin SYNC of all SLIC-DC devices in the system can be connected via jumper (0 Ω resistors) to synchronize the DC/DC converters.

5.4 Layout Hints for the SLIC-E

The placement and the layout hints for the VINETIC®-2CPE/-1CPE and the SLIC-DC described in this document in **Chapter 5.2** and **Chapter 5.3** can be used for the SLIC-E as well, however, the layout hints for the DC/DC converter part are obsolete. Therefore, this chapter only describes the components placement of the power supplies V_{BATL}, V_{BATH} and V_{HR} and the layout hints for this part.

5.4.1 Placement of Power Supply Components

For the placement of the power supply components the following rules have to be obeyed:

- The triple diode package BAS21U has to be placed close to the SLIC-E.
- The decoupling capacitors of V_{BATL} and V_{BATH} have to be placed close to the diodes.
- The decoupling capacitor of V_{HR} has to be placed close to the SLIC-E pin V_{HR}.

5.4.2 Routing

The power supply must be routed in big traces or better in planes from the power supply to the diodes. The traces between the diodes and the pin of SLIC-E must be routed as wide as possible (e.g. width of 1mm). The voltages between the supplies V_{BATL} or V_{BATH} to V_{HR} can be about 100 V or above. The separation between V_{BATL} or V_{BATH} to V_{HR} must fulfill country specific requirements for clearance and creepage (e.g. UL 60950 **[11]**).

5.4.3 Cooling Area on PCB

The SLIC-E is available in PG-DSO-20 or PG-VQFN-48 package. In the package PG-VQFN-48 a cooling area is required on board. The layout for this package and the cooling area are specified in **[8]**.

5.5 Dual Layout with PEF 3322HL Version 1.4 and PEB 3332HT Version 2.1

The VINETIC®-2VIP (PEF 3322HL) Version 1.4 and the VINETIC®-2CPE/-1CPE (PEB 3332/-3331HT) Version 2.1 can be placed in one layout, to have the possibility to place one of both types on the board. The board

must have 6 layers, 2 layers for the power supply and 4 layers to connect the devices. All components are placed on the component side (Top side).

The layer stack is:

- Layer-1: digital/analog signals
- Layer-2: digital signals
- Layer-3: Ground
- Layer-4: Power supply
- Layer-5: analog signals
- Layer-6: analog signals

The layer-1 is used for analog and digital signals, however, the analog signals are only routed in the area between VINETIC®-2CPE/-1CPE and SLIC-DC.

Figure 27 shows a placement of a system with dual layout.

Figure 28 shows the layout. The layers have the following colours. The Ground and power plane are not shown as these layers are filled with copper.

- Layer-1: black (component side)
- Layer-2: blue
- Layer-3: Ground not shown
- Layer-4: Power Supply not shown
- Layer-5: green
- Layer-6: red (solder side)

In **Figure 27** and **Figure 28** the decoupling capacitors are not referenced. All other components have a reference. The references are identical to the reference schematic found in **Chapter 8**.

The power supply voltages of both devices VINETIC®-2VIP (PEF 3322HL) Version 1.4 and VINETIC®-2CPE (PEB 3332HT) Version 2.1 are different. The VINETIC®-2VIP (PEF 3322HL) Version 1.4 needs +1.8 V and +3.3 V. The VINETIC®-2CPE (PEB 3332HT) Version 2.1 needs +1.5 V and +3.3 V.

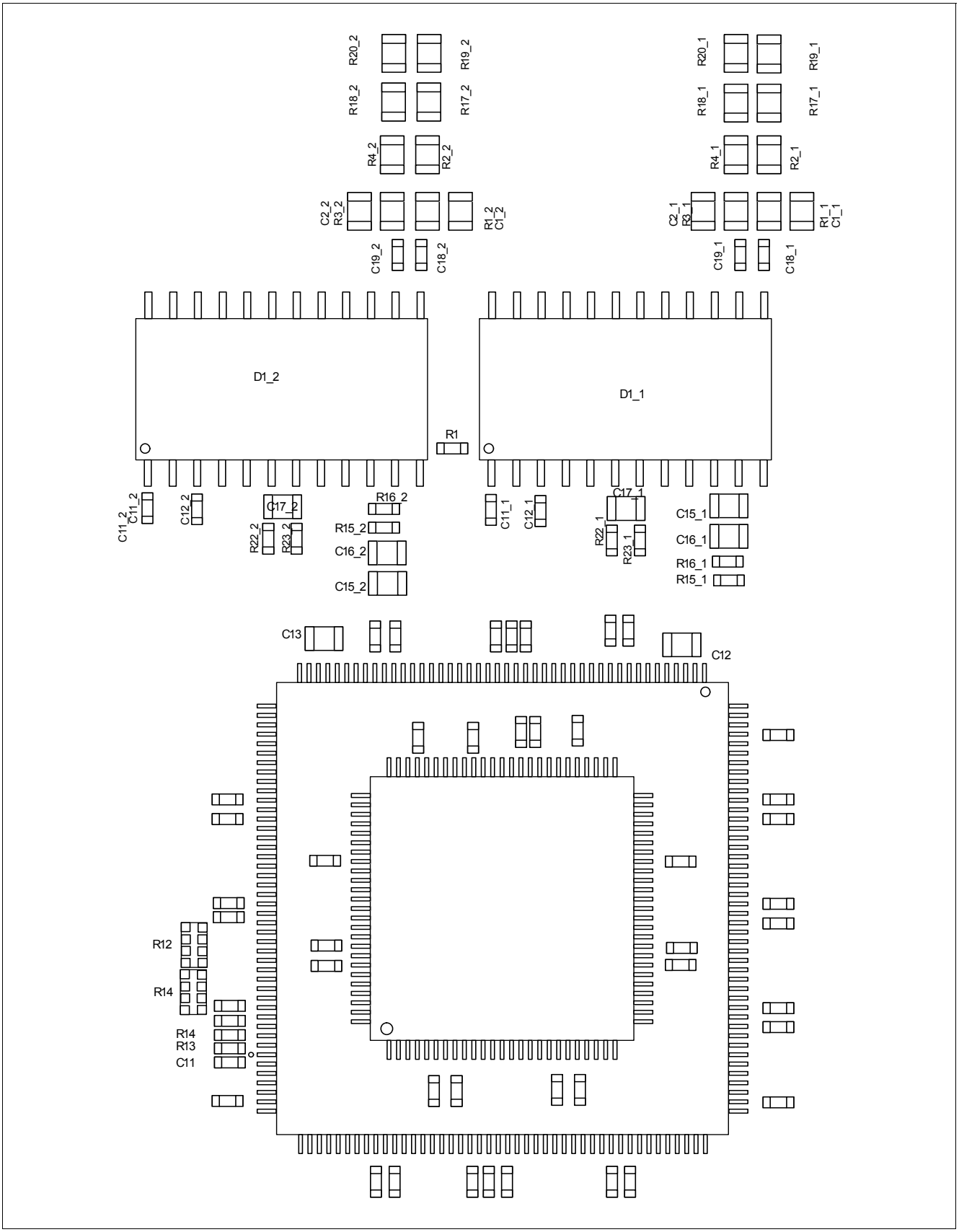


Figure 27 Placement of VINETIC®-2VIP, VINETIC®-2CPE and SLIC-DC with External Components

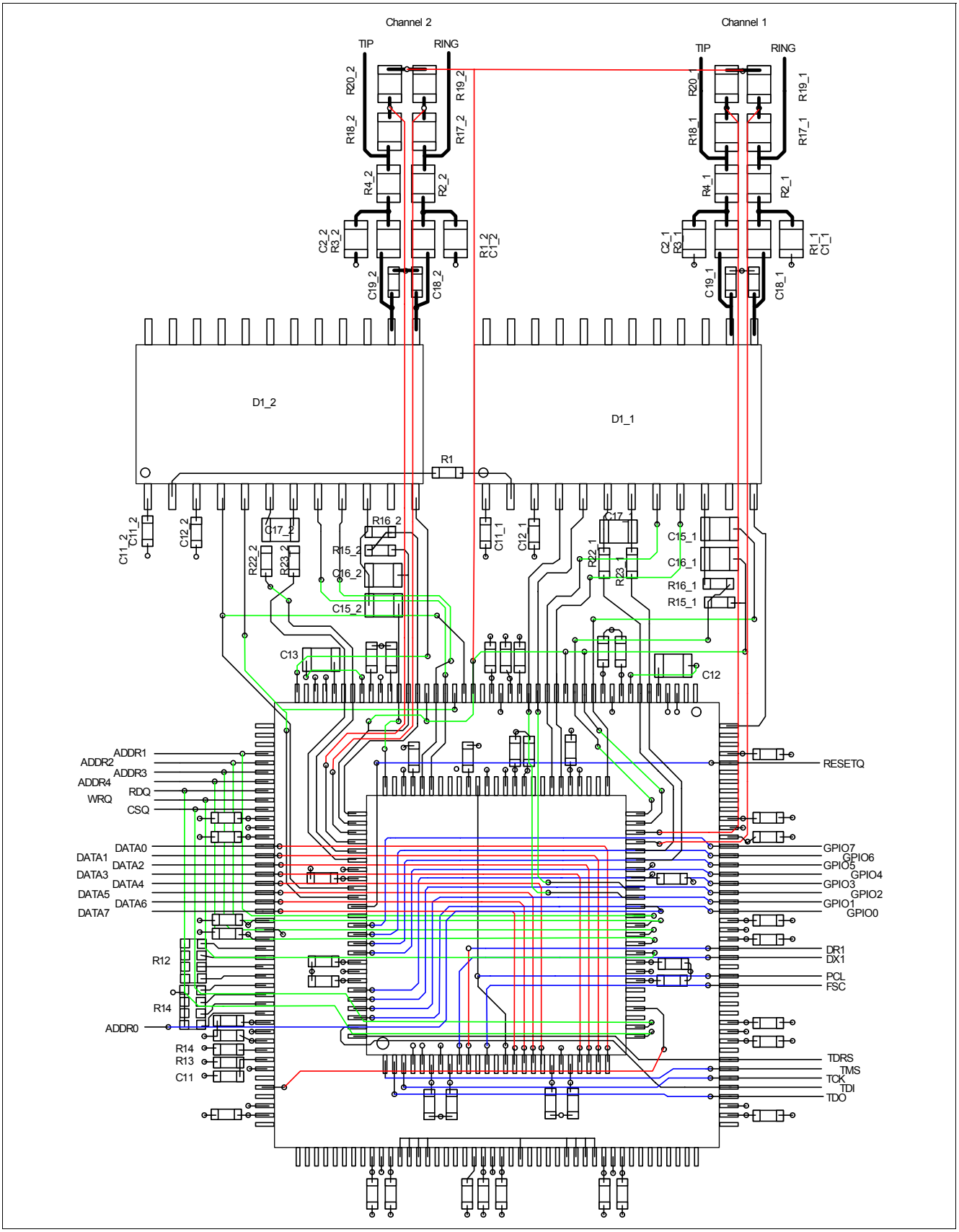


Figure 28 Layout Proposal of VINETIC®-2VIP, VINETIC®-2CPE and SLIC-DC with External Components

6 Transition Guide VINETIC®-2CPE Version 1.4 to Version 2.1

This chapter shows the minor hardware differences between both devices.

6.1 Packages

The VINETIC®-2CPE Version 2.1 is available in PG-TQFP-64-5/-8 and PG-TQFP-100-3/-18.

The VINETIC®-2CPE Version 1.4 is only available in a P-/PG-LBGA-144-1 package.

6.2 Power Supply

The VINETIC®-2CPE Version 2.1 needs two power supply rails of +1.5 V and +3.3 V. The power supplies needs no power-on sequence.

The VINETIC®-2CPE Version 1.4 needs two power supply rails of +1.8 V and +3.3 V. The power-on sequence is the following: the voltage +3.3 V must be applied earlier than the +1.8 V power rail voltage. A protection diode (BAS21) between +1.8 V to +3.3 V is recommended.

6.3 Host Interface

Both devices only have an 8-bit parallel host and the SPI interface. The differences are the selection of this interface and the used address and control lines.

6.3.1 Host Interface Selection

The VINETIC®-2CPE Version 2.1 has 2 pins to select the host interface mode IFSEL[1:0].

The VINETIC®-2CPE Version 1.4 has 3 interface selection pins IFSEL[2:0].

Table 3 Interface Selection Signals IFSEL

Mode	VINETIC®-2CPE Version 1.4			VINETIC®-2CPE Version 2.1	
	IFSEL2	IFSEL1	IFSEL0	IFSEL1	IFSEL0
SPI	0	0	1	1	1
8-Bit Intel demultiplexed	0	1	1	0	1
8-Bit Intel multiplexed	Not supported			0	0
8-Bit Motorola	1	0	0	1	0

6.3.2 Address Lines of the Host Interface

The address lines in the Intel demultiplexed mode and in Motorola mode are not identical. The VINETIC®-2CPE Version 2.1 has the A0 address line available. The number of address lines vary in every mode.

6.3.2.1 SPI Mode

The differences are:

- The first byte transferred to the VINETIC® at every new access must be an address field.
- The VINETIC®-2CPE Version 2.1 supports simultaneous read/write access and the protocol is changed.

There are more differences between both packages of the VINETIC®-2CPE Version 2.1, please refer to **Chapter 2.1.1**.

6.3.3 Intel Demultiplexed Mode

The VINETIC®-2CPE Version 2.1 has 5 address lines A[4..0] instead of 4 address lines A[4..1] for the VINETIC®-2CPE Version 1.4. The timing can be identical, but the new version Version 2.1 has a reduced cycle time of 20%.

The address lines are latched when the chip select line is low and the RDQ or WRQ goes low. The CSQ and the RDQ (Read sequence) or WRQ (write sequence) are ored. When both signals are low the falling edge of the generated internal signal activates the address latch. Therefore, the additional circuitry described in **Chapter 2.2** can be removed.

6.3.4 Intel Mulitplexed Mode

This mode is implemented in the VINETIC®-2CPE Version 2.1. The VINETIC®-2CPE Version 1.4 does not have this mode. The little or big endian mode can be set by the software. The default mode after reset is the little endian mode.

6.4 Motorola Mode

This mode is implemented in the VINETIC®-2CPE Version 2.1, with more address lines than the VINETIC®-2CPE Version 1.4. The device needs 6 address lines (A[5..0]) instead of 4 address lines (A[4..1]) with VINETIC®-2CPE Version 1.4. The little or big endian mode can be set by software. The defaultmode is the big endian mode.

6.5 Additional Differences in all Host Interface Modes

6.5.1 Interrupt Line

The polarity of the interrupt is programmable in the VINETIC®-2CPE Version 2.1. After a reset the polarity of the interrupt line is low active. The interrupts can be disabled by one chip access.

The VINETIC®-2CPE Version 1.4 has a fixed polarity with low active interrupt line.

6.5.2 GPIO Signals

The VINETIC®-2CPE Version 2.1 in the package PG-TQFP-100 has 8 GPIOs (GPIO[7:0]). These IOs are not channel specific. The VINETIC®-2CPE Version 2.1 in the package PG-TQFP-64 has no GPIOs.

The VINETIC®-2CPE Version 1.4 has 8 channel specific GPIOs (GPOIO[7:0]).

6.5.3 RDYQ Signal

The VINETIC®-2CPE Version 2.1 has an open drain output. This signal can be used to directly connect the signal to the transfer acknowledge signal TAQ of the Motorola prozessor. A pull-up resistor of 1.2 kΩ up to 3.3 kΩ is recommended.

The VINETIC®-2CPE Version 1.4 has an open source output. A pull-down resistor of 560 Ω is recommended.

When the signal is not used, the output can be left open at both devices.

6.6 Analog Interfaces

6.6.1 Digital/Analog IO Signals and SLIC Control

The VINETIC®-2CPE Version 2.1 has no digital/analog IO pins. For line testing there are the two input pins TIPx and RINGx. Both inputs are available for both channels. To control the SLIC-DC devices each channel of the VINETIC®-2CPE Version 2.1 has two control signals C1x and C2x. The SLIC-DC input pin C3 must be connected to GND.

The VINETIC®-2CPE Version 1.4 has 5 IO pins (IO[4:0]) for every channel and two control pins to control the SLIC-DC. The SLIC-DC input pin (C3) must be connected to GND.

6.6.2 Analog Signals

There are some slight differences in external components between VINETIC®-2CPE Version 2.1 and Version 1.4.

6.6.2.1 AC/DC Loop Signals

The ACP/ACN lines have no difference.

The DCP/DCN lines are different for both devices. The external DC low pass filter has different values (see **Figure 29**). The VINETIC®-2CPE Version 2.1 needs a capacitor of 100 nF at the SLIC-DC input pins DCP and DCN.

The VINETIC®-2CPE Version 1.4 needs a low pass filter with 2 resistors of 33 Ω and a capacitor of 4.7 µF.

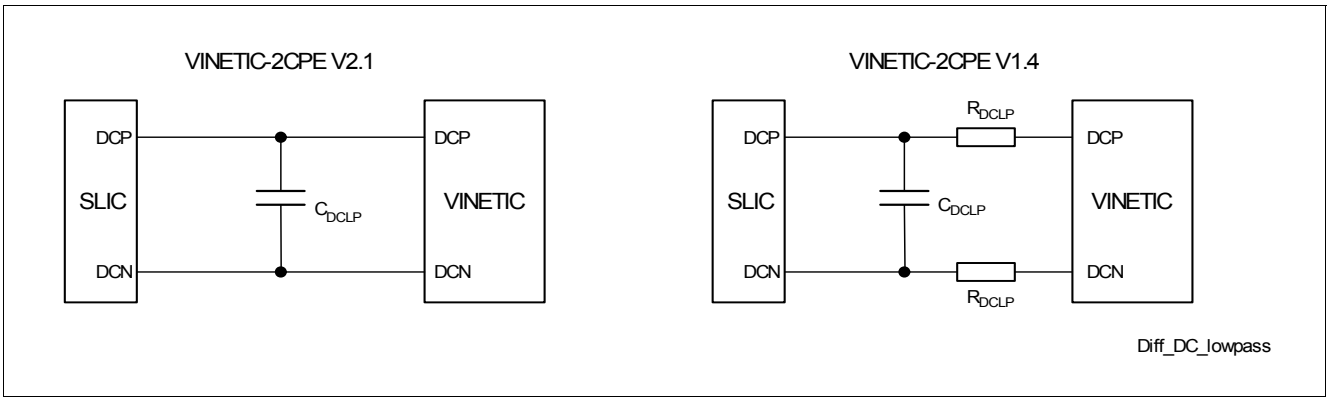


Figure 29 Differences in the DC Low Pass Filter

Table 4 Different Component Values in the DC Low Pass Filter

Component	VINETIC®-2CPE Version 2.1	VINETIC®-2CPE Version 1.4
R_{DCLP}	Not used	33 Ω/0.065 W
C_{DCLP}	100 nF/6.3 V/10 %	4.7 µF/6.3 V/10 %

6.6.2.2 Network between VINETIC®-2CPE and SLIC-DC

The network at ITAC, IT, VCMIT and IL is different between the two versions. The pin IL is not available with VINETIC®-2CPE Version 2.1. Therefore, the resistor R_{IL} is not used and removed.

Note: The SLIC-DC Version 1.2 does not provide the longitudinal current pin IL.

The differences between both networks are shown in **Figure 30**.

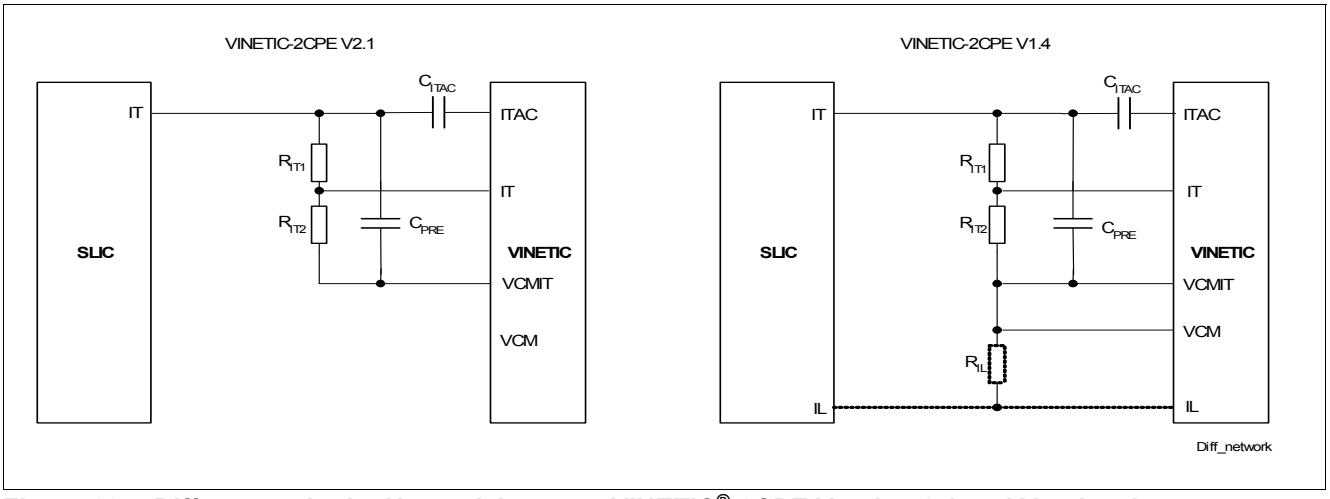


Figure 30 Differences in the Network between VINETIC®-2CPE Version 2.1 and Version 1.4

Table 5 Different Component Values in the Analog Network

Component	VINETIC®-2CPE Version 2.1	VINETIC®-2CPE Version 1.4
C_{ITAC}	1 µF/10 V/10 %	1 µF/10 V/10 %
R_{IT1}	499 Ω/0.065 W/1 %	510 Ω/0.065 W/1 %
R_{IT2}	499 Ω/0.065 W/1 %	680 Ω/0.065 W/1 %
R_{IL}	Not used	1.6 kΩ/0.065 W/1 %
C_{PRE}	4.7 nF/10 V/5 %	18 nF/10 V/5 %

The VINETIC®-2CPE Version 2.1 no longer has the signal VCMAB. Instead of VCMAB the line testing resistors must be connected to VCMITx. Due to lower core voltage of the VINETIC®-2CPE Version 2.1, the values of the line testing resistor dividers are different (see **Figure 31**).

6.6.3 Line Testing Resistors

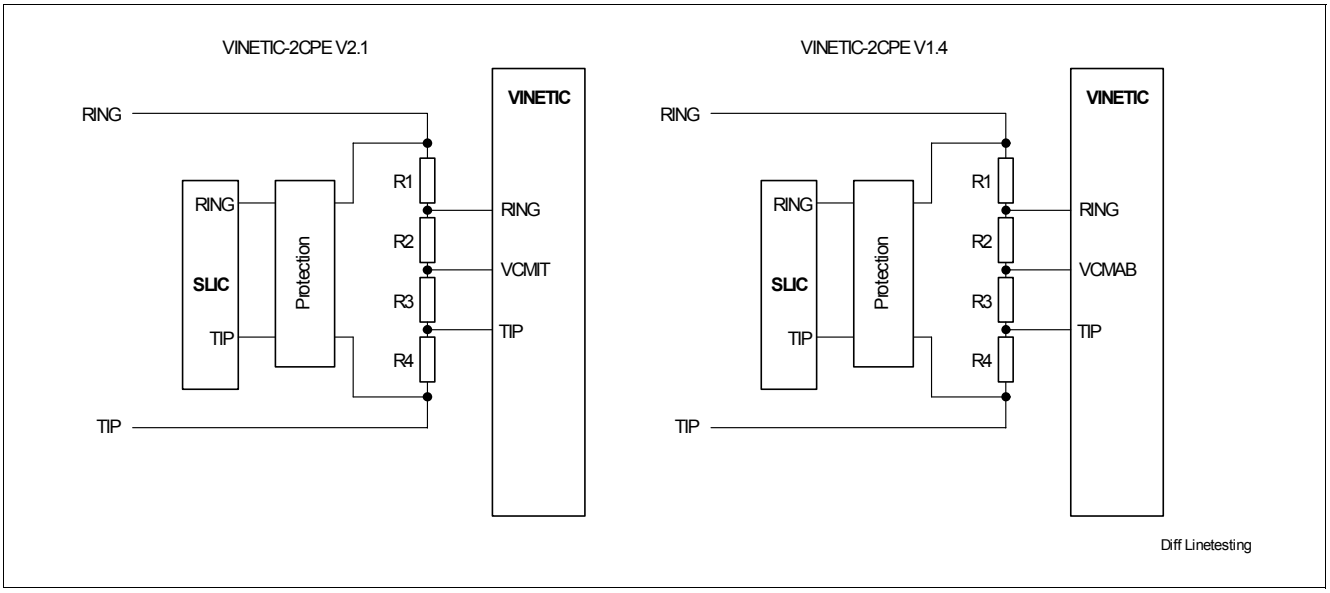


Figure 31 Different Line Testing Resistor Values

Table 6 Different Line Testing Resistors

Component	VINETIC®-2CPE Version 2.1	VINETIC®-2CPE Version 1.4
R1	1.5 MΩ/200 V/0.25 W/1 %	10 MΩ/200V/0.25 W/1 %
R2	3.3 kΩ/200 V/0.25 W/1 %	47 kΩ/200 V/0.25 W/1 %
R3	3.3 kΩ/200 V/0.25 W/1 %	47 kΩ/200 V/0.25 W/1 %
R4	1.5 MΩ/200 V/0.25 W/1 %	10 MΩ/200 V/0.25 W/1 %

7 Summary and Design Checklist

This chapter is divided into 2 parts: the guidelines for the schematic and the guidelines for the layout.

7.1 Schematic Guidelines

7.1.1 Power Supply

- Are the power supply tolerances for the VINETIC®-2CPE/-1CPE and the SLICs met? (**Chapter 4.2** and **Chapter 4.3**)
- Are the ripple requirements for the VINETIC®-2CPE/-1CPE and the SLICs met? (**[2]**)
- Is the load regulation of the power supplies for the VINETIC®-2CPE/-1CPE and the SLICs sufficient? (**Chapter 4.2** and **Chapter 4.3**)
- Are power-on/power-down sequences taken into account? (**Chapter 6.2**)

7.1.2 VINETIC® Section

- Is the host controller interface selection for VINETIC®-2CPE/-1CPE correct (IFSEL[1:0] pin setup)? (**Chapter 2.1**)
- Are the clocks FSC, PCL and MCLK stable before the reset is switched inactive? (**Chapter 2.5**)
- Is the bus width and the bus orientation (8-bit bus) done correctly (address shift)? (**Chapter 2.1**)
- Are all differential interfaces from the VINETIC®-2CPE/-1CPE to the SLIC connected with the right polarity (positive and negative)? (**Chapter 6.6.2.1**)
- Are unused pins on the VINETIC®-2CPE/-1CPE treated correctly?
- Are all required clocks provided (PCL, FSC and MCLK are required for the VINETIC®-2CPE/-1CPE)? (**Chapter 2.5**)
- Is the phase relationship of FSC and PCL correct? (**Chapter 2.5**)
- Is the pull-up resistor on the RDYQ pin provided? (**Chapter 2.1**)
- Is the pull-up resistor on the interrupt pin of the VINETIC®-2CPE/-1CPE provided? (**Chapter 2.1**)
- Is the TC1Q connected to pull-ups, when used? (**Chapter 2.6**)
- Is the JTAG interface correctly connected? (**Chapter 2.7**)
- Is the decoupling on the VINETIC®-2CPE/-1CPE correct (value of capacitors, type of capacitors)? (**Chapter 4.2**)
- Is the PLL supply (GND + power) separated from the supply of the other components? (**Chapter 4.4.2**)
- Are the voltage dividers for “foreign voltage measurement” dimensioned correctly for your application? (**Chapter 3.4** and **Chapter 6.6.3**)
- Are the correct capacitors used (tolerance, voltage rating, material, package size)?
- Are the correct resistors used (tolerance, power rating, pulse power rating)?

7.1.3 SLIC Section

- Is the decoupling on the SLIC correct (capacitors value, type of capacitors)?
- Are the correct capacitors for the target application used (tolerance, voltage rating, material, package size)?

- Do the protection devices fit to protection requirements? ([9])
- Are the correct resistors for the target application used in the network between SLIC and VINETIC®-2CPE/-1CPE and at the telephone line (tolerance, power rating, pulse power rating)? (Chapter 6.6.2.2)?
- Is the heat dissipation area (PG-DSO-36 and PG-VQFN-48) electrically isolated from the power supplies?

Note: Protection tests should be performed at an early development state in order to figure out that the protection circuit is suitable for the application. This Hardware Design Guide has no focus on overvoltage protection issues. Please refer to the appropriate document [9].

7.2 Layout Guidelines

The layout guide supports all designs with the Infineon VINETIC® Chip Set Family including the SLIC-DC.

This layout guide serves as a guideline for the placing and routing process during layout. The layout guide also includes also a checklist for the most important placement and layout rules. It also provides an overview of layer stack setup options and important thermal considerations.

7.2.1 Placement, Layer Stack up, and the Routing Rules

The Placement, Layer Stack up, and the routing rules are described in an Application Note “Layout Recommendation”, please refer to this document for more details.

7.2.2 Summary and Checklist Layout

7.2.2.1 General Points

- Are all thermal requirements met? (Chapter 5.4.3)
- Are thermal vias provided on all devices? (Chapter 5.3)
- Are enough layers connected to the thermal vias? (Chapter 5.3)
- Is the layer stack symmetrical (to avoid mechanical problems and improve impedance characteristics)? (Chapter 5.1)

7.2.2.2 Digital Section and Signals

- Place VINETIC®-2CPE/-1CPE and SLIC so that the digital signals do not cross the analog signals! (Chapter 4.1.1)
- Separate all analog circuitry from any digital signal source, especially crystals, clock sources, and FSC signal! (Chapter 4.1.1)
- Use series resistors in data lines as needed to reduce reflections. Place these close to the related output!
- Avoid routing digital traces adjacent (or crossing) to analog traces! (Chapter 4.1.1)

7.2.2.3 Analog Sections and Signals

- Place the VINETIC®-2CPE/-1CPE and SLIC-DC and/or SLIC-E so that the interface between the two devices is straight-forward. Try to maintain close distances between the VINETIC®-2CPE/-1CPE and the SLIC! (Chapter 5.2.1)
- Use differential pair rules on DCP and DCN. Route these signals over GND planes, if possible! (Chapter 5.2.1)

- Place line side passive components (R_{STAB} and C_{STAB}) close to the SLIC!(**Chapter 5.2.1**)
- Place EMC capacitors close to the SLIC-DC! (**Chapter 5.2.1**)
- Route ACP and ACN symmetrically, with short distances over ground planes! (**Chapter 5.2.1**)
- Use 8 mil traces for all analog signals for all traces from the SLIC-DC/-E to the VINETIC®-2CPE/-1CPE!
- Use minimum of 16 mils as the trace width for routing from the line to the line feed resistor (including traces to primary protection components). (recommended for ITU-T K.45 enhanced level!)
- Keep a minimum distance of 18 mils between the Tip/Ring traces, to prevent arcing during lightning induced surge events!
- Keep a minimum spacing between differential pairs that is four times the distance between the single traces of the differential pair!

8 Appendix

Several reference schematics are available for the VINETIC®-2CPE and SLIC-DC. In this chapter an exerpt is shown of these schematics. All of them are available as PDF-files with a Bill of Material. The major changes are the external components to support different ringer loads and the voltage of the power supply V_S of the SLIC-DC. The differences are described in details in **Table 7**.

Figure 32 and **Figure 33** describe how do connect the VINETIC®-2CPE to the SPC/SPI interface.

Figure 34 up to **Figure 37** show the different external circuitry for different ringer loads and power supply voltage.

Figure 38 up to **Figure 42** show the “Dual Layout” with VINETIC®-2CPE V2.1 and VINETIC®-2VIP V1.4.

Figure 43 shows the external circuitry for SLIC-E.

Table 7 Ringer Load and Power Supply Voltage versus External Circuitry

Ringer load	Power Supply VS	Modification to Standard EU
3 REN	+12 V no EMV	L2_x is removed
3 REN	+12 V with EMV	Standard EU
5 REN	+12 V with EMV	R10_, R12_, V1_x and L1_x are modified and R9_x is removed
5 REN	+9 V	R10_, R12_, R13_x, V1_x,T1_x and L1_x are modified and R9_x, C8_x are removed

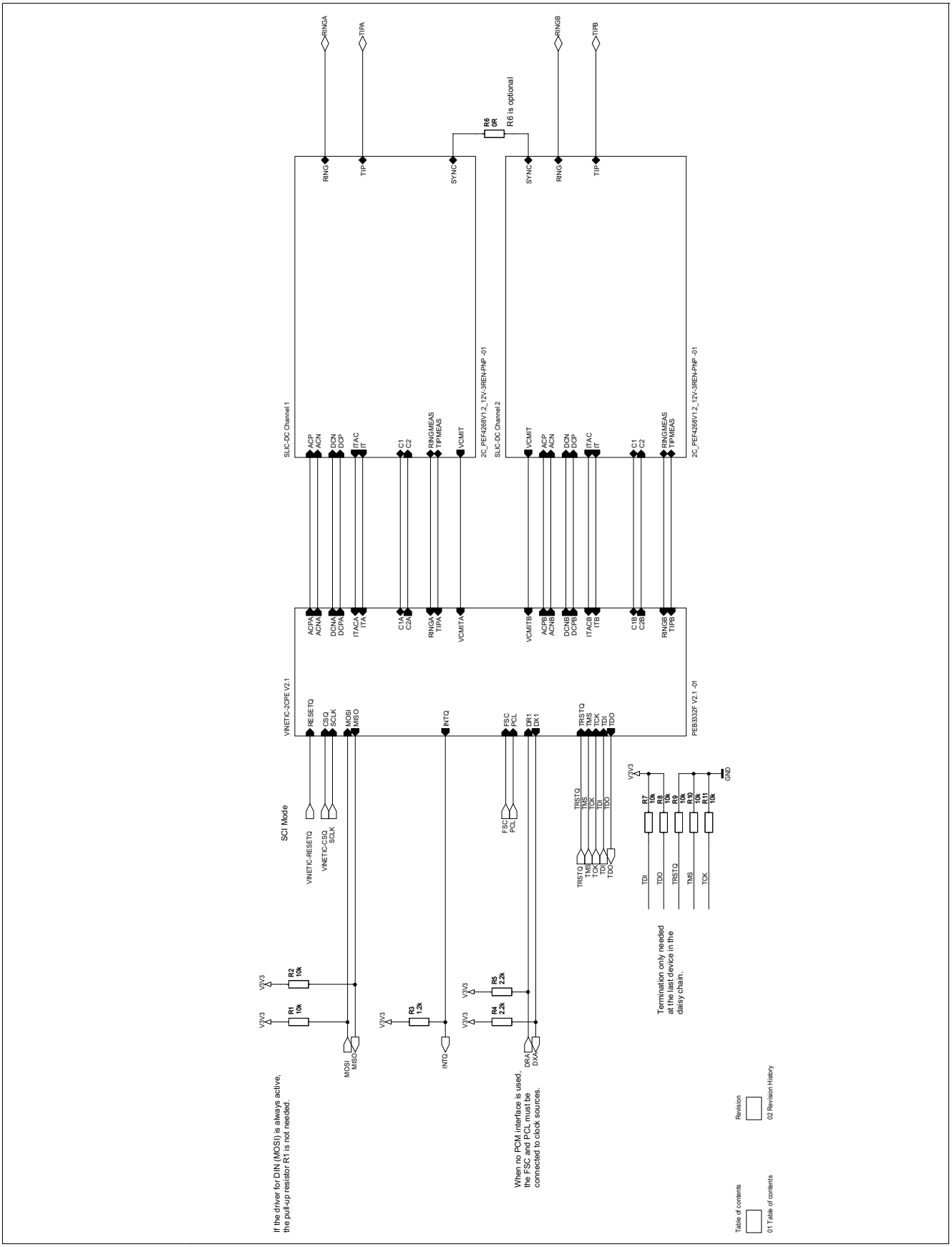


Figure 32 VINETIC®-2CPE Version 2.1, SLIC-DC Version 2.1 (Top Sheet)

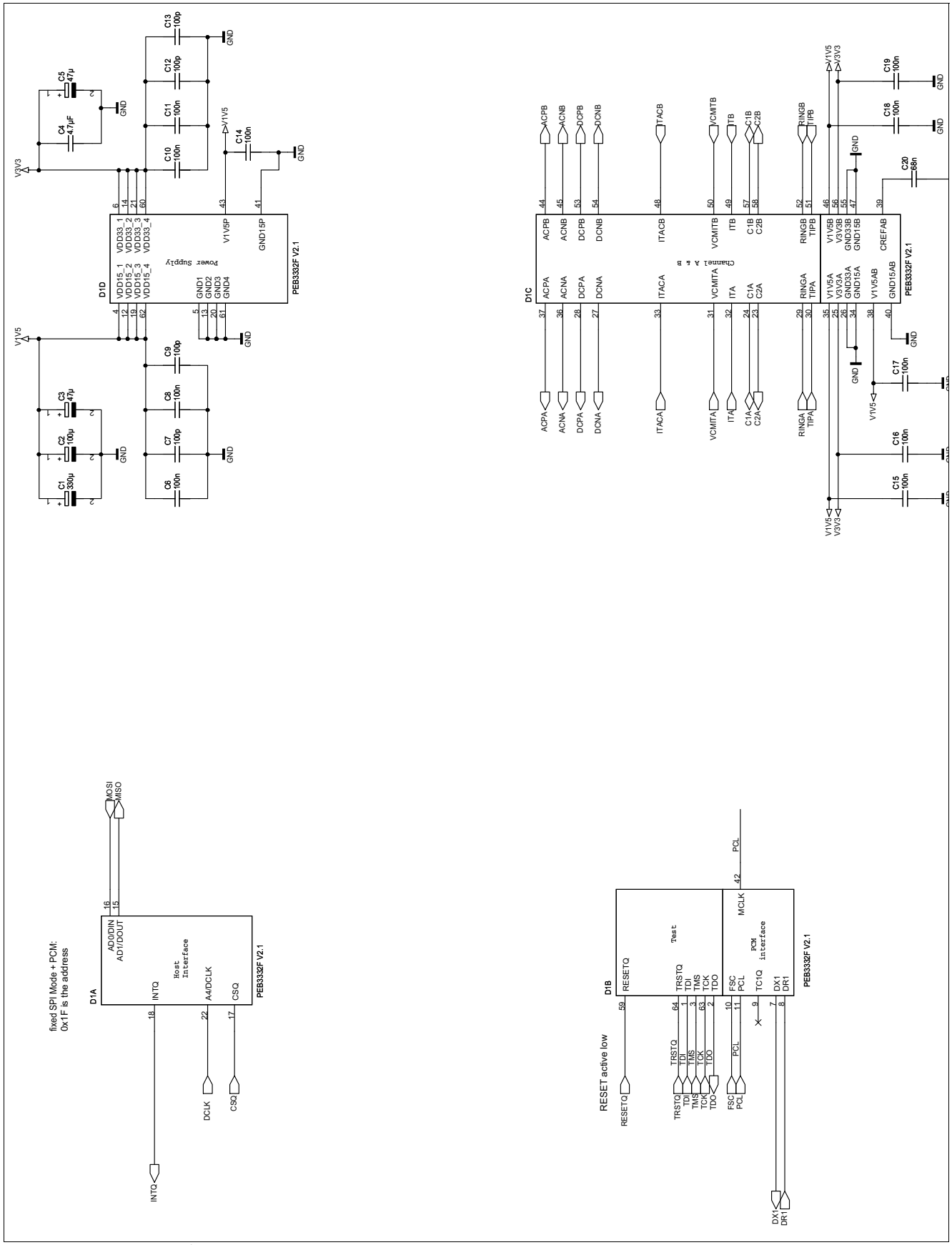


Figure 33 VINETIC®-2CPE Version 2.1 in SCI/SPI Mode

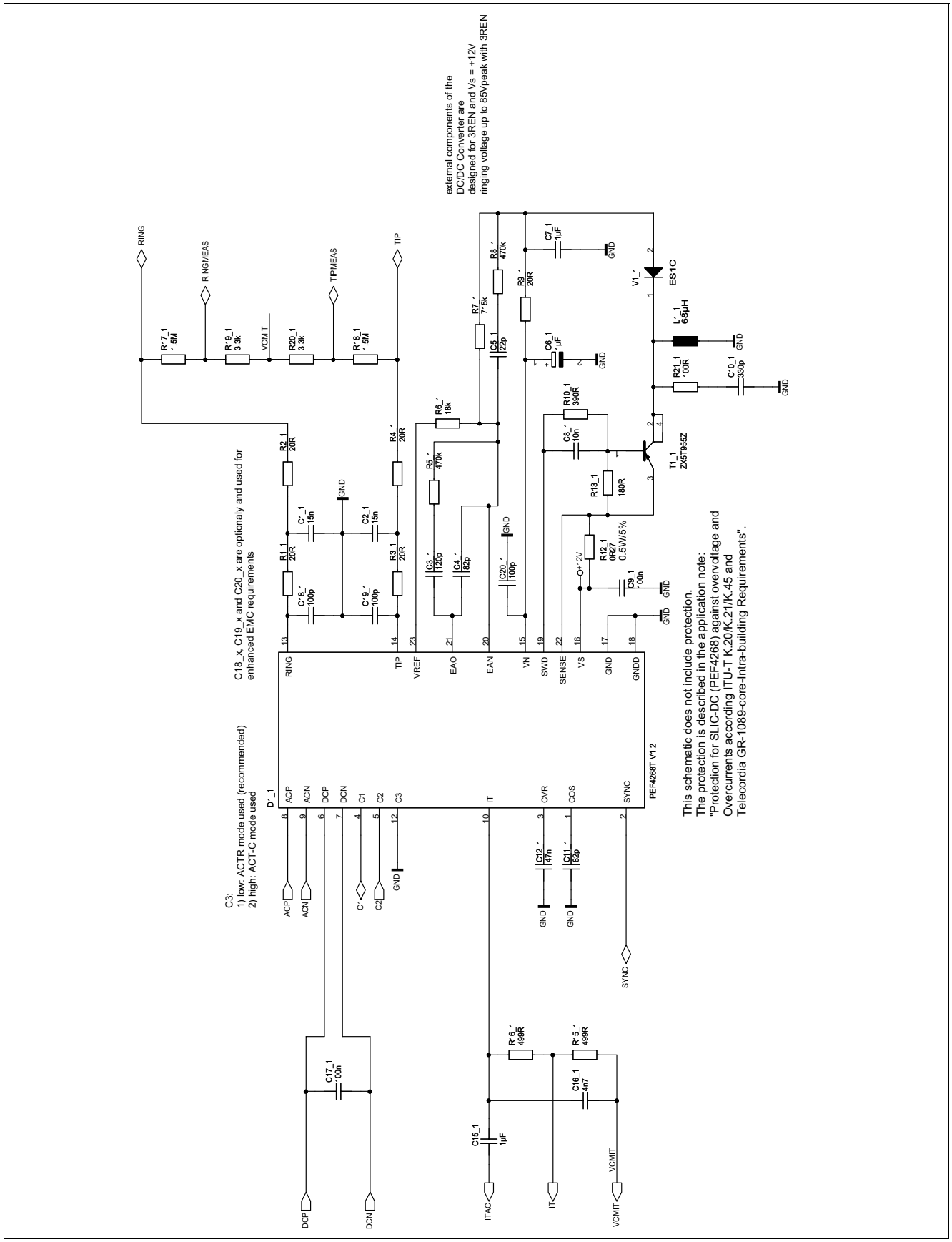


Figure 34 SLIC-DC Version 1.2 for 3 REN and +12 V Power Supply (Low Cost)

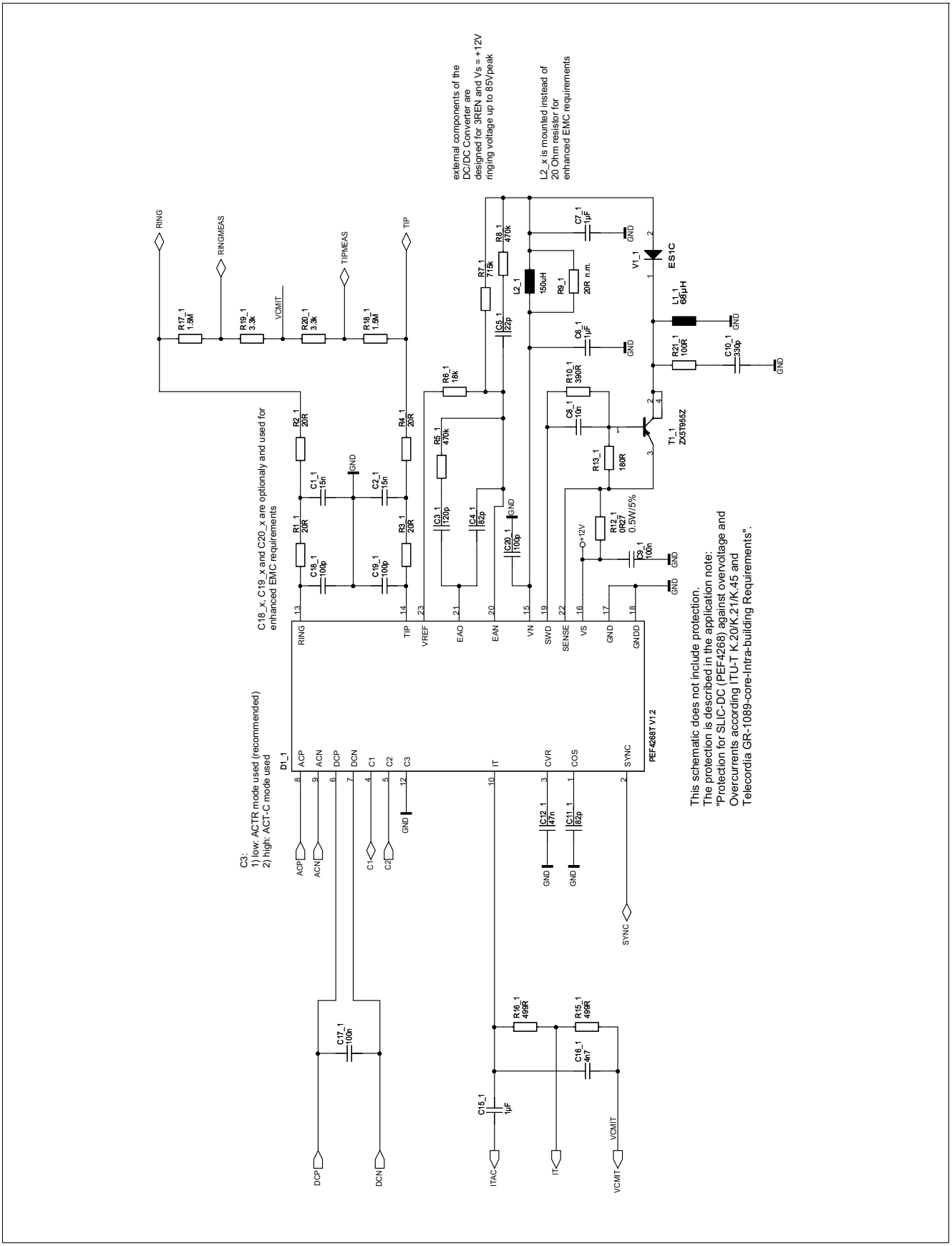


Figure 35 SLIC-DC Version 1.2 for 3 REN and +12 V Power Supply (Standard EU Market)

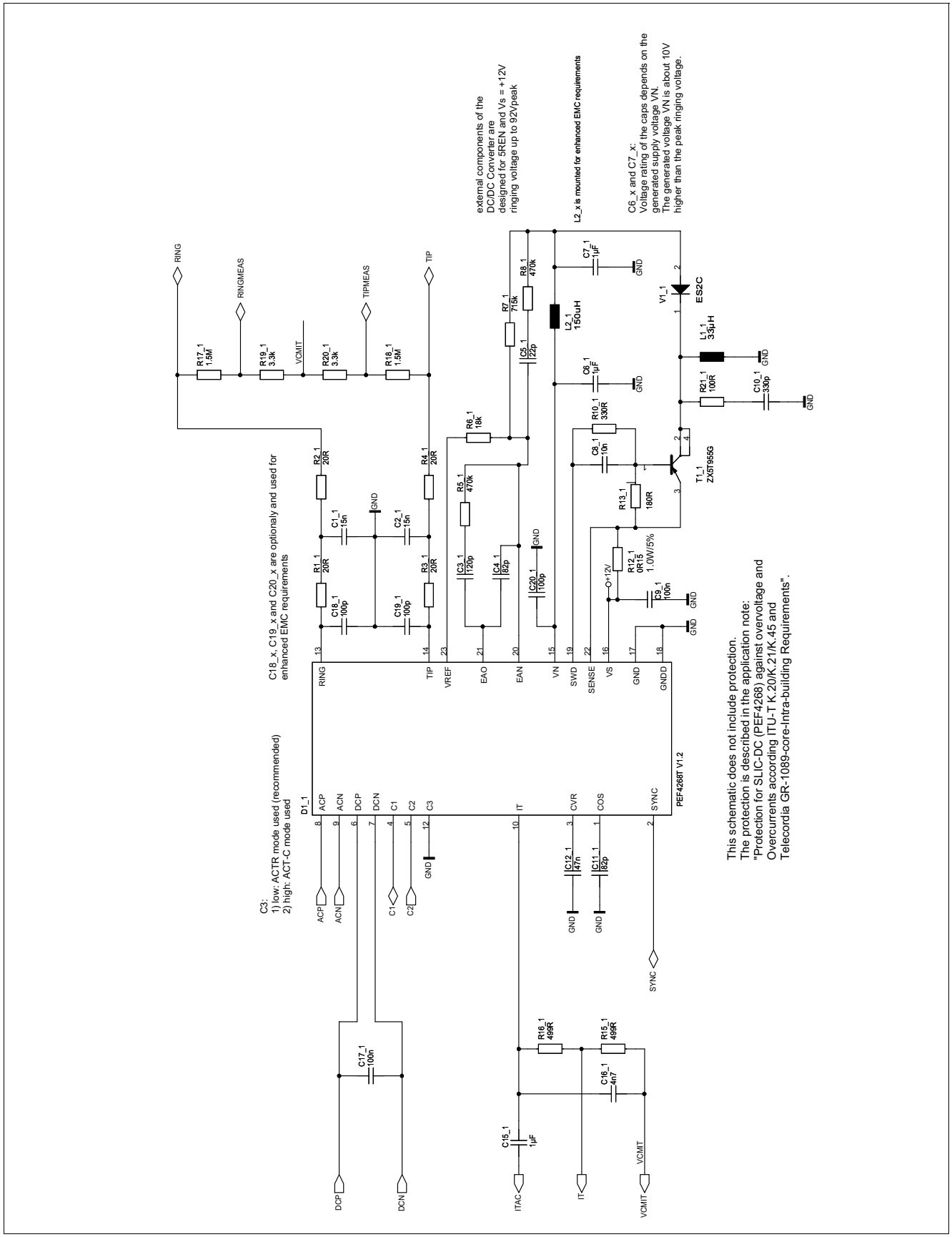


Figure 36 SLIC-DC Version 1.2 for 5 REN and +12 V Power Supply

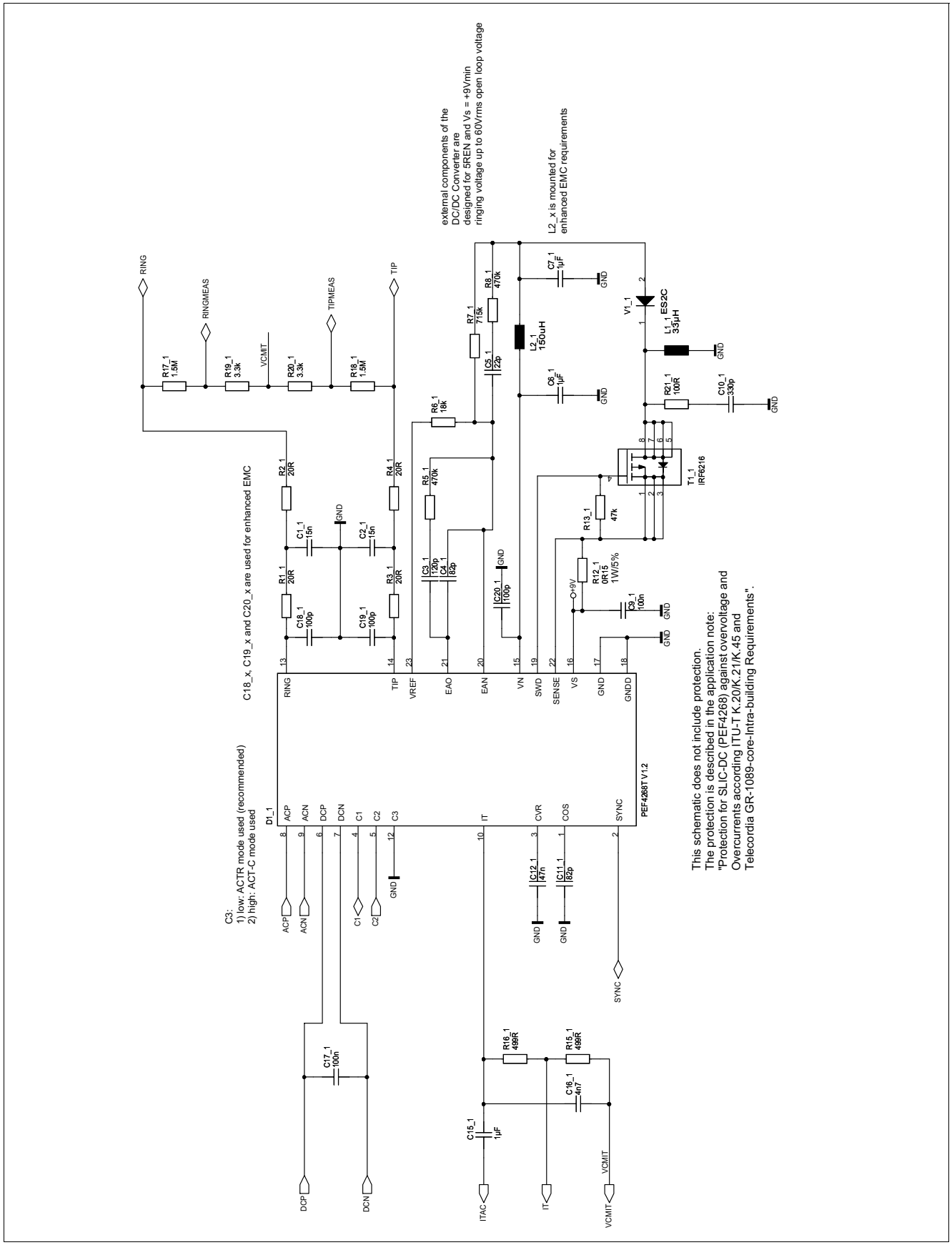


Figure 37 SLIC-DC for 5 REN and +9 Vmin Power Supply

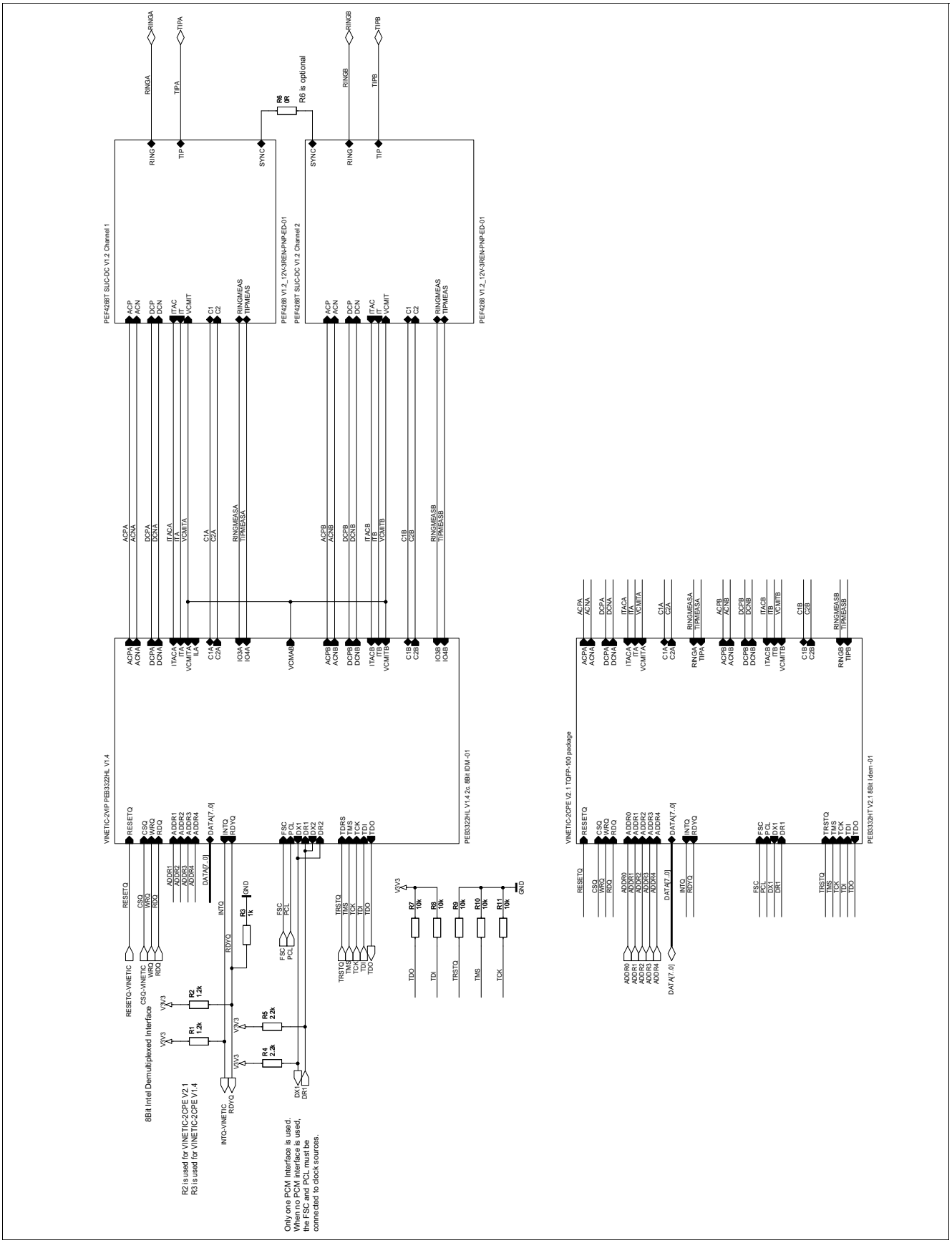


Figure 38 Dual Layout with PEF 3322HL Version 1.4, PEB 3332HT Version 2.1 & PEF 4268T (Top Sheet)

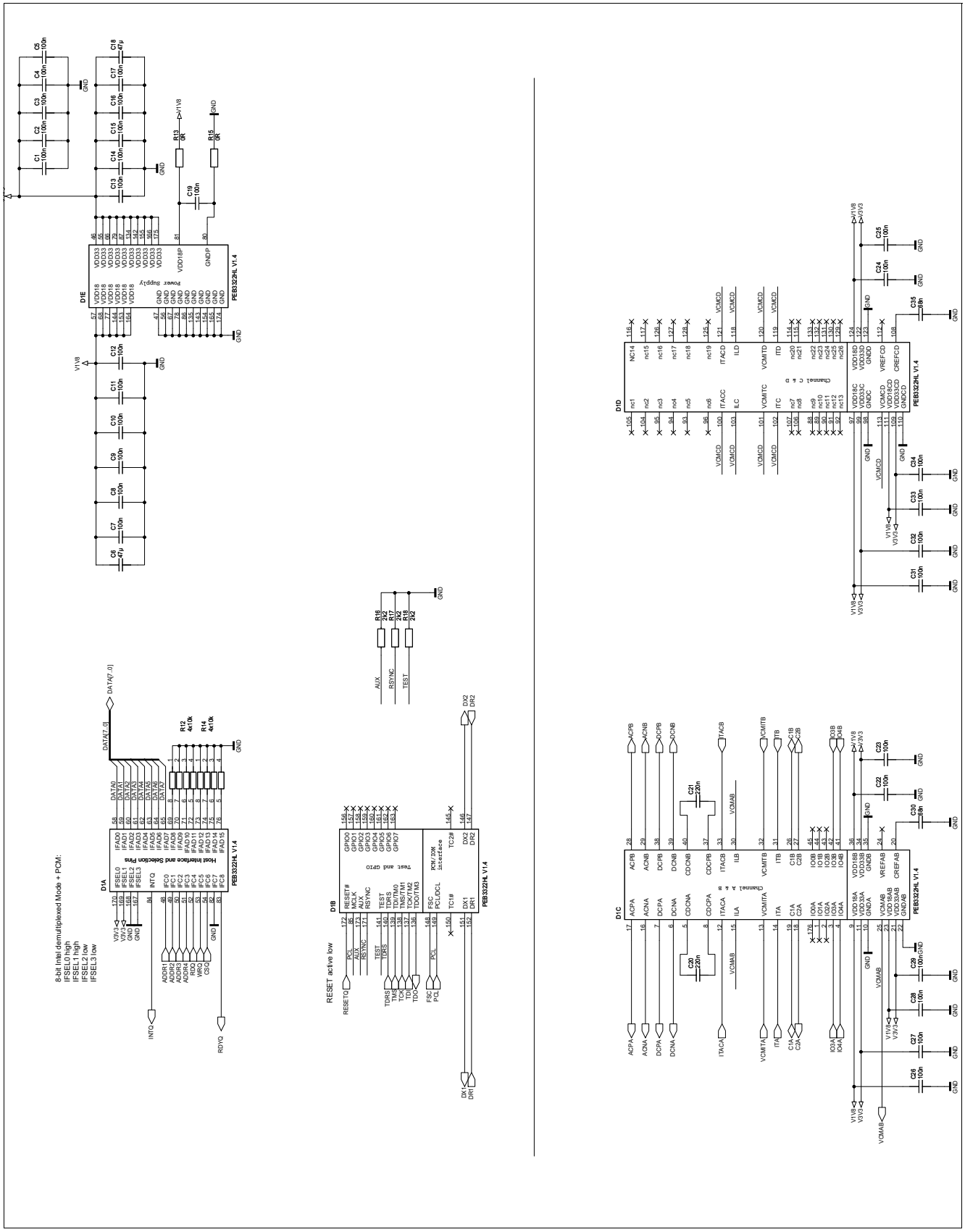


Figure 39 Dual Layout: Part PEF 3322HL Version 1.4 8 Bit Intel Demultiplexed Mode

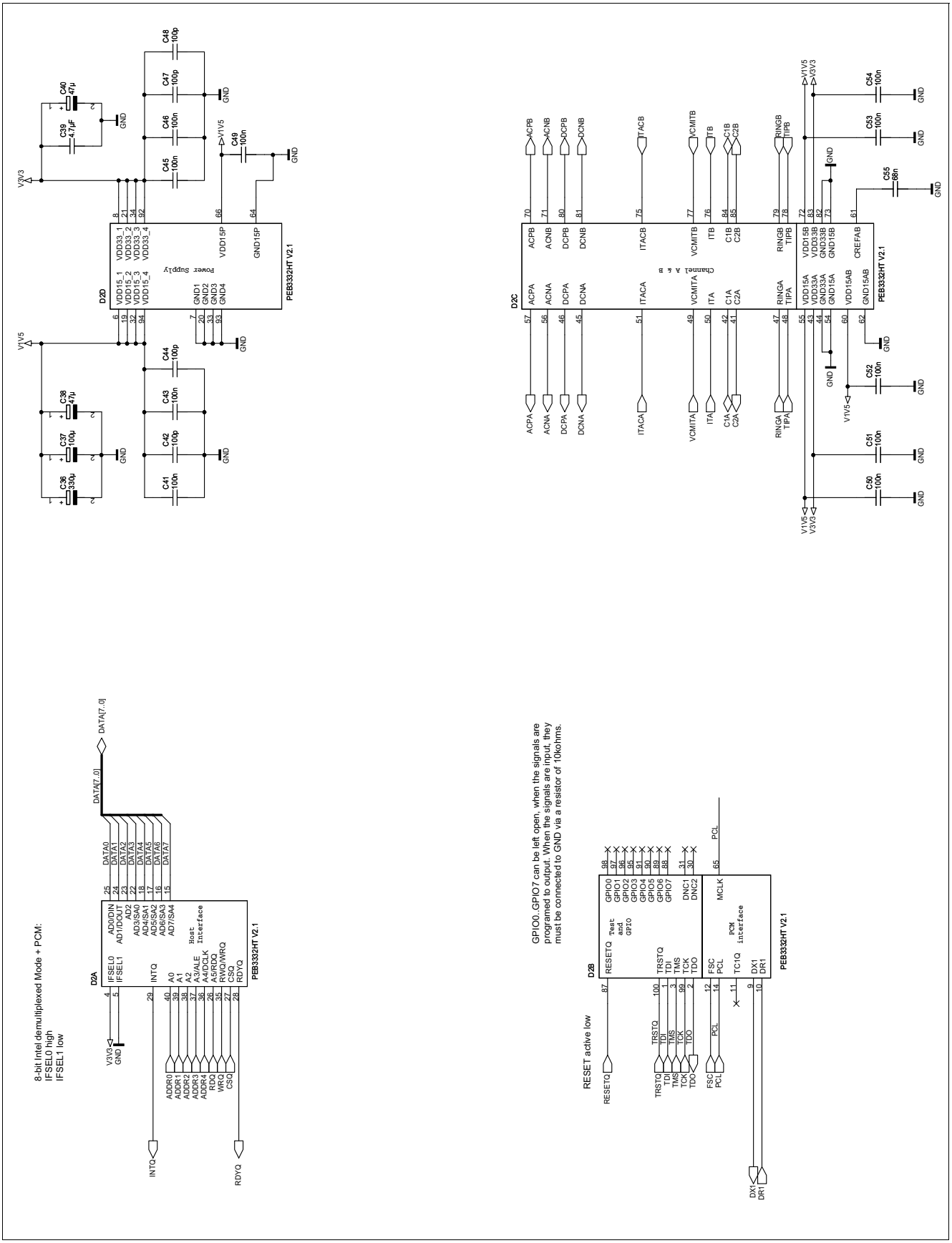


Figure 40 Dual Layout: Part PEB 3332HT Version 2.1 8 Bit Intel Demultiplexed Mode

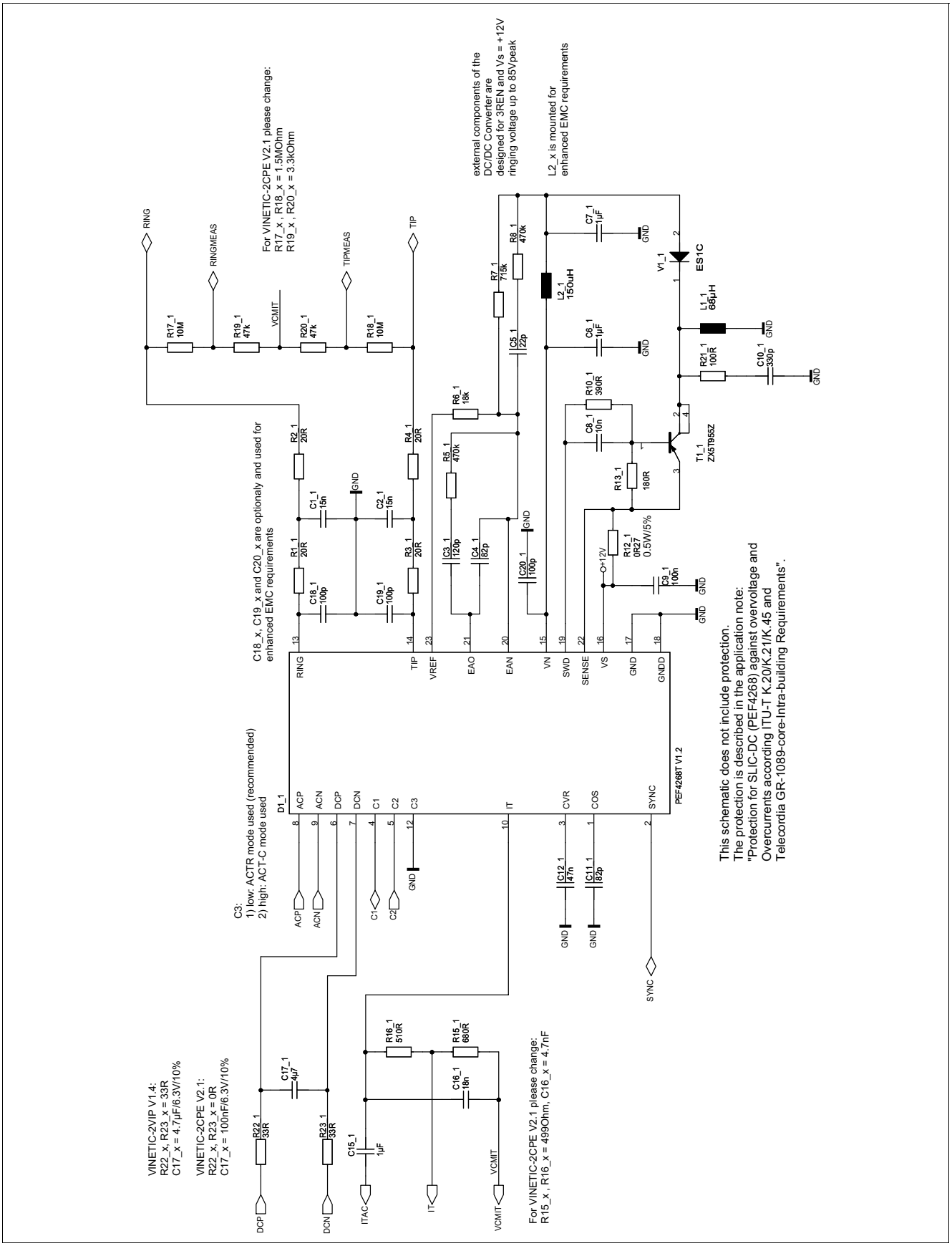


Figure 41 Dual Layout: SLIC-DC (PEF 4268T) Version 1.2 Channel A (for 3REN ringing load)

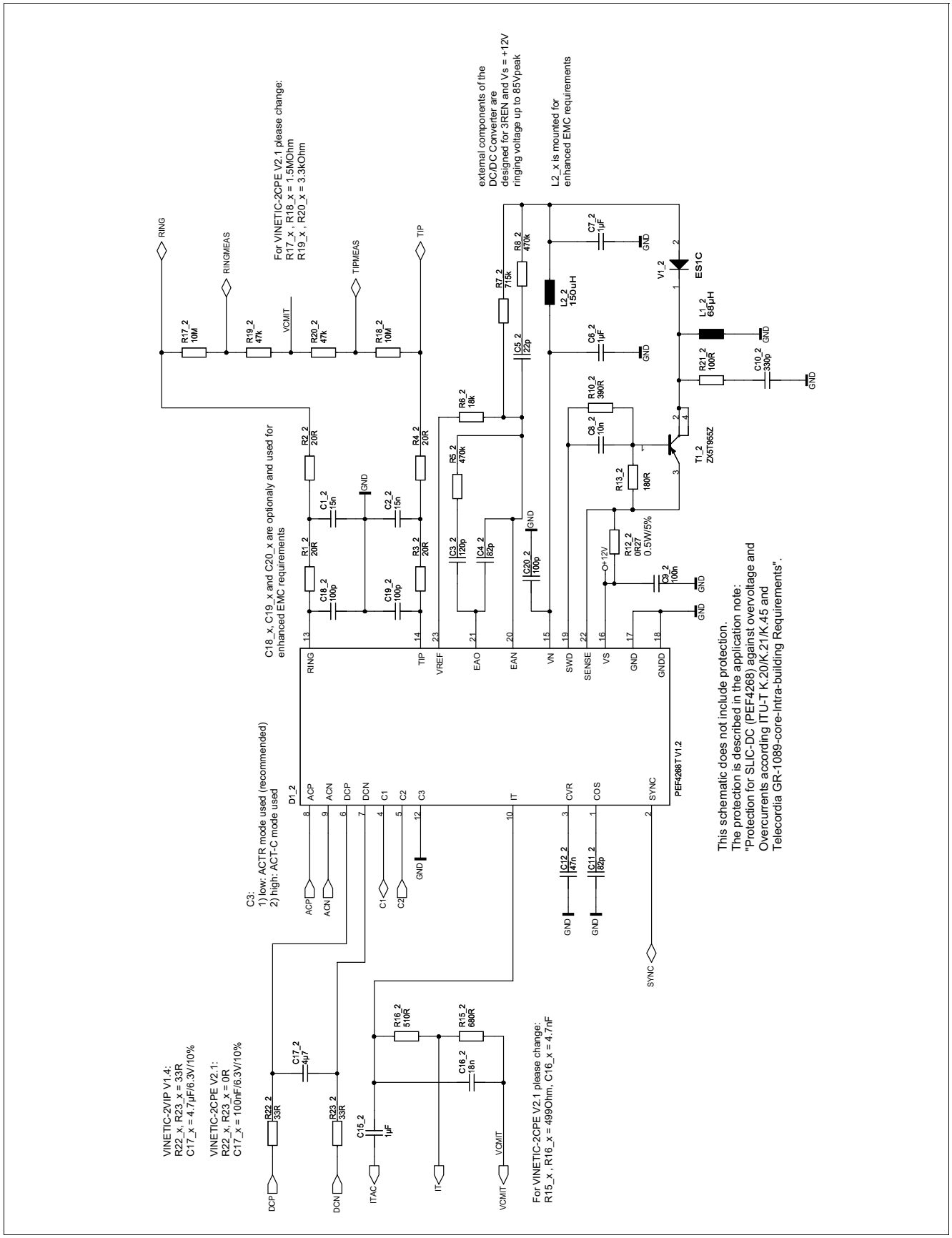


Figure 42 Dual Layout: SLIC-DC (PEF 4268T) Version 1.2 Channel B (for 3REN ringing load)

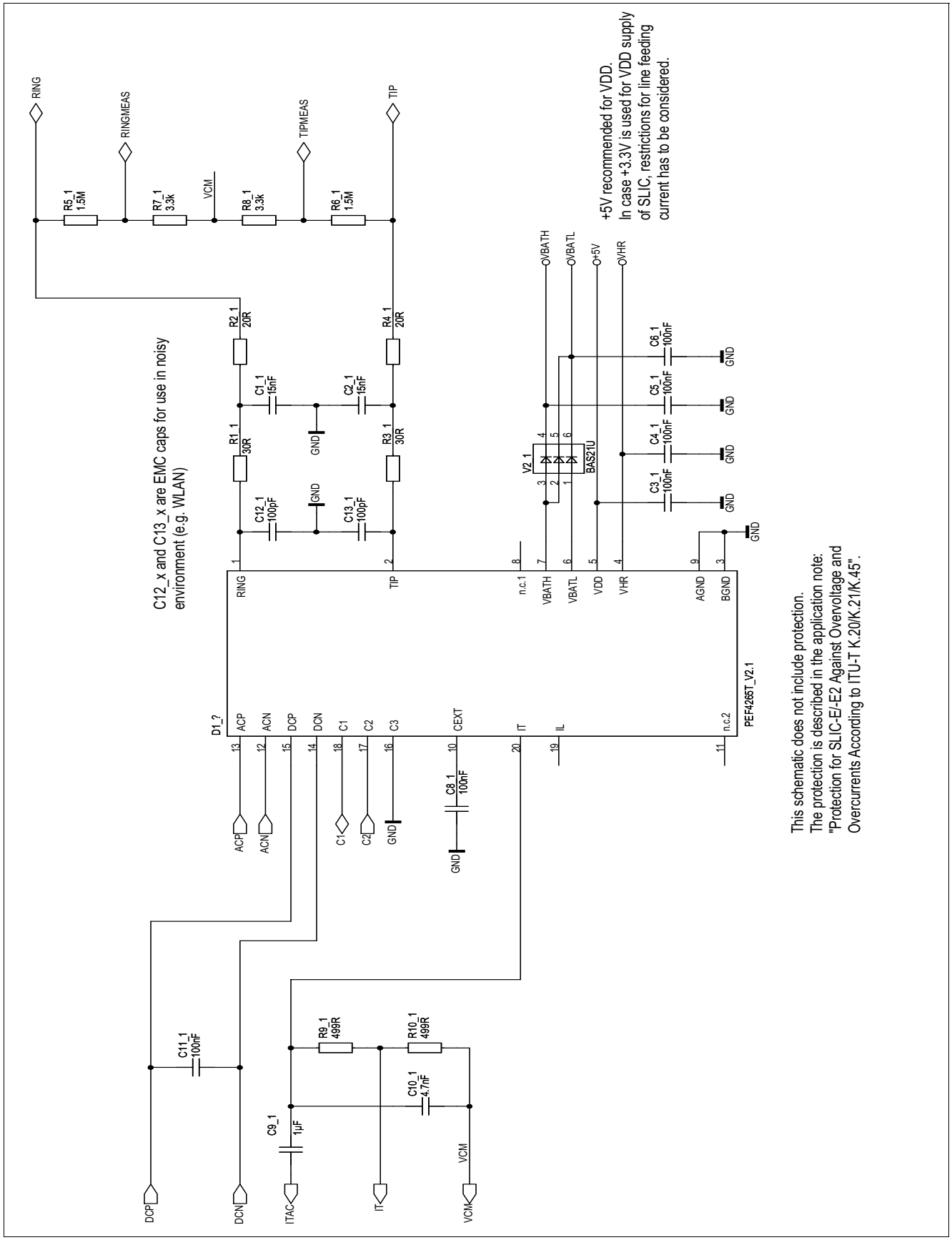


Figure 43 SLIC-E (PEF 4265 T) Version 2.1 Channel A

References

[1] VINETIC®-2CPE (PEB 3332) Version 1.4 Prel. Data Sheet Rev. 3.0, 2005-07-18

[2] VINETIC®-2CPE/-1CPE (PEB 3332/-3331) Version 2.1 Prel. Data Sheet Rev. 2.0, 2006-02-13

[3] VINETIC®-CPE Version 2.1 Prel. User's Manual System Description Rev. 1.0, 2006-01-31
VINETIC®-CPE Prel. User's Manual System Description Rev. 1.1

[4] VINETIC®-CPE Version 2.1 Device Driver Prel. User's Manual Driver and API Description Rev. 1.0, 2006-01-31
VINETIC®-CPE Device Driver Prel. User's Manual Driver and API Description Rev. 1.1, in preparation

[5] VINETIC®-CPE Device Driver Prel. Porting and Integration Guide Rev. 1.0 , 2006-03-01

[6] VINETIC®-CPE System Package Release Notes

[7] SLIC-DC (PEF 4268) Version 1.2 Prel. Data Sheet Rev. 2.0, 2005-07-11

[8] SLIC-E/TSLIC-E (PEF 4265/PEF 4365) Version 2.1 Preliminary Data Sheet Rev. 1.0, 2006-01-20

[9] SLIC-DC (PEF 4268) Version 1.2 Application Note Protection Against Overvoltages and Overcurrents According to ITU-T K.20/K.21/K.45 and Telecordia GR-1089-core Intra-building Requirements Rev. 2.0, 2005-10-04

[10] SLIC-E (PEB_4265) Version 1.2 Application Note Protection for SLIC-E/-E2 Against Overvoltages and Overcurrents According to K.20/K.21/K.45

Attention: Please refer to the latest revision of the documents.

Standards References

[11] ANSI/UL 60950-2000, December 1, 2000, Safety of Information Technology Equipment

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