SLIC-DC

Subscriber Line Interface Circuit with Integrated DC/DC Converter

PEF 4268, Version 1.2

Wireline Communications

Never stop thinking.

Edition 2005-07-11

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
81669 München, Germany

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Revision History: 2005-07-11, Rev. 2.0

Previous Version: Rev. 1.1

Page	Subjects (major changes since last revision)
all	Chip Version changed from Version 1.1 to 1.2

Trademarks

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1 General Description

The SLIC-DC (PEF 4268) is a high-voltage ringing Subscriber Line Interface Circuit with integrated DC/DC-converter. The device is fabricated in Infineon Technologies' well-proven Smart Power SLIC process SPT170 and forms a reliable interface between telephone line and any codec out of Infineon's VINETIC or DuSLIC family.

SLIC-DC is able to provide cost optimized solutions particularly in CPE applications, requiring only a single power supply voltage between 9 V and 40 V. All the necessary POTS supply voltages are generated by the on-chip buck-boost DC/DC converter together with a minimum of external components. Due to the high 150 V supply voltage limit, all requirements on the ring signal can easily be met, even for worst-case loads (e.g. 5 US-REN).

As usual, in the regular active transmission modes the DC/DC converter output voltage tracks the DC line voltage. But additionally SLIC-DC offers the unique feature to extend this tracking concept to the ringing mode, thereby drastically reducing on-chip power dissipation. This, on the one hand, allows to use small and cheap packages without any thermal enhancements (P-/PG-DSO-24-8 and P-/PG-TQFP-48-1, resp.) while, on the other hand, reduces power and current requirements for the external DC/DC converter components, a further contribution to system cost reduction.

SLIC-DC based systems offer full programmability of DC and AC characteristics and meet all relevant transmission standards (e.g. Q.552). As with all of Infineon's Codec/SLIC solutions, integrated line and board testing is supported in a very efficient way.

Compared with the former version V1.1, the following main changes have been included in the new SLIC-DC V1.2:

- High impedance inputs at pins DCP/DCN
- Full 150 V operating range for total supply voltage VS - VN
- No longitudinal line current sensing (no IL output pin)
- Pin CEXT (TQFP version of V1.1 only) skipped: not needed for sufficient common mode line voltage filtering

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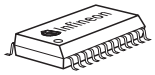
Subscriber Line Interface Circuit with Integrated DC/DC Converter SLIC-DC

PEF 4268

Version 1.2

1.1 Features

- High-voltage Ringing SLIC with integrated DC/DC-converter
- Single supply voltage (+9 V to +40 V)
- Generation of optimized negative SLIC supply voltage
- Minimum power dissipation by line voltage tracking
- Significant ring power reduction by extension of tracking concept to ringing mode
- Up to 125 V peak ring signal
- Ring load up to 5 US REN
- Accurate transversal line current sensing
- Overtemperature protection
- Support of integrated line testing
- Minimum external component count enables low cost system solutions and high board densities
- Robust and reliable Smart Power Technology SPT170
- Package options P-/PG-DSO-24-8, P-/PG-TQFP-48-1



P-/PG-DSO-24-8

P-/PG-TQFP-48-1

Type	Package
PEF 4268 T	P-/PG-DSO-24-8
PEF 4268 F	P-/PG-TQFP-48-1

1.2 Logic Symbol

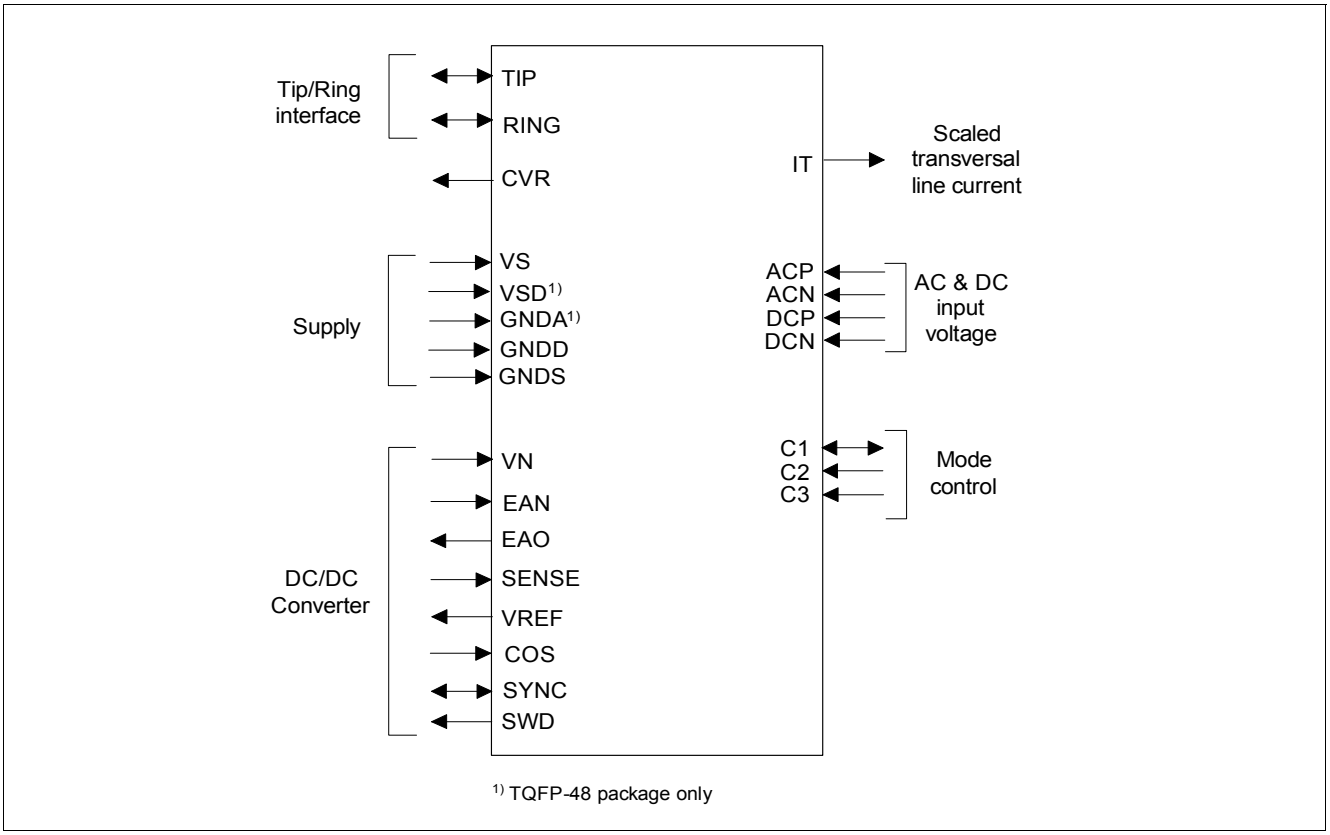


Figure 1 Logic Symbol

1.3 Pin Configurations

1.3.1 Pin Configuration P-/PG-TQFP-48-1 Package

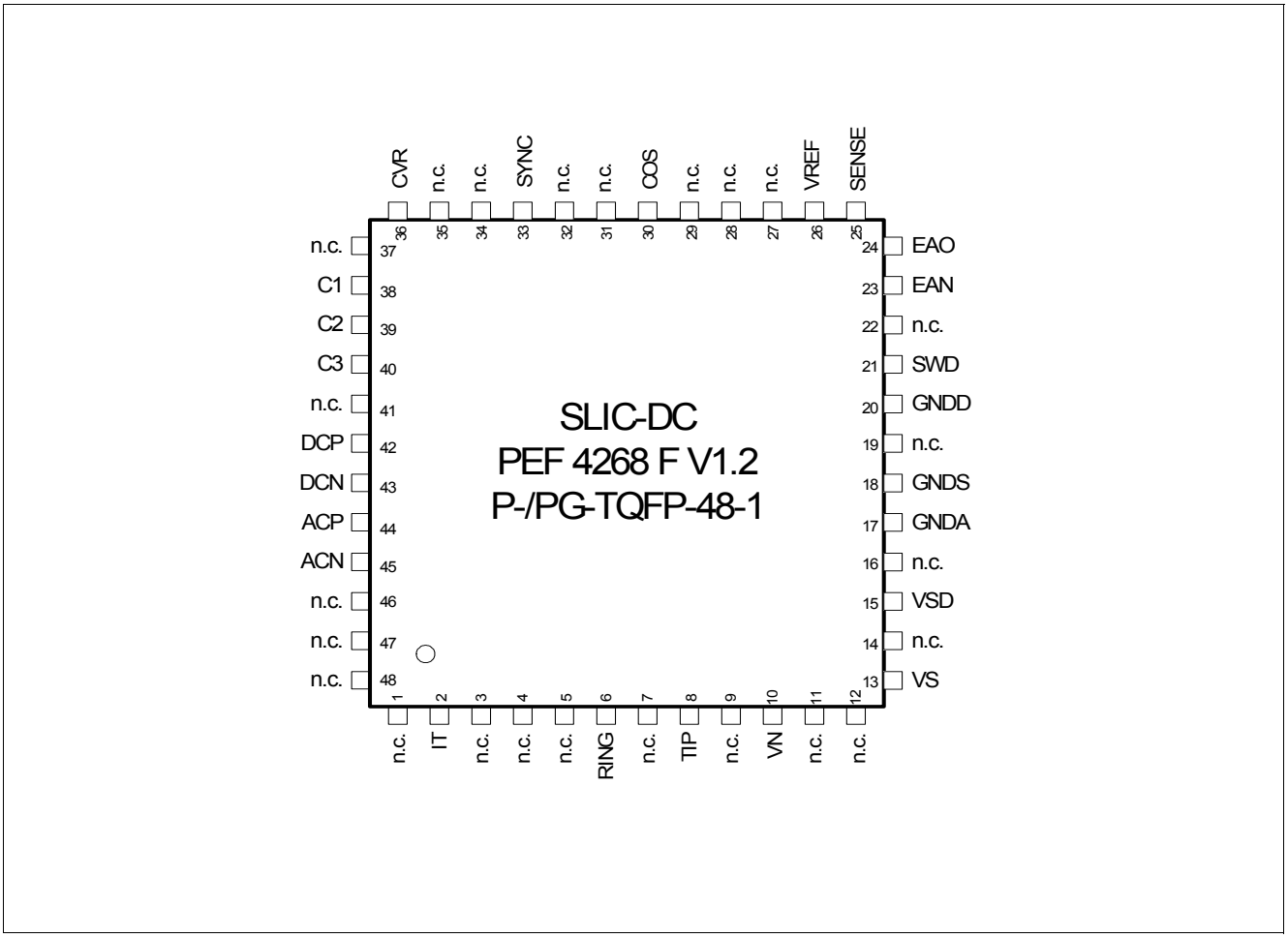


Figure 2 Pin Configuration P-/PG-TQFP-48-1 Package (Top View)

Note: Some of the "not connected" pins are used to increase the minimum distance between high voltage pins.

1.3.2 Pin Configuration P-/PG-DSO-24-8

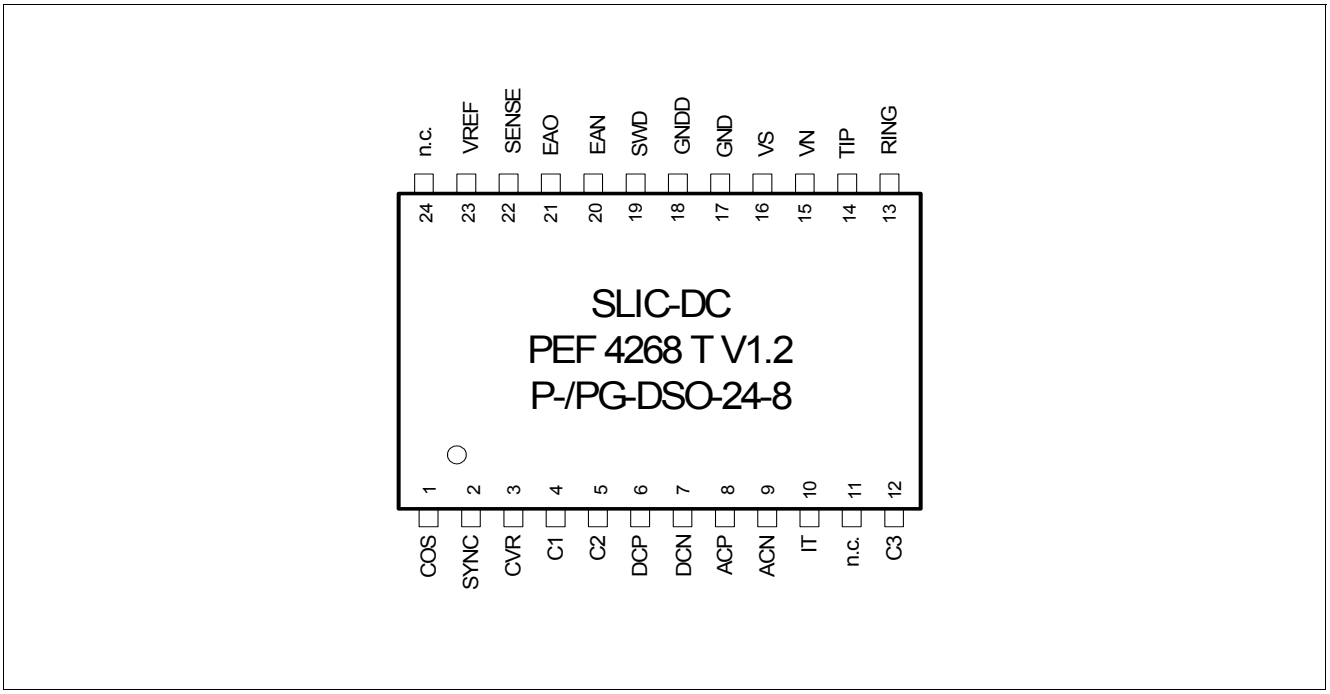


Figure 3 Pin Configuration P-/PG-DSO-24-8 Package (Top View)

1.3.3 Pin Description

Table 1 Pin Definitions and Functions SLIC-DC for P-/PG-TQFP-48-1

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
13	VS	Power	–	Positive supply voltage (9 V < VS < 40 V)
15	VSD	Power	–	Positive supply voltage for gatedriver (9 V < VS < 40 V)
20	GNDD	Power	–	Switch driver ground
18	GNDS	Power	–	DC/DC converter ground
17	GNDA	Power	–	Analog ground
10	VN	Power	–	DC/DC converter output: regulated negative SLIC battery voltage (-130 V < VN < -15 V)
36	CVR	O	–	External capacitor for supply voltage filtering
38	C1	I/O	–	Ternary logic input controlling the operation mode Indication of thermal overload (junction temp > 165 °C)
39	C2	I	–	Ternary logic input controlling the operation mode
40	C3	I	–	Ringing mode control (constant / tracking supply)
33	SYNC	I/O	–	Input for synchronization of the DC/DC converter oscillator with an external clock (falling edge) or output to synchronize multiple devices
30	COS	I	–	External capacitance for sawtooth generator
25	SENSE	I	–	Sense pin for limitation of switch transistor current
23	EAN	I	–	Inverting input of the error amplifier
24	EAO	O	–	Error amplifier output for connection of loop stabilization network
26	VREF	O	–	Reference voltage controlling DC/DC converter output voltage
21	SWD	O	–	Switching transistor driver output
8	TIP	I/O	–	Subscriber loop connection
6	RING	I/O	–	Subscriber loop connection
2	IT	O	–	Transversal line current scaled down by a factor of 50
42, 43	DCP, DCN	I	–	Differential DC or ring input voltage; multiplied by +40
44, 45	ACP, ACN	I	–	Differential AC input voltage; multiplied by +6

Table 2 Pin Definitions and Functions SLIC-DC for P-/PG-DSO-24-8

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
16	VS	Power	–	Positive supply voltage (9 V < VS < 40 V)
17	GND	Power	–	Ground
18	GNDD	Power	–	Switch driver ground
15	VN	Power	–	DC/DC converter output: regulated negative SLIC battery voltage (-130 V < VN < -15 V)
3	CVR	O	–	External capacitor for supply voltage filtering
4	C1	I/O	–	Ternary logic input controlling the operation mode Indication of thermal overload (junction temp > 165 °C)
5	C2	I	–	Ternary logic input controlling the operation mode
12	C3	I	–	Ringing mode control (Constant / tracking supply)
2	SYNC	I/O	–	Input for synchronization of the DC/DC converter oscillator with an external clock (falling edge) or output to synchronize multiple devices
1	COS	I	–	External capacitance for sawtooth generator
22	SENSE	I	–	Sense pin for limitation of switch transistor current
20	EAN	I	–	Inverting input of the error amplifier
21	EAO	O	–	Error amplifier output for connection of loop stabilization network
23	VREF	O	–	Reference voltage controlling DC/DC converter output voltage
19	SWD	O	–	Switching transistor driver output
14	TIP	I/O	–	Subscriber loop connection
13	RING	I/O	–	Subscriber loop connection
10	IT	O	–	Transversal line current scaled down by a factor of 50
6, 7	DCP, DCN	I	–	Differential DC or ring input voltage; multiplied by +40
8, 9	ACP, ACN	I	–	Differential AC input voltage, multiplied by +6

1.4 Functional Block Diagram

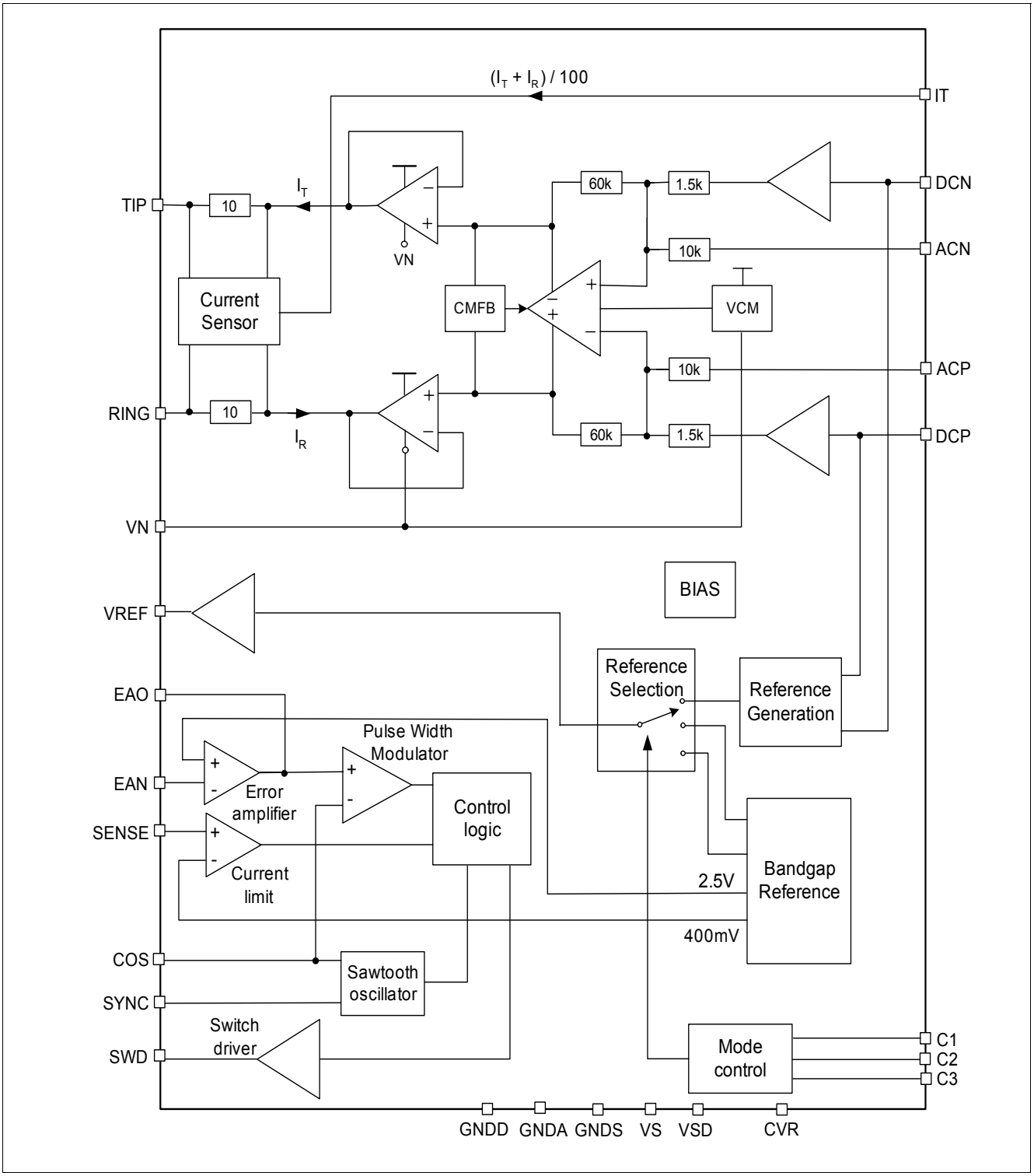


Figure 4 Block Diagram

2 Functional Description

2.1 SLIC Operation

SLIC-DC supports AC and DC control loops based on feeding a voltage V_{TR} to the line and sensing the transversal line current I_{Trans}.

In transmit direction, the DC and AC voltages are handled separately with different gains. Both are applied differentially via the codec interface pins DCP / DCN and ACP / ACN, respectively, defining the transversal line voltage V_{TR} through

$$V_{TR} = V_{TIP} - V_{RING} = 40 \cdot (V_{DCP} - V_{DCN}) + 6 \cdot (V_{ACP} - V_{ACN}) \quad (1)$$

A reversed polarity of V_{TR} is easily obtained by changing the sign of (V_{DCP} – V_{DCN}).

In receive direction, the transversal line current I_{Trans} is sensed and a scaled image is provided at the IT interface pin:

$$I_{IT} = (I_T + I_R)/100 = I_{Trans}/50 \quad (2)$$

This current information is converted to a voltage and split into AC and DC components by an external RC network. Programmable feedback loops are established via the VINETIC / DuSLIC codec to synthesize any required DC and AC line impedance.

Offhook and ring trip detection is also achieved via this regular current sensor.

2.2 SLIC Supply Voltage Generation

Generally, the SLIC's supply voltage is generated and controlled by a buck-boost DC/DC converter. It converts the available positive supply voltage VS, that may range from +9 V to +40 V, to the negative SLIC battery supply voltage VN. The integrated control circuitry together with a few external power parts (switch transistor, inductor, diode and capacitor) allows to control VN in such a way, that at any time it equals the minimum possible value. Beside the obvious advantage, that in a SLIC-DC based system no effort has to be spent for the design of high voltage supplies, this approach also helps to minimize the power dissipation in any active operating mode, independent on line conditions. Particularly in the most critical ring mode a new supply concept (patent pending) leads to significant on-chip power reduction.

Depending on operating mode, the following supply voltages are generated

Onhook

VN is typically set to a constant - 50 V to allow a line voltage of 45 V. This is achieved by selecting an internally generated, accurate fixed reference voltage to control the DC/DC converter. As the loop is open, no current and no power has to be fed to the line. To save power, the switching frequency is set to half the regular value. This is achieved by internally generating an accurate fixed reference voltage for DC/DC control.

Offhook

When the phone goes off-hook, a DC-path is formed and control loops are activated to meet a programmed DC line characteristic, e.g. a constant line current. The optimum supply voltage then would be equal to the required DC line voltage plus an additional constant drop voltage accounting for the AC signal amplitudes, the internal buffer drop and DC inaccuracies. According to **Equation (1)**, the DC line voltage is proportional to the DC input

voltages DCP and DCN; thus these can be used to control the DC/DC converter. If the output voltage VN now is regulated to fulfill

$$VN = -(40 \cdot |V_{DCP} - V_{DCN}| + V_{Drop}) \quad (3)$$

then VN always corresponds to the minimum possible supply voltage. The absolute value in **Equation (3)** accounts for polarity reversal. This well-known method of line voltage tracking obviously guarantees minimum on-chip power dissipation, as the difference between supply voltage VN and DC line voltage V_{TR} is responsible for most of the power dissipated on-chip. From **Equation (3)** and **Equation (1)**, this voltage is always equal to the small value V_{drop}, independent of loop length. Depending on signal requirements, V_{drop} is just 8 or 11 V (with metering).

Ringing

SLIC-DC is the first to consequently extend the supply tracking method to ringing, normally the most critical mode with respect to power. This new approach is highly efficient by using the “quasi-balanced” signal shape. With conventional balanced ringing as depicted in **Figure 5**, the signals at TIP and RING are differential low-frequency sine waves (neglecting DC components) and the circuit is supplied by a constant voltage VN somewhat larger than their peak-to-peak value. In mode ACT-C a constant -75 V supply is chosen allowing balanced sine wave ringing up to approx. 50 Vrms. The commen mode potential VCM, i.e. the mean value (VTIP + VRING) / 2, is constant and equal to half the supply voltage:

$$V_{CM} = \left(\frac{V_{TIP} + V_{RING}}{2}\right) = \frac{VN}{2} \quad (4)$$

Obviously the difference between VN and the line voltage $V_{TR} = V_{TIP} - V_{RING}$ is of sinusoidal shape, too. This on-chip voltage drop unavoidably leads to large on-chip power, at least equal to the ring power delivered to the line. An improvement is obvious: if VN would track the negative signal envelope, power dissipation could be reduced. However, the power saving potential is limited, as a symmetrical tracking approach on the positive side cannot be realized easily.

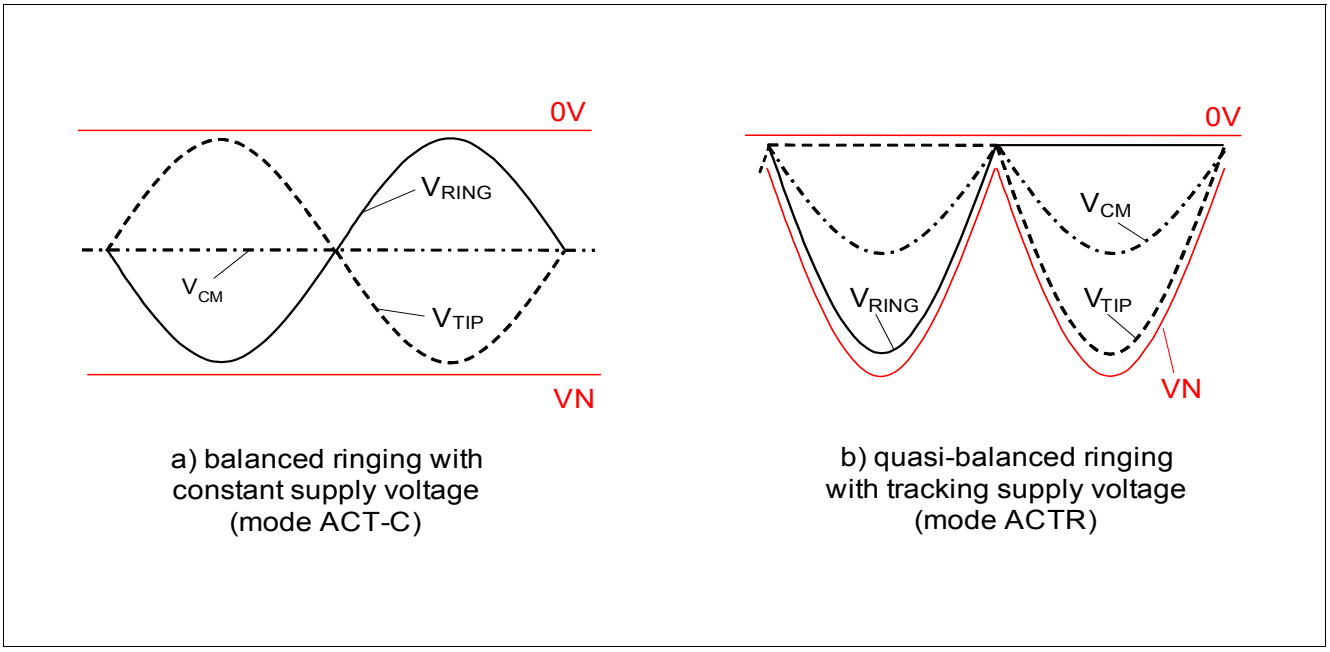


Figure 5 Comparison of Ringing Waveforms

The situation changes with the “quasi-balanced” signal shape of **Figure 5**. Here both line voltages V_{TIP} and V_{RING} alternately exhibit negative sine half waves for half a ring period, whereas stay close to zero for the other half. It is important, that compared to the normal balanced (differential) waveform, the difference voltage on the line, V_{TR}, remains an unchanged large sinewave; however, the positive envelope now is constant. Consequently, the common mode potential V_{CM} is not constant any more, but also shows the sine half wave shape. As is evident from **Figure 5**, if the supply voltage VN is generated to track the negative envelope, the voltage drop in the SLIC, VN - V_{TR}, is minimized at any time to a constant few volts, thus minimizing the resulting on-chip power dissipation. **Equation (4)** then is still valid, i.e. the common mode potential equals half the supply voltage.

From the above, also the inverse argument is valid: If VN has a “rectified sine wave” shape and if V_{CM} fulfills **Equation (4)**, then the respective positive wire is constant and close to ground and the quasi-balanced signal shape results. This indicates a simple generation method, depicted in **Figure 6**. The correct signals automatically result from processing the ring signal input voltage **as if it were a DC voltage**. According to **Equation (3)**, the generated VN is controlled by the absolute value of the DC input voltage difference, leading to the required half sine wave behaviour of VN. In the fully differential input amplifier a common mode feedback loop (CMFB) defines the common mode potential V_{CM}. by deriving (V_{TIP} + V_{RING}) / 2 and comparing it with a reference voltage $V_{ref,CM}$. If now the reference voltage for this common mode loop is chosen to equal VN / 2, then **Equation (4)** is fulfilled and the quasi-balanced voltage shapes result. It is worth noting, that the chosen architecture does not require any additional circuitry compared with the traditional approach. However, the external DC/DC converter components have to be dimensioned to support ring voltage tracking; particularly, this means the use of a relatively low converter capacitance. The new ringing method is very effective in critical applications by typically halving the power dissipation during ring burst.

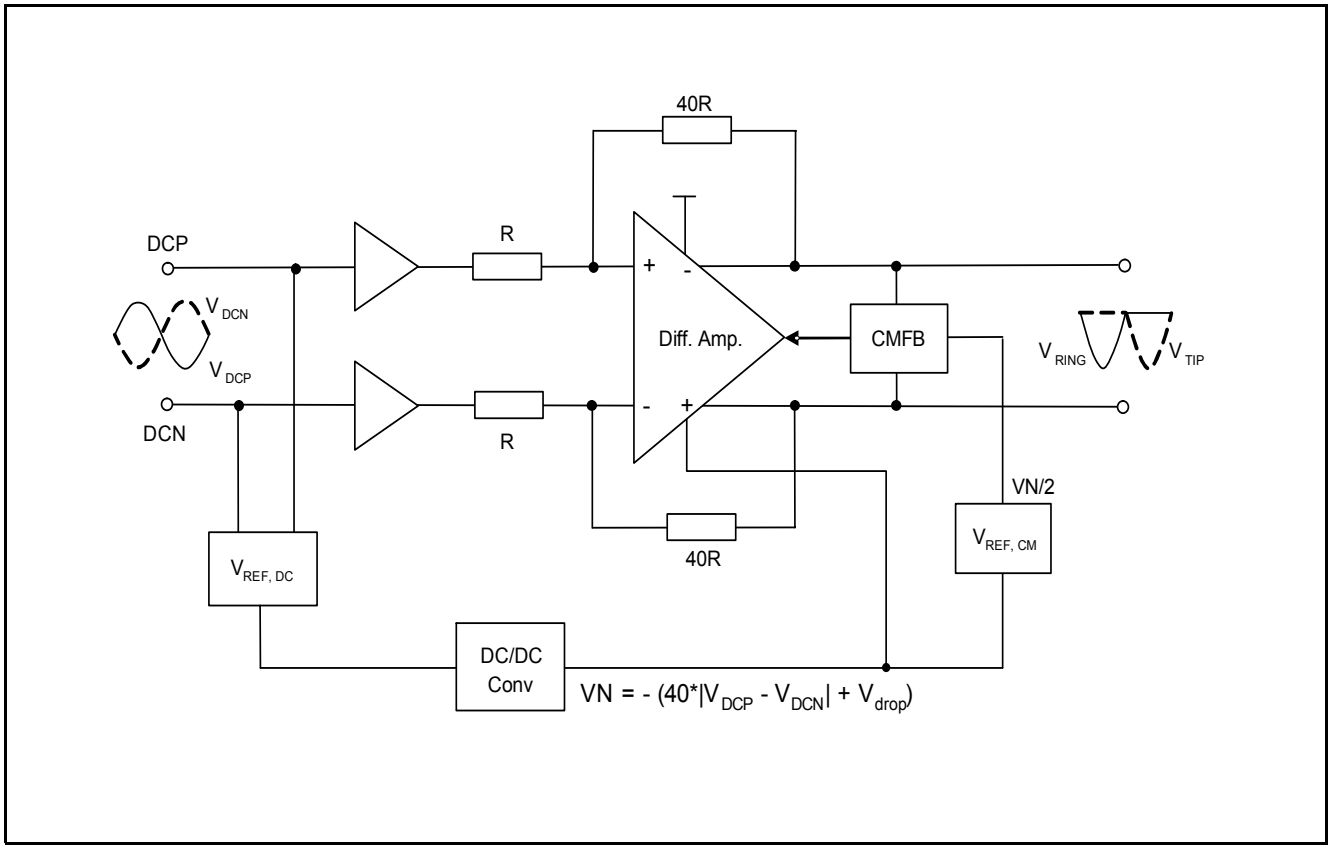


Figure 6 Generation of Quasi-balanced Ring Signal

2.3 Basics of DC/DC Operation

Figure 7 shows the basic topology of a buck-boost DC/DC converter. A conversion cycle, defined by the period of the switching clock, $1/f_{SW}$, starts by closing switch SW and connecting the inductance L with the positive supply VS. As a consequence, the current in the inductor, i_L, rises at a rate VS/L and capacitor C gets discharged by the load current at a time constant $C*Z_L$. After a time t_1 the current has reached its peak value Ip = VS/L * t_1. Then the switch is opened again and the inductor current decreases at a rate VN/L, i.e. proportional to the output voltage VN. During this time t_2 energy is transferred from the inductor to the capacitor and the load and C is charged again. The ratio of on-time t_1 to switching period $1/f_{SW}$ is the duty cycle D. For proper operation, D has to stay in a range of appr. 0.1 to 0.9. From the converter control dynamics it is crucial, that zero inductor current is reached within any conversion period (discontinuous current mode operation). This means, that the total energy stored in the inductor, $L * I_p^2 / 2$, has been transferred to C and Z_L, increasing the output voltage by ΔVN. In equilibrium, if this energy is equal to the energy, that is dissipated in the load during one conversion cycle, VN stays constant. This can be achieved by controlling time t_1, and thus peak current Ip and the transferred energy.

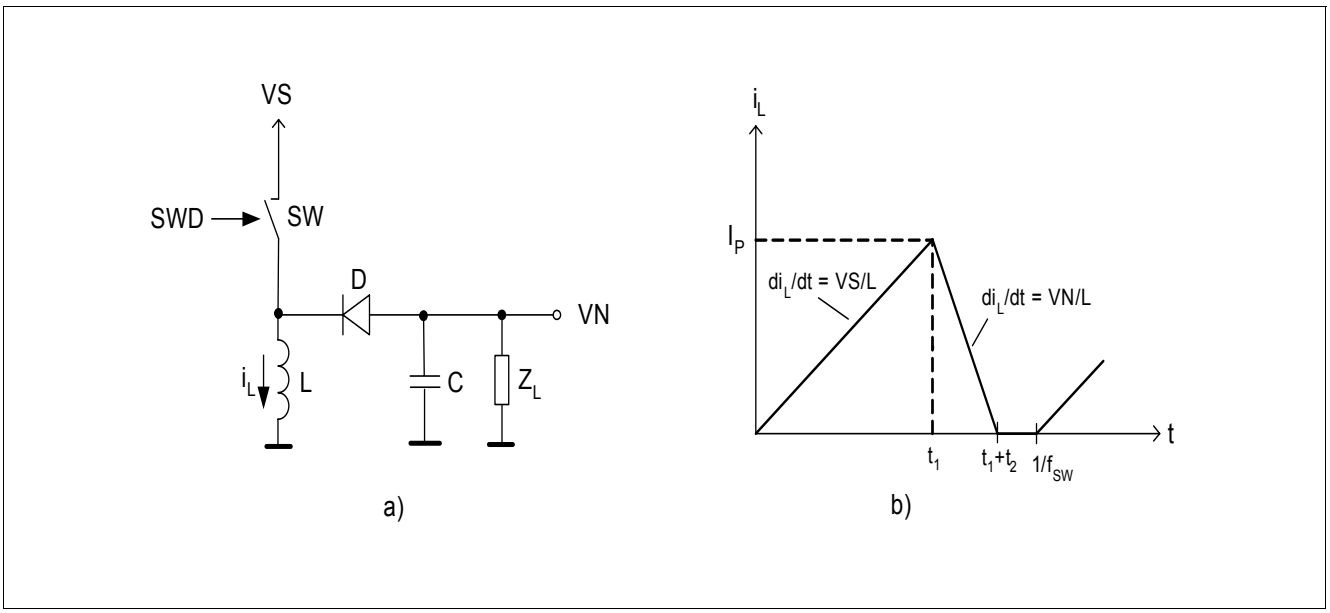


Figure 7 Basic Buck-Boost Topology (a) and Inductor Current (b)

The most important relations for dimensioning the external DC/DC components follow from above. The condition of reaching zero inductor current during any conversion cycle, is equivalent to the discontinuity equation

$$t_1 + t_2 = I_p \cdot \left(\frac{L}{VS} + \frac{L}{VN}\right) < \frac{1}{f_{SW}} \tag{5}$$

The energy transfer condition states, that during any conversion cycle the energy stored in the inductor must be equal to the energy dissipated in the load

$$\frac{L \cdot I_p^{\,2}}{2} = \frac{P_{VN}}{\eta \cdot f_{SW}} \tag{6}$$

Here P_{VN} is the mean load power during a conversion cycle, while the efficiency η accounts for all nonidealities and losses. Obviously P_{VN} varies strongly, depending on the operating mode.

Substituting **Equation (6)** in **Equation (5)** yields an upper limit for the inductance:

$$L < \left(\frac{VS \cdot VN}{VS - VN}\right)^2 \cdot \frac{\eta}{2 \cdot f_{SW} \cdot P_{VN,\,max}} \tag{7}$$

It should be pointed out, that higher power reqires lower inductor values, but from **Equation (6)** this means higher peak currents. In most cases of practical importance, the maximum output power coincides with the maximum output voltage VN_{max}, i.e. the load Z_L is ohmic (note, that the US ringer equivalent also forms a nearly ohmic load). With practical VN_{max} / VS ratios (6 to 10) (**Equation (7)**) is reduced to

$$L < 0{,}7 \cdot \left(\frac{VS}{VN_{max}}\right)^2 \cdot \frac{\eta \cdot R_L}{2 \cdot f_{SW}} \quad (8)$$

Once L is chosen, the peak current, one of the most important parameters for component selection, results from (**Equation (6)**). Examples are calculated in **Chapter 4.3.1**.

The concept of ring supply voltage tracking obviously poses an upper limit to the DC/DC capacitance C due to the d(VN)/dt requirements. On the other hand, the voltage change ΔVN during each conversion cycle due to charge storage in this capacitance is inversely proportional to C. This voltage change is a significant component of the total ripple voltage on VN. Therefore an additional RC low-pass filter at the output (see **Figure 10**) is recommended to sufficiently smooth VN.

2.4 DC/DC Details

Figure 8 contains the main functional blocks and components of the DC/DC converter. Here the power switch of **Figure 7** is realized by pnp transistor QSW, and a control loop is formed to regulate the generated output voltage to the required value. In equilibrium, the mean voltage at the Error Amplifier input EAN, averaged over one conversion cycle, is equal to the 2.5 V reference. Thus the mean converter output voltage VN' is defined by the reference voltage VREF through

$$VN' = -40 \cdot [VREF - (2,5V)] + 2,5V \quad (9)$$

Equation (3) can easily be fullfilled by properly deriving VREF from the DC input voltages, thus providing the optimized supply voltage in off-hook and ring modes. This is due to the choice of identical gains for DC/DC loop and SLIC receive path. For on-hook operation or ringing with constant supply, fixed reference voltages result in fixed supply voltages of typically -50 and -75 V, resp.

From the above, the voltage at EAN is proportional to VN' and thus changes during the conversion cycle. However, in equilibrium the mean value is 2.5 V, and then the net output current at EAO is zero and the voltage at EAO remains constant. This voltage is now compared with the output voltage of a sawtooth oscillator in the pulse width modulator and thereby defines the duty cycle of the output pulse, i.e. the time t_1 the switch transistor is on. The control loop forces t_1 and thus the peak current and the energy stored in the inductor, to fulfill the energy transfer condition of **Equation (6)**. If the load power changes, VN' will change accordingly, resulting in a non-zero input voltage to the error amplifier. This will cause net output current and a change in output voltage, thereby also changing the switching duty cycle. The RC network connected to the error amplifier's input EAN defines the dynamic behaviour of the control loop (stability, settling behaviour, overshoot). The values proposed in the application circuit of **Chapter 3** are optimized for a switching frequency of 100 kHz and guarantee stable operation and good settling behaviour under all load conditions.

The sawtooth oscillator is realized by simply charging and discharging the external capacitance at COS between +3 and +5 V at +30 and -80 µA, respectively. With a capacitance of 82 pF, a typical switching frequency f_{SW} of 100 kHz results (**Figure 11**). An increase in f_{SW} by lowering COS would on the one hand reduce inductance value and size, but on the other hand lead to higher switching losses and thus lower efficiency. So the 100 kHz can be regarded as an optimum. The switching cycles of up to 8 different PEF 4268 devices can be synchronized at the highest respective clock frequency by either connecting their SYNC pins or using an external clock signal with a frequency in excess of the fastest internal clock.

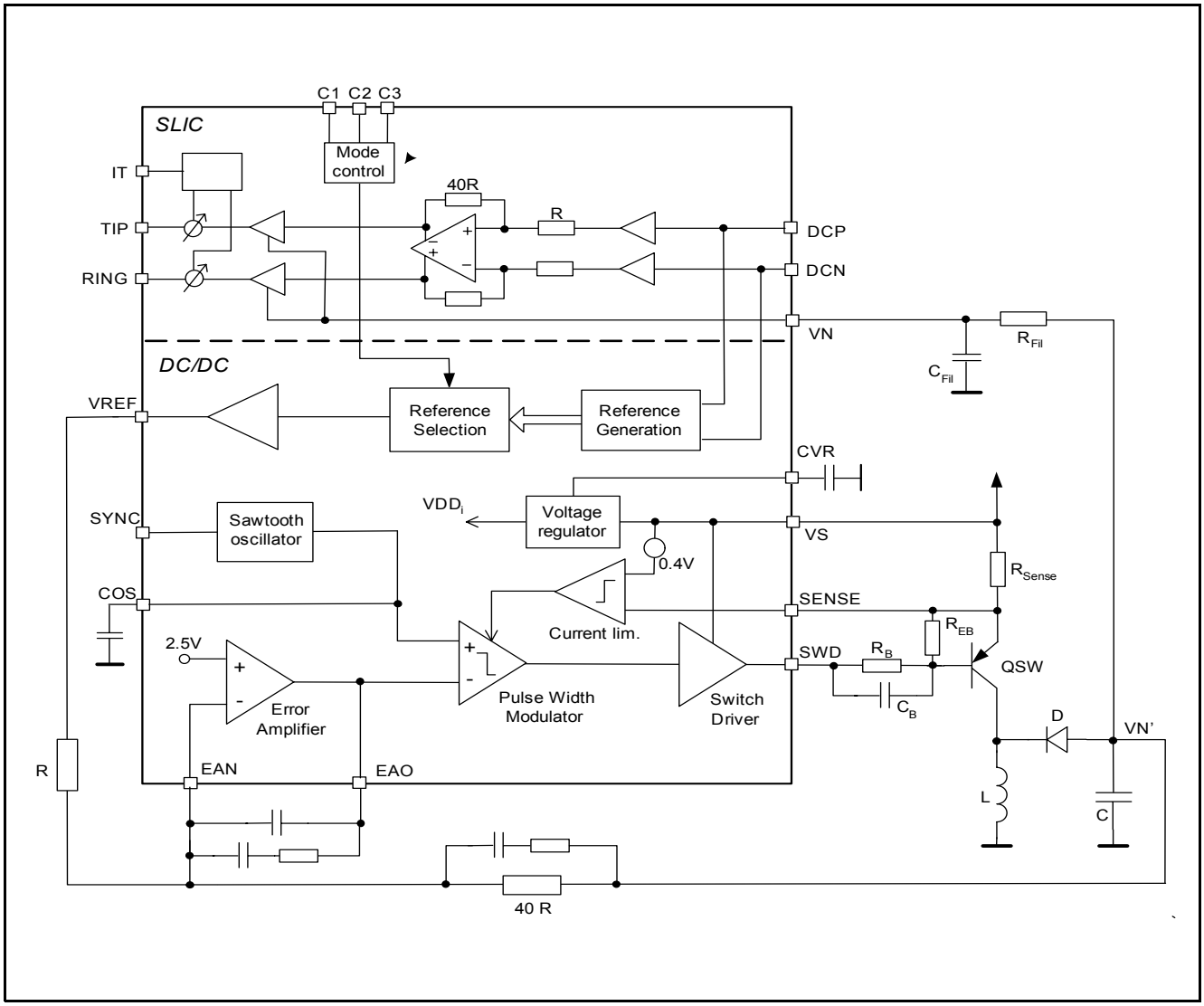


Figure 8 DC/DC Blocks and Components

The switch driver is designed to drive either pnp or pMOS transistors. Its output voltage is clamped to a voltage swing of typically 8 V, thus switching between the input voltage VS and VS - 8 V. When driving a pnp transistor, this swing is still high, and thus a base resistor R_B is used to limit DC base current. The parallel capacitance CB forms a low-impedance path required for fast switching off transistor QSW. Additionally, resistor R_{EB} helps to discharge the large emitter-base diffusion capacitance. The emitter current in the switch transistor is sensed via an external resistor. If the voltage drop across R_{Sense} exceeds a typical 0.4 V, the current limitation block switches off QSW.

As VS may cover a broad range of 8.7 to 40 V, a voltage regulator provides the internal supply voltage VDD_i of typically 7.5 V. CVR is used to filter this voltage.

Finally, R_{Fil} and C_{Fil} are needed to reduce the ripple voltage on VN'. This ripple voltage is not only due to the unavoidable charging and discharging of C, but includes also components caused by the ohmic resistances of the converter's L, C, and D. Nevertheless, due to the SLIC's good power supply rejection, the cheap RC-filter is sufficient to meet all relevant transmission standards.

2.5 External Component Selection

From the above, the main criteria for selecting the key external DC/DC components, i.e. switch transistor, inductor and capacitor can be derived. All other externals are given in the reference schematics of **Chapter 3**.

2.5.1 Inductor

The inductance value L is limited by the condition for discontinuous current operation to fulfill **Equation (7)** and **Equation (8)**, resp. The higher the maximum power or the the maximum output-to-input voltage ratio VN/VS (both typically happens during the peak of the ringing signal), the lower the upper limit for the inductance. This is due to the fact, that lowering the inductance allows higher peak currents, thereby increasing the energy storage capability per conversion cycle, $L*I_p^2/2$. This value defines size and cost of the inductor. For moderate ringing loads, an $L*I_p^2$ of around 100 µWs is achievable with cheap SMD parts (see calculation example in **Chapter 4.3.1**). The ohmic resistance causes some power loss, but typically is not dominating overall efficiency.

2.5.2 Switch Transistor

SLIC-DC supports both pnp and pMOS switching transistors. Independent on type, the voltage and current specifications are evident: collector-emitter and source-drain breakdown voltages must exceed the sum of highest input and output voltage VS - VN (the on-chip limit due to the wafer process is 150 V), whereas the peak inductor current treated above also defines the maximum switch current. All other deviations from an ideal switch finally cause power dissipation in the transistor, thus influencing converter efficiency. The most important parameters influencing efficiency are: current gain, transit frequency and saturation voltage for pnp, gate charge and on-resistance for pMOS transistors. Whereas pnp transistors are recommended for lowest cost applications and are restricted to a maximum 20 V supply, pMOS switches work over the full supply range up to 40 V at highest efficiency. **Figure 9** gives the measured overall efficiency for the respective reference application circuits, defined as the ratio of the output-to input power ratio, P_{VN}/P_{VS}

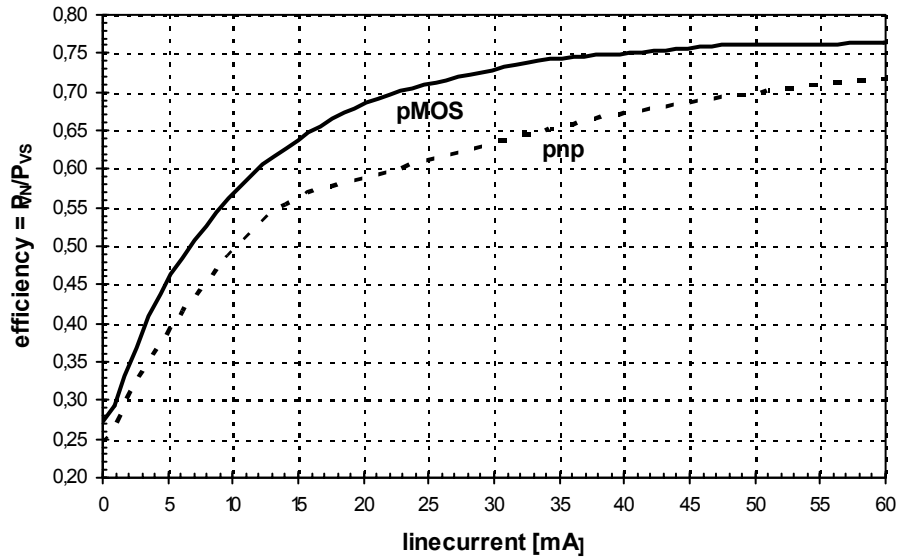


Figure 9 Efficiency versus Line Current, f_{SW} = 105 kHz

As explained in **Chapter 2.4**, resistor R_{Sense} has to be chosen to always limit the current through QSW to a safe value I_{lim}; when choosing R_{Sense}, the maximum power dissipation P_{max} has to be taken into account, too. Obviously the following relations are valid:

$$I_{lim}[A] = \frac{0,4V}{R_{Sense}} > I_p$$

$$P_{max} > I_{lim}^{2} \cdot R_{Sense} \quad (10)$$

2.5.3 Capacitor

From DC/DC principles, the output capacitor gets charged and discharged during any conversion cycle. This charge, depending on the load power, leads to a voltage change across VN of

$$\Delta VN_C = \frac{D \cdot P_{VN}}{VN \cdot C \cdot f_{SW}} = \frac{t_1 \cdot I_{Load}}{C} \quad (11)$$

Here D again denotes the duty cycle. Obviously, to achieve low ΔVN_C, C has to be chosen as high as possible. On the other hand, the tracking ring voltage concept requires, that the time constant formed by C and and the equivalent load resistance be higher than the highest ring frequency. Thus C is limited to values in the 1 µF range, leading to relatively high C-related voltage ripple compared with conventional solutions. As there is also a ripple component related to the capacitors equivalent series resistance (ESR), the total voltage ripple equals

$$\Delta VN = \Delta VN_C + \Delta VN_R = \frac{t_1 \cdot I_{Load}}{C} + I_p \cdot ESR \quad (12)$$

The two terms typically are of the same order of magnitude. From this point of view and from the fact, that C requires a voltage capability of at least VN, a low capacitance value finally helps to reduce BOM. Due to the good PSRR of the differential SLIC architecture, a simple first order RC filter is sufficient to reduce switching induced distortions on the line to an acceptable level.

2.6 Operating Modes

The PEF 4268 (SLIC-DC) can be operated in the following modes, controlled by ternary logic signals at the C1 and C2 input pins; C3 enables the choice between the two different ring modes.

Table 3 SLIC-DC Interface Code (C1, C2, C3)

		C2				
		L	**M**	**H**		
C1	**L**[1)]	PDN	ONHK	ONHK		**C3**
	M	ACT-T	ACT	ACT(R)	L	
		ACT-T	ACT	ACT-C	H	
	H	HIRT	HIT	HIR		

1) No ‘Overtemp’ signalling possible via pin C1 if C1 is low.

Table 4 SLIC-DC Operating Modes

Mode	Mode Description	VN Supply	Functionality
PDN	Power Down	-	None
ONHK	Active Onhook	- 50 V	DC/DC, Line driver + Preamplifier, Current Sensor
ACT / ACT(R)	Active	- (40* $\lvert V_{DCP}-V_{DCN}\rvert + V_{Drop1}$)	DC/DC, Line driver + Preamp., Sensor
ACT-T	Active Teletax	- (40* $\lvert V_{DCP}-V_{DCN}\rvert + V_{Drop2}$)	DC/DC, Line driver + Preamp., Sensor
ACT-C	Active constant supply	- 75 V	DC/DC, Line driver + Preamp., Sensor
HIT	High Impedance on TIP	- 75 V	DC/DC, RING-Amplifier, Sensor
HIR	High Impedance on RING	- 75 V	DC/DC, TIP-Amplifier, Sensor
HIRT	High Impedance on RING and TIP	- 75 V	DC/DC, Sensor

Power Down (PDN)

PDN offers high impedance at TIP and RING. All SLIC and DC/DC converter functions are switched off. Off-hook detection is not available.

Active Onhook (ONHK)

With respect to all other active modes, power consumption is reduced by omitting every second DC/DC switching cycle. VN is regulated to a constant -50 V, while the line voltage is set to typically 45 V.

Active (ACT / ACT(R))

This is the regular transmit and receive mode for voice band and ringing. The supply voltage VN is regulated by the DC/DC converter to track the DC line voltage,

VN = - (40* $\lvert V_{DCP}-V_{DCN}\rvert + V_{Drop1}$)

V_{Drop1} is a constant voltage drop required for voice signal transmission (typically 8 V). The same SLIC mode can be chosen, if a ring signal is applied at DCP/DCN. Then the supply voltage follows the ringing voltage as explained in **Chapter 2.2**, thereby minimizing power dissipation.

Active Teletax (ACT-T)

Like ACT, but with an increased voltage drop V_{Drop2} of 11 V to additionally enable the transmission of metering signals.

Active Constant Supply (ACT-C)

Like ACT, but with the DC/DC converter providing a constant supply voltage of typ. - 75 V; intended for ringing to achieve a conventional balanced ringing waveform.

High Impedance (HIR, HIT, HIRT)

In these modes each of the line outputs can be programmed to show high impedance. HIT switches off the TIP buffer, while HIR switches off the RING buffer. The current through the active buffer is still measured at IT. In the HIRT mode both buffers show high impedance. The current sensor remains active thus allowing sensor offset calibration (for test purposes). In all high impedance modes the DC/DC converter provides a -75 V supply voltage.

2.7 Current Limitation/Overtemperature

In any operating mode (except Power Down), the total current delivered by the output drivers is limited to approximately 100 mA. If the junction temperature exceeds 165 °C, pin C1 sinks a signalling current I_{therm} to indicate overtemperature. In this case switching to PDN mode is recommended.

3 Typical Application Circuit

Figure 10 shows an example for a typical low-cost application of SLIC-DC in the P-/PG-DSO-24-8 package with a pnp-type switching transistor. By using a pMOS switch, efficiency can be improved (see **Figure 9**). The DC/DC part is dimensioned to allow dynamic ring voltage tracking, but is applicable for constant voltage ringing, too. In **Table 5** the recommended typical values of the external components for an applicatiation with VS = 12 V, f_{SW} = 100 kHz, V_p = 85 V and moderate ringer load (3 REN); the circuitry for both switch transistor types is listed. Overvoltage protection topics are covered in the Application Note “Overvoltage Protection for SLIC-DC”, Release Date 2004-10-14.

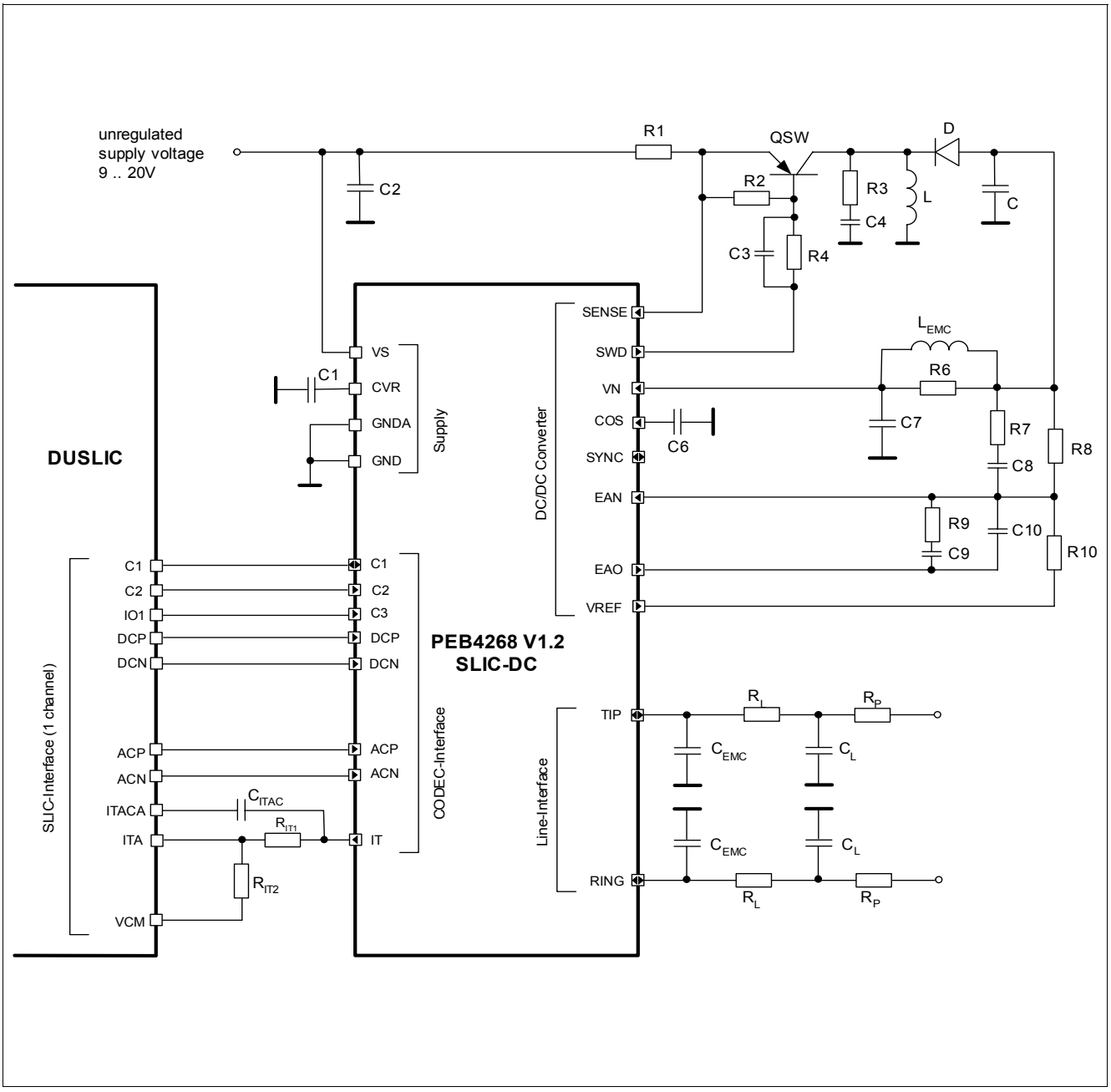


Figure 10 Application Circuit

Table 5 Components for SLIC-DC Application Circuit

	Symbol	Function	Typ. Value	Unit	Tolerance	Rating
2	R_L	Overcurrent limitation, stabilization	20	Ω	1 % (rel.)	0.25 W
2	C_L	EMC filtering	15	nF	10 % (rel.)	100 V
2	C_{EMC}	Optional EMC filtering in noisy environment	100	pF	10 %	100 V
2	R_P	Overcurrent limitation, EMC filtering	20	Ω	1 % (rel.)	0.25 W (depending on protection requirements)
1	R_{IT1}	IT current/voltage conv. AC	470	Ω	1 %	0.1 W
1	R_{IT2}	IT current/voltage conv. DC	680	Ω	1 %	0.1 W
1	C_{ITAC}	AC separation on IT	680	nF	10 %	10 V
1	C1	Filtering of internal positive supply voltage	47	nF	10 %	10 V
1	C2	VS supply filtering[1)]	100	nF	10 %	50 V
1	C6	Switching frequency setting	82	pF	5 %	50 V
1	QSW	Switching transistor (pnp)	–	–	–	Zetex ZX5T955Z or equivalent
(1)	QSW	Alternative switching transistor (pMOS)	–	–	–	Int. Rectifier IRF 6216 or equiv.
1	R1	Current limitation	270	mΩ	5 %	0.5 W
1	R2	Base-emitter / gate-source discharge resistor	180 47	Ω kΩ	5 % 5 %	pnp pMOS
1	R4[2)]	DC base current limitation	390	Ω	5 %	0.1 W
1	C3[2)]	Base current highpass	10	nF	10 %	50 V
1	R3	Damping of overshoots	100	Ω	5 %	0.1 W
1	C4	Damping of overshoots	330	pF	10 %	100 V
1	L	DC/DC inductor	68	µH	20 %	I_{peak} = 1 A, e.g. EPCOS B82472-G6683-M
1	D	DC/DC diode	–	–	–	100 V, 1 A, e.g. ES1C
1	C	DC/DC capacitance	1	µF	10 %	100 V, low ESR, e.g. ceramic X7R
1	R8	Output voltage divider	715	kΩ	1 %	0.1 W
1	R10	Output voltage divider	18	kΩ	1 %	0.1 W
1	R7	Smoothing of VN transients	470	kΩ	5 %	0.1 W
1	C8	Smoothing of VN transients	22	pF	10 %	100 V
1	R6	VN filtering	20	Ω	5 %	0.5 W
1	C7	VN filtering	1	µF	10 %	100 V
1	L_{EMC}	Optional EMC filtering in noisy environment	150	µH	20 %	e.g. EPCOS B82432-T1154-K
1	R9	Error amplifier loop filter	470	kΩ	5 %	0.1 W
1	C9	Error amplifier loop filter	120	pF	10 %	50 V
1	C10	Error amplifier loop filter	82	pF	10 %	50 V

1) Total VS blocking capacitance must be chosen to fulfill the minimum voltage requirements even under worst-case conditions

2) Only with pnp solution

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	VS	- 0.4		50	V	
Total supply voltage	VS - VN			150	V	
Ground voltage difference		- 0.4		0.4	V	
Junction temperature	T_j			150	°C	
ESD voltage, all pins				500	V	SDM[1)]
				1	kV	HBM[1)]

1) EOS/ESD Assn. Standard DS5.3-1993.

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

4.2 Operating Range

Table 7 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	VS	9		40	V	With pMOS switch
		9		20	V	With pnp switch
Generated battery voltage	VN	- 130		- 15	V	
Total supply voltage	VS - VN			150	V	
Voltage at IT	V_{IT}	- 0.4		3.5	V	
Input range V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}	V_{ACDC}	0		3.3	V	
Ambient temperature	T_{amb}	- 40		85	°C	
Junction temperature	T_J			125[1)]	°C	

1) Operation up to T_J = 150 °C possible. However, a permanent junction temperature exceeding 125 °C could degrade device reliability.

Table 8 Thermal Resistances

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal Resistance junction to ambient P-/PG-DSO-24-8	$R_{th, jA}$	–	50	–	K/W	
Thermal Resistance junction to ambient P-/PG-TQFP-48-1	$R_{th, jA}$	–	50	–	K/W	

4.3 Electrical Parameters

Minimum and maximum values are valid within the full operating range.

Testing is performed according to the specific test figures at V_S = 12 V.

Functionality and performance is guaranteed for T_A = 0 to 70 °C by production testing. Extended temperature range operation at –40 °C < T_A < 85 °C is guaranteed by design, characterization and periodically sampling and testing production devices at the temperature extremes.

4.3.1 Supply Current and Power Dissipation

Table 9 Supply Currents (I_R = I_T = 0)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VN current Onhook	$I_{N,OH}$	–	3.8	4.5	mA	
VN current Active	$I_{IN,ACT}$	–	4	4.7	mA	Mode: ACT(R)
	$I_{IN,ACT-C}$	–	4.7	5.5	mA	Mode: ACT-C
VS current Power Down	$I_{S,PD}$	–	0.6	1	mA	
VS current Onhook	$I_{S,OH}$	–	5.6	7	mA	
VS current Active	$I_{S,ACT}$	–	6	7.5	mA	

Power Considerations

As with any SLIC, the total power P_{VN} from the generated battery supply voltage VN consists of the quiescent power P_Q due to the SLIC bias currents (see **Table 9**) and additional power resulting from any DC line current $I_{L,DC}$. This component P_L obviously consists of a part P_O dissipated in the SLIC's output stage and the load power P_{load} (load R_L including loop resistance and protection resistors).

$$P_{VN} = P_Q + P_L = P_Q + P_O + P_{Load} \quad (13)$$

Table 10 summarizes the calculation of these power components in the different operating modes.

Table 10 Calculation of VN Power Components

Mode	Load	VN [V]	P_Q [mW]	P_O [mW]	P_{Load} [mW]
ONHK	open	- 50	50 * $I_{N,OH}$	0	0
ACT	R_L	- (R_L*$I_{L,DC}$+V_{drop1})	- VN * $I_{IN,ACT}$	V_{drop1} * $I_{L,DC}$	R_L*($I_{L,DC}$)^2
ACT-T	R_L	- (R_L*$I_{L,DC}$+V_{drop2})	- VN * $I_{IN,ACT}$	V_{drop2} * $I_{L,DC}$	R_L*($I_{L,DC}$)^2
ACT(R)[1]	ringer equiv. Z = R_L + 1/jωC = $Z_L e^{i\varphi}$	tracking supply: VN(t) = - |V_{Rng}(t) + V_{DC}| - V_{drop1}	- 2/π * VN_p * $I_{IN,ACT}$	2/π * $V_{Rng,p}$ / Z_L * V_{drop1}	($V_{Rng,p}$)^2 * cos φ / (2*Z_L)
ACT-C[1]		- 75	75 * $I_{IN,ACT-C}$	75 * 2/π * $V_{Rng,p}$ / Z_L - P_{Load}	($V_{Rng,p}$)^2 * cos φ / (2*Z_L)

1) Sinusoidal ringing with peak ring voltage $V_{Rng,p}$ and DC voltage V_{DC}; power values are time averages.

The power dissipation of the DC/DC control circuits P_S = I_S * V_S adds to the on-chip power to yield the total SLIC power dissipation

$$P_{SLIC} = P_Q + P_O + P_S \quad (14)$$

In **Table 11** on-chip power dissipation examples are calculated using the formulae of **Table 10** for typical application conditions ($I_{L,DC}$ = 25 mA, R_L = 400 Ω; sine wave ringing @ 20 Hz, 45 V_{rms}, 3 US-REN; VS = 12 V). Note that on-chip power dissipation is significantly reduced by utilizing the quasi-balanced ring concept.

Table 11 Typical SLIC On-chip Power Dissipation

Mode	Load	- VN [V]	P_Q [mW]	P_O [mW]	P_S [mW]	P_{SLIC} [mW]
ONHK	Open	50	190	0	70	260
ACT	400 Ω	18	72	200	75	350
ACT-T	400 Ω	21	84	275	75	435
ACT(R)	400 + 2300 Ω, 24 µF (3REN)	70 V_{peak}	178	115	75	370
ACT-C		75	350	385	75	810

Now the power required from the VS supply, P_{VS}, can be calculated. Obviously VS has to deliver the total VN power P_{VN}, i.e. the sum of the components in **Table 10**, plus all the losses arising from DC/DC conversion, P_{Loss}. These include the SLIC's current consumption from VS and the losses in the external converter parts (switch transistor, inductor, capacitor and diode). Thus

$$P_{VS} = P_{VN} + P_{Loss} = P_{VN} / \eta \quad (15)$$

This can be regarded as a definition of efficiency η. As P_{Loss} includes some nearly constant components (e.g. SLIC bias current, switching losses), the efficieny depends on power, degrading at low P_{VN} values. Furthermore it depends on the switch transistor type (pnp vs. pMOS) and the switching frequency. Typical efficiency measurement results have been given in **Figure 9**.

It should be pointed out, that the instantaneous power dissipation during ringing varies over the ring period. The relations given in **Table 10** apply for the average power, that together with efficiency determines the power/current requirements on the VS supply (see **Table 12**). However, when dimensioning the DC/DC components, the maximum power values with respect to the switching cycle have to be taken into account. For sinusoidal ring voltages they differ from the average values by a factor of 2 and π/2, respectively. **Table 12** contains both average and peak ring power values.

Table 12 Typical Power Supply Values

Mode	Load	P_{Load} [mW]	P_{VN} [1)] [mW]	Efficiency	P_{VS} [mW]	IS_{avg} [mA]
ONHK	Open	0	190	0.50	380	32
ACT	400 Ω	250	520	0.58	900	75
ACT-T	400 Ω	250	610	0.60	1015	85
ACT(R)	400 + 2300 Ω, 24 µF (3REN)	730 avg 1460 peak	1020 avg 1850 peak	0.63	1620	135
ACT-C		730 avg 1460 peak	1465 avg 2075 peak	0.66	2220	185

1) = $P_Q + P_O + P_{Load}$ (**Table 12**)

With the application specific maximum P_{VN} power values known, the DC/DC inductance L can be chosen according to the guidelines of **Chapter 2.3**. Then the important peak current I_p, that will be reached during the conversion cycle, can be calculated from **Equation (6)**

$$I_p = \sqrt{2P_{VN,max} / (\eta \cdot L \cdot f_{SW})} \quad (16)$$

As an example, with a 68 µH inductor and the values of **Table 12**, the peak current from VS will be in the 1 A range.

4.3.2 DC Characteristics (V_{ACP} = V_{ACN} = 1.5 V)

Table 13 Line Termination TIP, RING

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DC line voltage active (open loop)	$V_{TR, DC}$	-0.6		0.6	V	V_{DCP} = V_{DCN} = 1.5 V
		31.2	32	32.8	V	V_{DCP} – V_{DCN} = 0.8 V
		-32.8	- 32	-31.2	V	V_{DCP} – V_{DCN} = -0.8 V
Onhook line voltage	V_{TR}	42	45	–	V	V_{DCP} = V_{DCN} = 1.5 V
Output current limit	$\|I_{R, max}\|$, $\|I_{T, max}\|$	80	95	110	mA	T_{amb} = 25°C[1)] Mode: ACT-x, ONHK, HIR, HIT
High impedance output leakage current	$I_{Leak,R}$		20	40	µA	VN < V_R < 0 Mode: HIR, HIRT
	$I_{Leak,T}$		20	40	µA	VN < V_T < 0 Mode: HIT, HIRT

1) The typical temperature dependence of the output current limits is - 0.3 % / °C.

Table 14 DC/DC Converter Output Voltage VN

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VN range	–	-130		-15	V	Mode: ACT-x
Signal headroom	V_{drop1}		8		V	Mode: ACT
	V_{drop2}		11		V	Mode: ACT-T
DC/DC converter output voltage	VN	-20	-18	-16	V	V_{DCP} – V_{DCN} = 0.25 V Mode: ACT
		-23	-21	-19	V	V_{DCP} – V_{DCN} = 0.25 V Mode: ACT-T
		-78	-75	-72	V	Mode: ACT-C
		-52.5	-50	-47.5	V	Mode: ONHK

Table 15 Inputs DCP, DCN, ACP, ACN, Output IT

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current DCP, DCN	I_{DC}	–	0.1	–	µA	
Differential AC-Input resistance ACP, ACN	R_{AC}	–	10	–	kΩ	
IT output current	I_{IT}	-15	0	15	µA	I_R = I_T = 0 mA
		380	400	420	µA	I_R = I_T = 20 mA
		-420	-400	-380	µA	I_R = I_T = -20 mA

Table 16 Control Inputs C1, C2, C3

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
H-input voltage	V_{IH}	2.7		3.6	V	–
M-input voltage	V_{IM}	1.2		2.1	V	C1, C2 only
L-input voltage	V_{IL}	–0.3		0.6	V	–
Input leakage current	I_{Leak}		5	10	µA	–
Thermal overload current C1	I_{therm}	120	150	250	µA	V_{C1} = 1.20 V Mode: ACTx, HIx

4.3.3 AC Characteristics

Table 17 AC Characteristics TIP, RING

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Receive gain	G_r	–	6.0	–	–	Tip / Ring open loop[1], $V_{ACP} - V_{ACN}$ = 640 mV_{rms}, f = 1015 Hz
Total harmonic distortion V_{TR}	THD	–	0.01	0.1	%	$V_{ACP} - V_{ACN}$ = 640 mV_{rms}, f = 1015 Hz
Teletax distortion (Mode ACT-T)	$THDTTX$	–	0.02	0.1	%	$V_{TR,AC}$ = 3 V_{rms}, f = 16 kHz, R_L = 200 Ω $I_{Trans,DC}$ = 25 mA
	$THDTTX_0$	–	0.1	0.2	%	$I_{Trans,DC}$ = 0
Psophometric noise	N_{pVTR}	–	-85	-82	dBmp	
Longitudinal to transversal rejection ratio V_{long}/V_{TR}	$LTRR$	–	70	–	dB	V_{long} = 3 V_{rms}, 300 Hz < f < 3.4 kHz
Longitudinal to transversal rejection ratio V_{long}/V_{TR} (loop) (see **Figure 13**	$LTRR_{loop}$	t.b.d.	60	–	dB	300 Hz < f < 1 kHz
		t.b.d.	60	–	dB	f = 3.4 kHz
Onhook longitudinal to transversal rejection ratio V_{long}/V_{TR} (loop)	$LTRR_{onhk}$		48		dB	300 Hz < f < 3.4 kHz, I_{DC} = 0
Transversal to longitudinal rejection ratio V_{TR}/V_{long}	$TLRR$	40	50	–	dB	300 Hz < f < 3.4 kHz
Power supply rejection ratio VS/V_{TR}	$PSRR$	50	60	–	dB	$V_{SupplyAC}$ = 100 mV_p, 300 Hz < f < 3.4 kHz
VN/V_{TR}		40	60	–	dB	
Ringing amplitude at TIP/RING	V_{RNG}	62	64	66	V_{rms}	R_R = 2300 Ω, C_R = 24 µF, f = 20 Hz, $V_{DCP} - V_{DCN}$ = 0.15 V (DC) + 1.6 V_{rms} (sine wave)
Ringing distortion	–	–	0.1	–	%	

1) In closed loop operation the internal sense resistors of 2 * 10 Ω have to be taken into account.

Note: If not otherwise stated, AC characteristics are tested at a DC line current of 25 mA in active mode; load resistor R_{Load} is 600 Ω..

Table 18 AC Characteristics IT

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Transversal current ratio	$1/G_{IT}$	49.5	50	50.5	–	$V_{ACP} - V_{ACN}$ = 640 mV_{rms}, f = 1015 Hz
Total harmonic distortion V_{IT}	THD_{IT}	–	0.01	0.2	%	$I_{Trans,DC}$ = 25 mA, $V_{ACP} - V_{ACN}$ = 640 mV_{rms}, f = 1015 Hz
Psophometric noise	N_{pVIT}	–	-112	-105	dBmp	
Longitudinal to transversal current output rejection ratio	$LITRR$	t.b.d.	85	–	dB	V_{long} = 3 V_{rms} 300 Hz < f < 1 kHz
V_{long}/V_{IT}		t.b.d.	85	–	dB	f = 3.4 kHz
Power supply rejection ratio	$PSRR$					$V_{SupplyAC}$ = 100 mV_p, 300 Hz < f < 3.4 kHz
VS/V_{IT}		–	80	–	dB	
VN/V_{IT}		–	80	–	dB	

Note: These characteristics are valid for both DC line current directions (normal and reverse polarity).

Table 19 AC Characteristics DC/DC Converter

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switching frequency active	$f_{SW,act}$	–	100	–	kHz	COS = 82 pF[1]; T = 25°C[2]
Switching frequency onhook	$f_{SW,onhk}$	–	50	–	kHz	COS = 82 pF; T = 25°C[2]
Maximum switching frequency	$f_{SW,max}$	–	300	–	kHz	
Switch driver output slew rate	SR	–	50	–	V/µs	C_{Load} = 1 nF
SWD output voltage swing	ΔV_{SW}	–	8	10	V	
Maximum SWD output voltage duty cycle	D	–	90	–	%	
Switch transistor current limit reference voltage[3]	$V_{lim,ref}$	–	400	–	mV	
Oscillator charging current						
positive direction	$I+$	–	30	–	µA	
negative direction	$I-$	–	-80	–	µA	
Oscillator threshold voltage						
positive	$V+$	–	5	–	V	
negative	$V-$	–	3	–	V	

1) Dependency on COS see **Figure 11**

2) The typical temperature dependence of f_{SW} = -0.1 kHz / °C.

3) Effective value for typical application at 100 kHz: $I_{p,max} < V_{lim,ref}$ / R1; differs from static value.

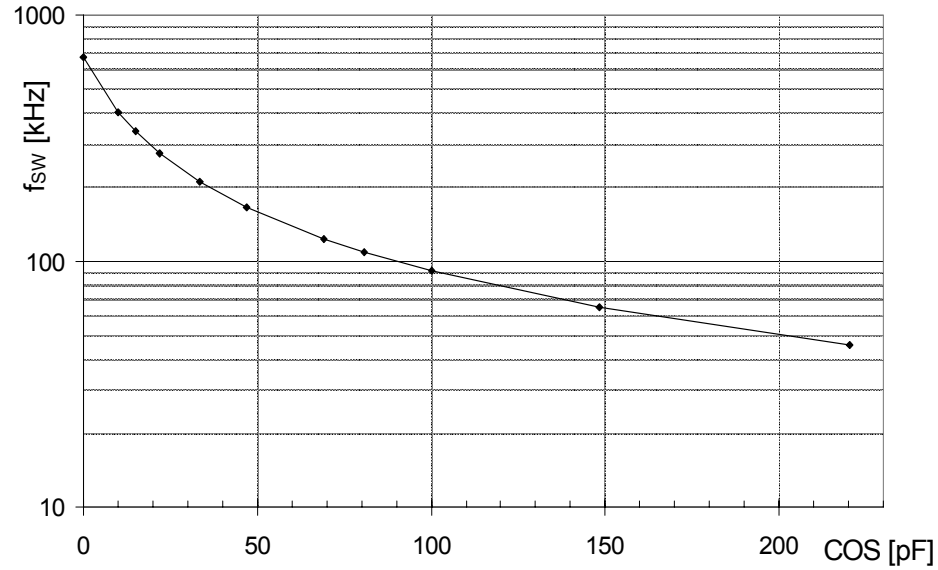


Figure 11 Oscillator Frequency vs. Capacitance at COS

5 Test Figures

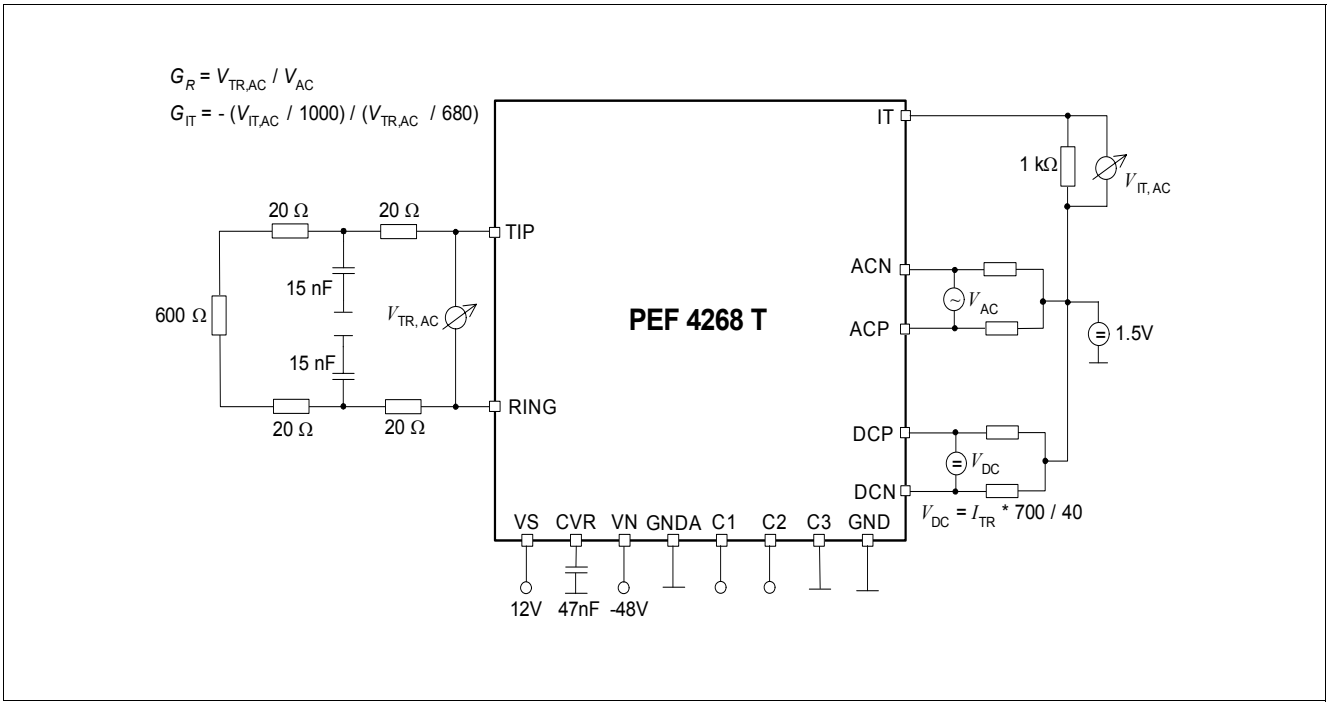


Figure 12 Transmission Characteristics

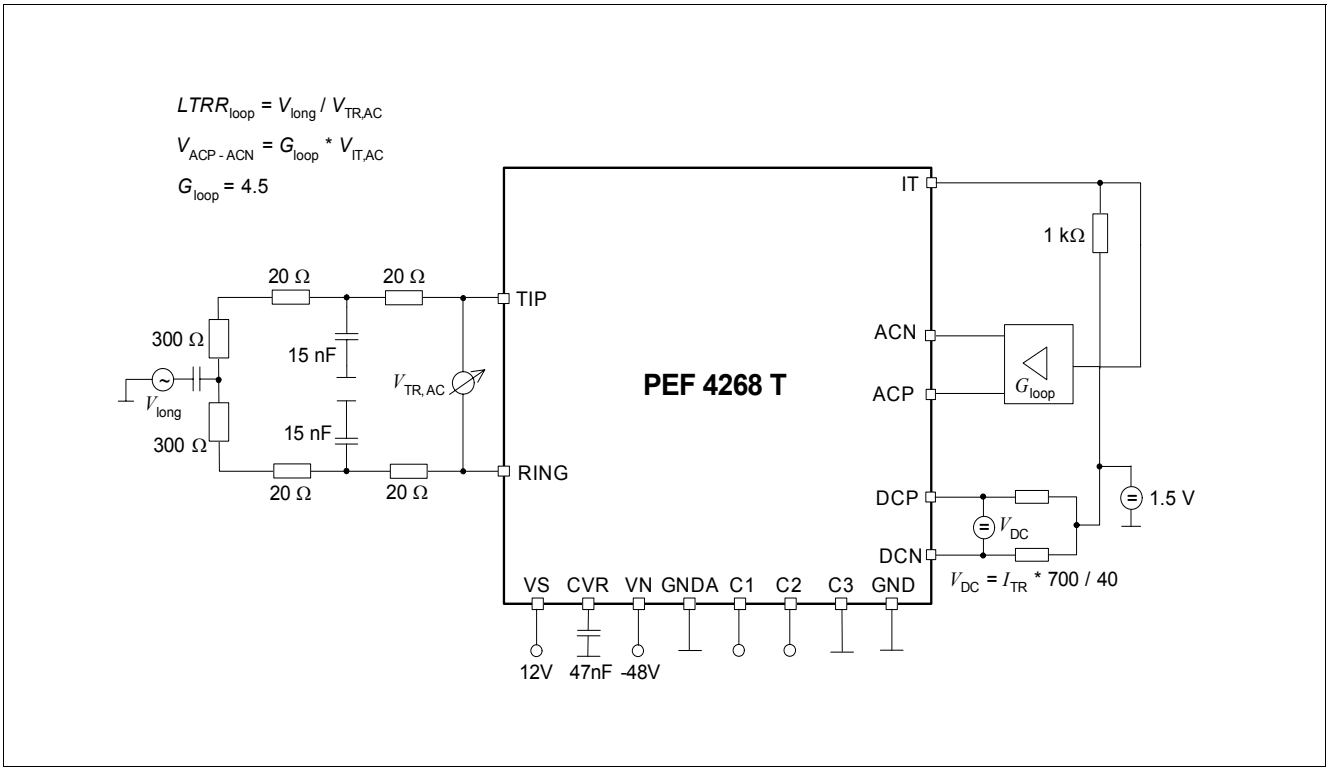
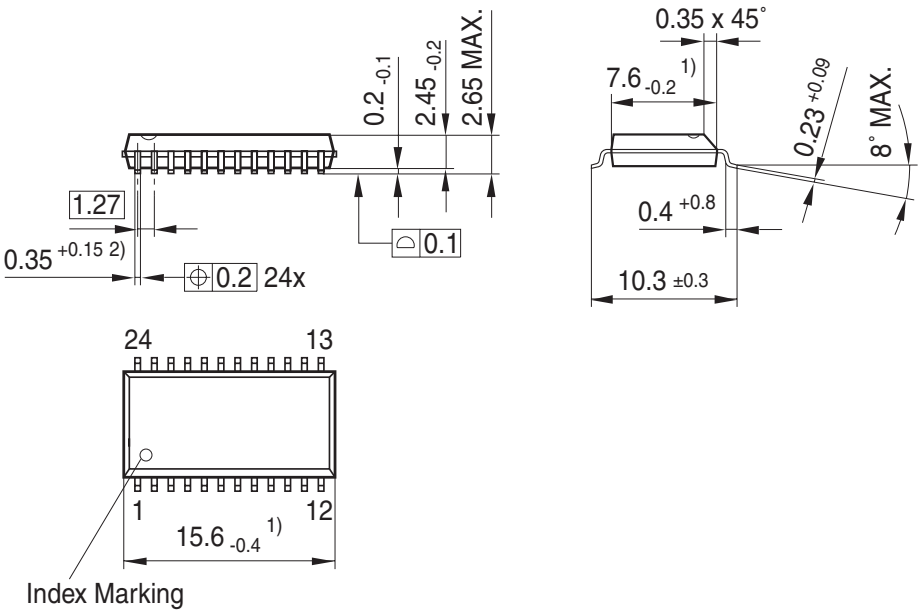


Figure 13 Longitudinal to Transversal Rejection Loop

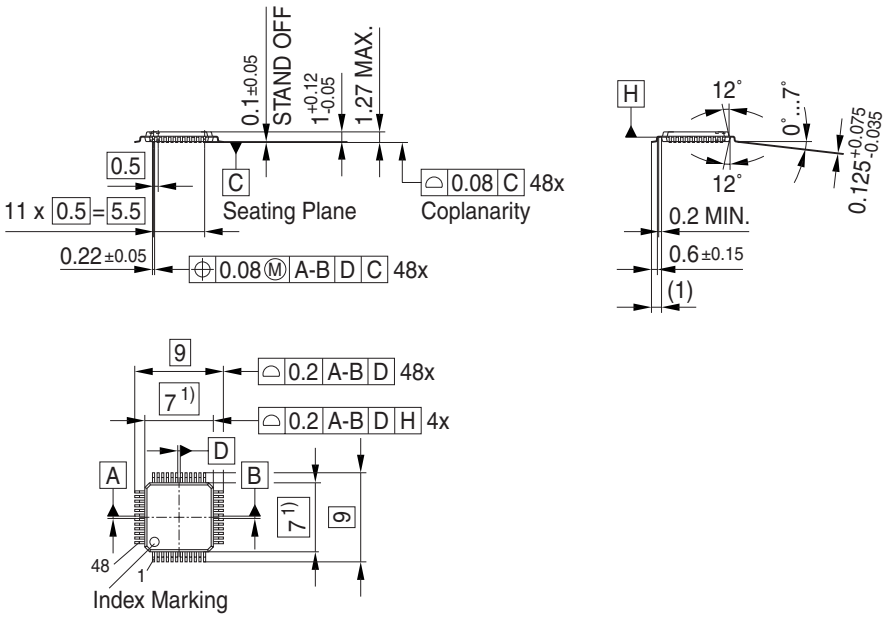
6 Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Lead width can be 0.61 max. in dambar area

Figure 14 P-/PG-DSO-24-8 (Plastic/Plastic Green Dual Small Outline Package)

Note: Dimensions in mm.



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPP05612

Figure 15 P-/PG-TQFP-48-1 (Plastic/Plastic Green Thin Quad Flat Package)

Note: Dimensions in mm.

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