

VINETIC[®]-2CPE/-1CPE

Voice and Internet Enhanced Telephony Interface
Circuit

VINETIC[®]-2CPE, PEB 3332, Version 2.1

VINETIC[®]-1CPE, PEB 3331, Version 2.1

CONFIDENTIAL
Distribution with NDA only

Communications



N e v e r s t o p t h i n k i n g .

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Preface

This Preliminary Data Sheet describes the VINETIC®-2CPE/-1CPE, a member of the Voice and Internet Enhanced Telephony Interface Circuit (VINETIC®) chip set family. The VINETIC®-2CPE/-1CPE includes two/one analog lines connected via two/one single-channel SLIC chips.

To simplify matters, the following synonyms are used:

VINETIC®-x:

Synonym used for the CODEC versions VINETIC®-2CPE/-1CPE.

SLIC:

Synonym used for the SLIC-DC Version 1.2.

Organization of this Document

This document is divided into 6 chapters. It is organized as follows:

- **Chapter 1**
A general description of the chip set, key features/requirements, and typical applications.
- **Chapter 2**
Pin layout and pin description.
- **Chapter 3**
Description of clocking, reset behavior, and test modes.
- **Chapter 4**
Parallel (Intel, Motorola) and serial interfaces (PCM, SCI/SPI).
- **Chapter 5**
Parameters, symbols, and limit values.
- **Chapter 6**
Illustrations and dimensions of the package outlines.
- **Terminology**
List of abbreviations and descriptions of symbols.

1 Family Overview

The VINETIC® family of devices is designed for accessing analog telephone lines. VINETIC® devices are available in different granularity (0, 1, 2, 4 and 8 analog voice channels) and with different levels of DSP performance (CPE, VIP, M, C, S). Their seamless connection to a broad range of SLICs provides the most effective solution for each application.

Executive Summary

The VINETIC® family integrates the necessary DSP and RAM/ROM for voice processing into the CODEC/SLIC chip set, thereby offering a unique set of features for Voice over Packet (VoP):

- **Cost and board space reduction** - CODEC, DSP and RAM/ROM are integrated into one small package, significantly reducing cost and board space required.
- **Scalability** - VINETIC® supports each voice channel with the necessary amount of DSP performance, due to the encapsulation of CODEC and DSP.
- **Flexibility** - The VINETIC® family provides one to eight analog ports and various levels of DSP performance, while remaining pin-compatible (only for four or eight channels, respectively) and softwarecompatible.
- **World-wide usage** - The VINETIC® can be adapted to different country requirements without hardware changes (AC and DC path, ringing, metering, etc. are programmable).
- **Future-proof** - The integrated RAM (VINETIC®-4VIP, VINETIC®-2CPE/-1CPE) for downloading advanced CODECs or its own DSP software guarantees that the system will retain state-of-the-art technology and permit future remote updates.
- Designed for Voice over Packet (**VoIP, VoDSL, Packetcable, VoATM**).

(not all features are available in all VINETIC® versions)

Voice and Internet Enhanced Telephony Interface Circuit VINETIC®-2CPE/-1CPE

PEB 3332
PEB 3331

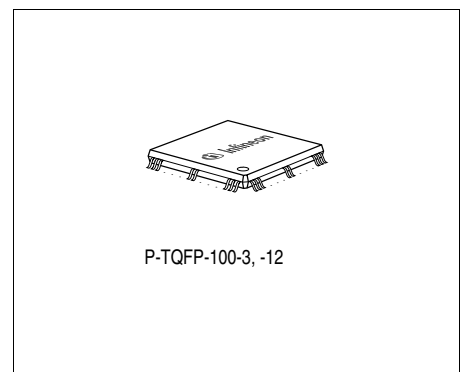
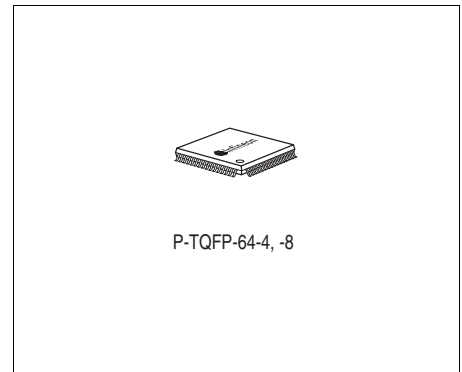
Version 2.1

1.1 Features VINETIC®-2CPE/-1CPE

- Fully programmable 2- and 1-channel CODEC with enhanced signal-processing capabilities
- Glueless interface to the Infineon SLIC-DC Version 1.2

1.1.1 Integrated DSP Features

- Integrated VoIP DSP with RAM and software download capability
- Enhanced signal processing
- Voice coding: G.711, G.711 Annex I (Packet Loss Concealment), G.711 Annex II (VAD + CNG), G.723.1, G.726, G.729 A, B, G.729 E, iLBC royalty free vocoder
- 4(2) VoIP channels with low-bitrate vocoding implemented in VINETIC®-2CPE (VINETIC®-1CPE)
- RTP/RTCP packetization (packetization time programmable: 5 to 30 ms encoding, 5 to 60 ms decoding)
- Voice Activity Detection (VAD)
- Comfort Noise Generation (CNG)
- Algorithms for Line Echo Cancellation (LEC) exceeding G.165, G.168, G.168-2002/2004: Near End Line Echo Cancellation (NLEC) up to 16 ms tail length or Windows-Based Line Echo Cancellation up to 128 ms tail length
- Integrated DTMF generator
- Integrated DTMF decoder
- Integrated Caller ID (with Frequency Shift Keying (FSK)) generator according to V.23 and Bell 202
- Integrated fax/modem detection, In-band tone detection
- Multi-party conferencing
- T.38 Fax relay support with V.17, V.21, V.27ter, V.29
- Voice play-out (reordering, fixed and adaptive jitter buffer up to 200 ms, clock synchronization)
- Compliant with packet cable specification
- Universal Tone Generator (UTG) including all Japanese tones
- Call Progress Tone Detector
- Caller-ID Detector for V.23 and Bell 202



Product Name	Product Type	Package
VINETIC®-2CPE/-1CPE	PEB 3332 F/-3331 F	PG-TQFP-64-8
	PEB 3332 HT/-3331 HT	PG-TQFP-100-3, PG-TQFP-100-18

1.1.2 CODEC/SLIC Features

- Specification in accordance with ITU-T Recommendation Q.552 for interface Z and ETSI TS 102 971 V1.1.1
- Internal ringing capability
- Sinusoidal ringing
- Loop start signaling
- Polarity reversal
- Automatic modes for POTS signaling
- Line Testing according to Telcordia GR-909-CORE
- On-hook transmission
- Direct connection of DAA solution possible (FXO)

1.1.3 Interface Features

- PCM interface with one PCM highway
- Serial control interface, SCI (Infineon) compatible, SPI compatible
- Parallel host interface: Intel/Motorola compatible
- JTAG interface for boundary scan

1.2 Typical Applications

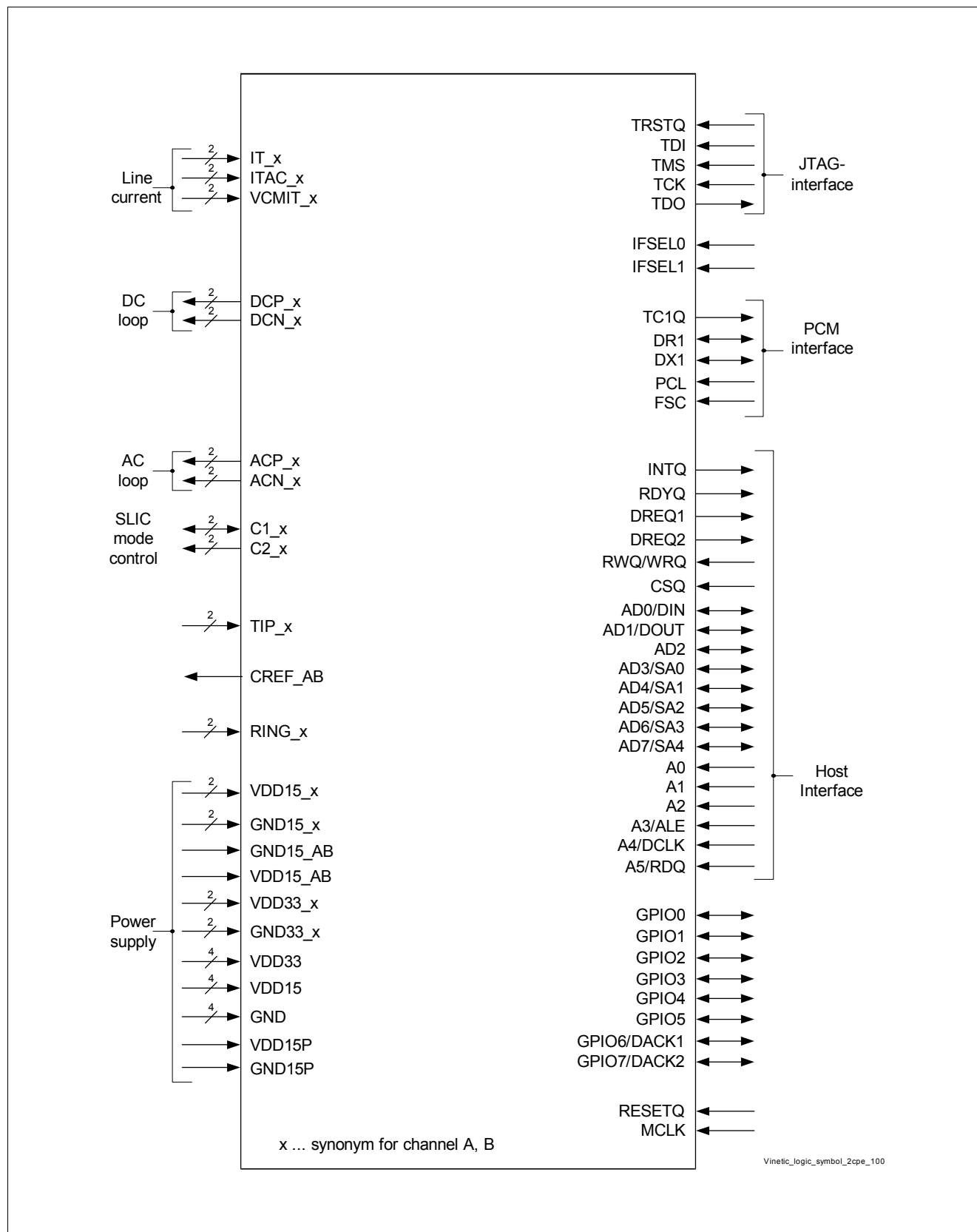
The VINETIC®-2CPE/-1CPE and SLIC-DC system is dedicated primarily to Customer Premises Equipment (CPE) and provides solutions for the following applications:

Access network:

- FTTH - TDM, VoIP
- WLL - TDM, VoIP

CPE:

- Residential Gateway/Home Gateway/Internet Telephony Gateway (ITG) - VoIP
- Integrated Access Device (IAD) - VoIP
- Cable Modems/Media Terminal Adapter (MTA) - VoIP
- Analog Telephony Adapter (ATA) - VoIP
- Router - VoIP
- SOHO IP PBX


Figure 1 Logic Symbol for VINETIC®-2CPE (PG-TQFP-100-3 and PG-TQFP-100-18)

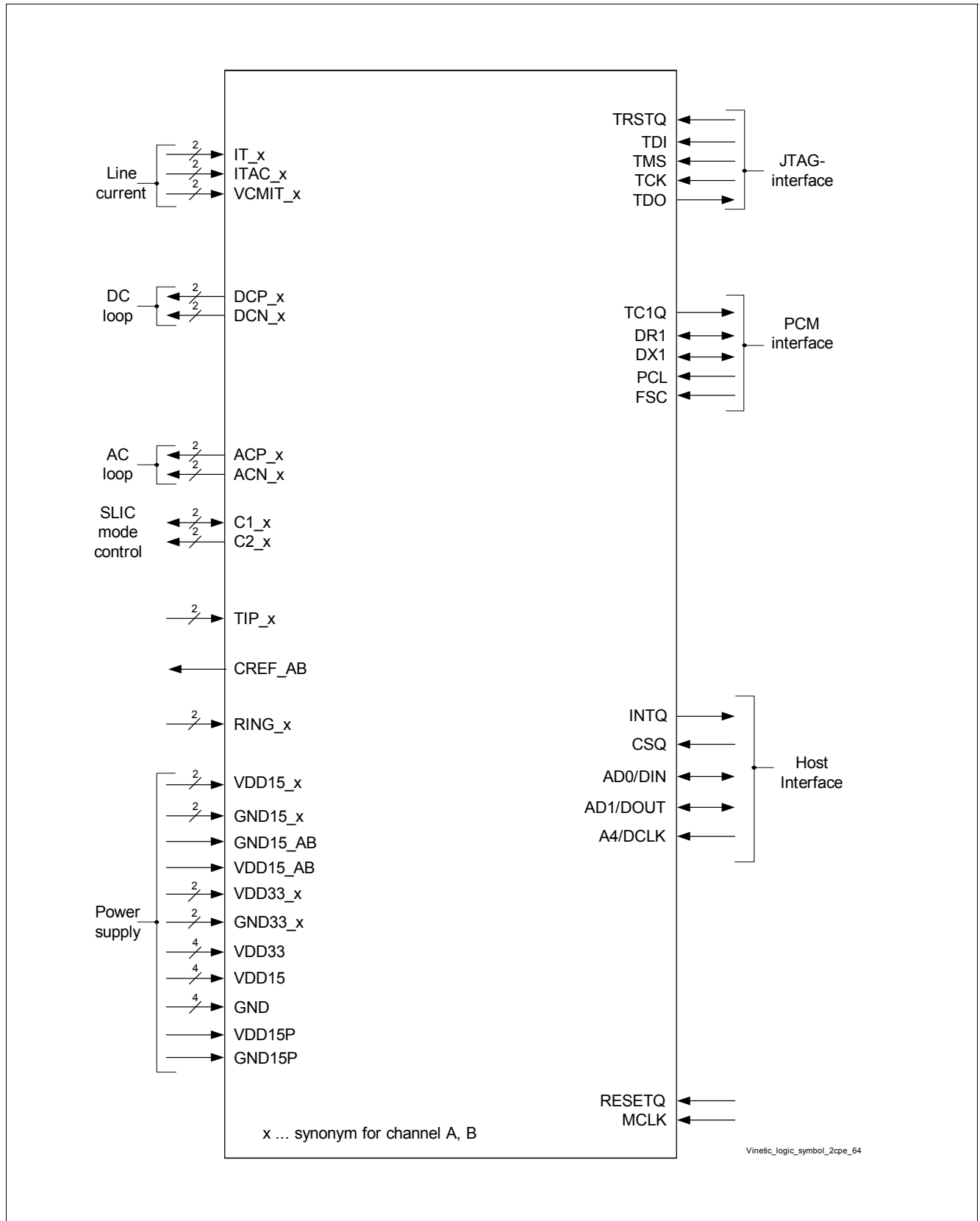


Figure 2 Logic Symbol for VINETIC®-2CPE (PG-TQFP-64-8)

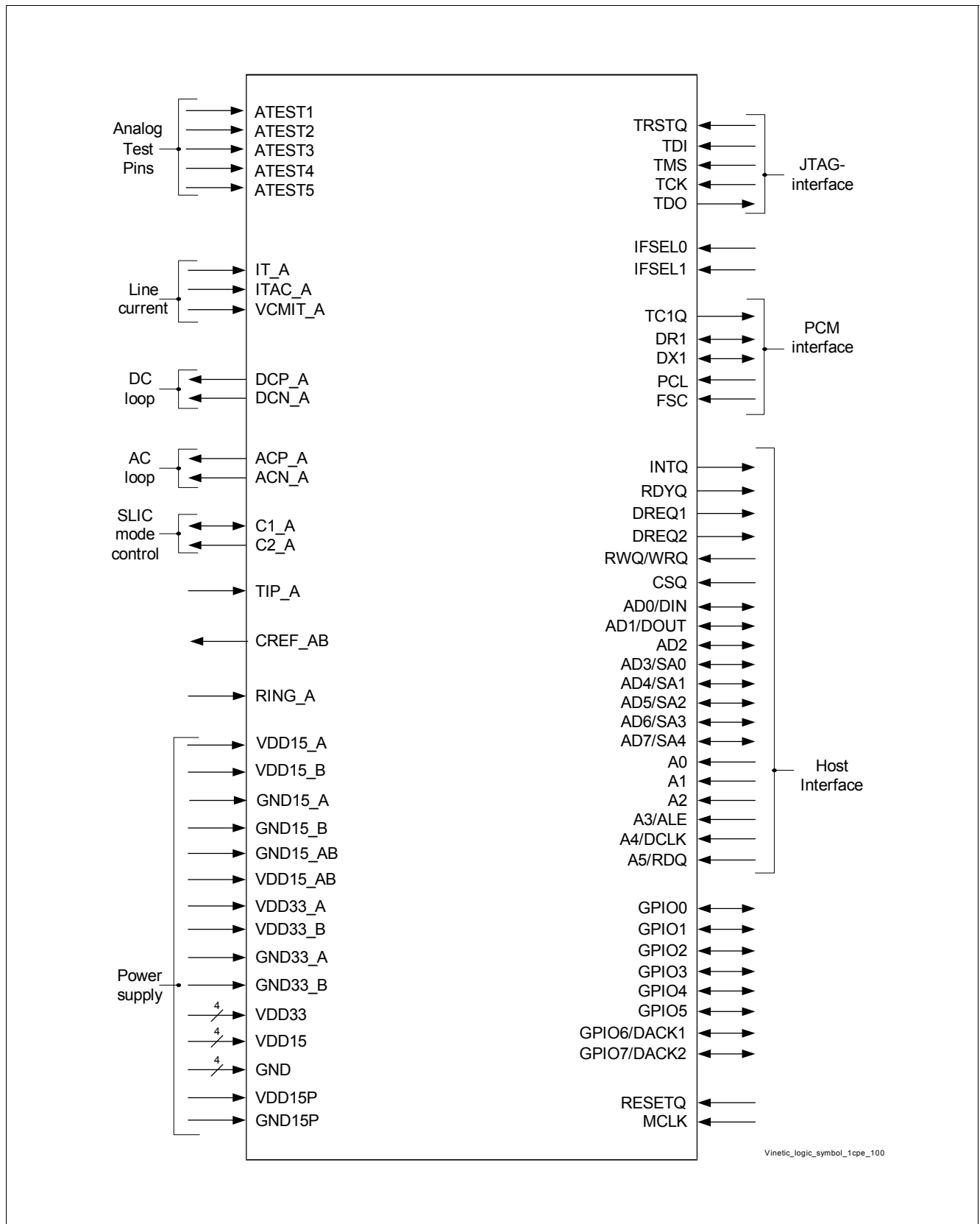


Figure 3 Logic Symbol for VINETIC®-1CPE (PG-TQFP-100-3 and PG-TQFP-100-18)

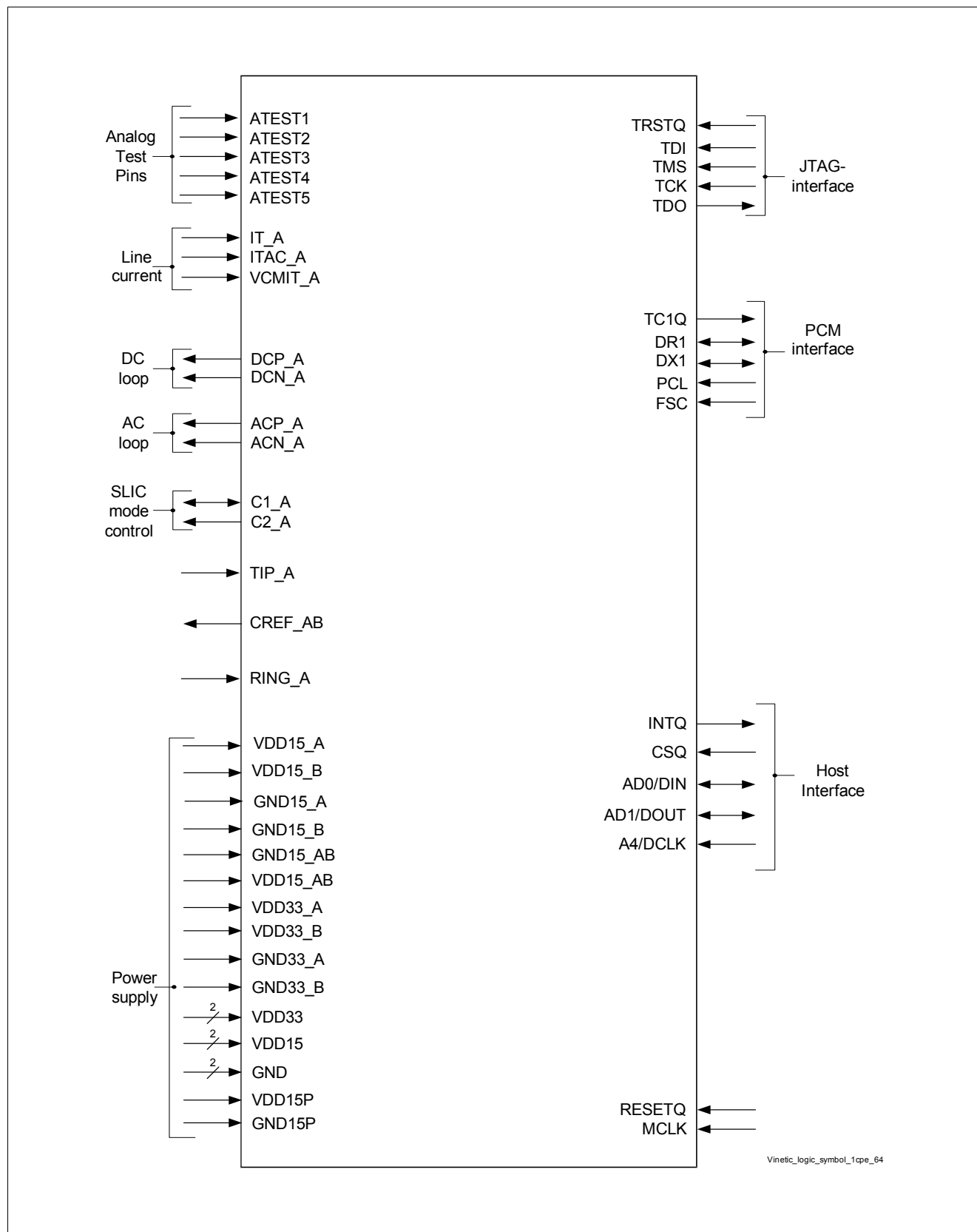


Figure 4 Logic Symbol for VINETIC®-1CPE (PG-TQFP-64-8)

2 Pin Description

2.1 VINETIC®-2CPE Pin Diagrams

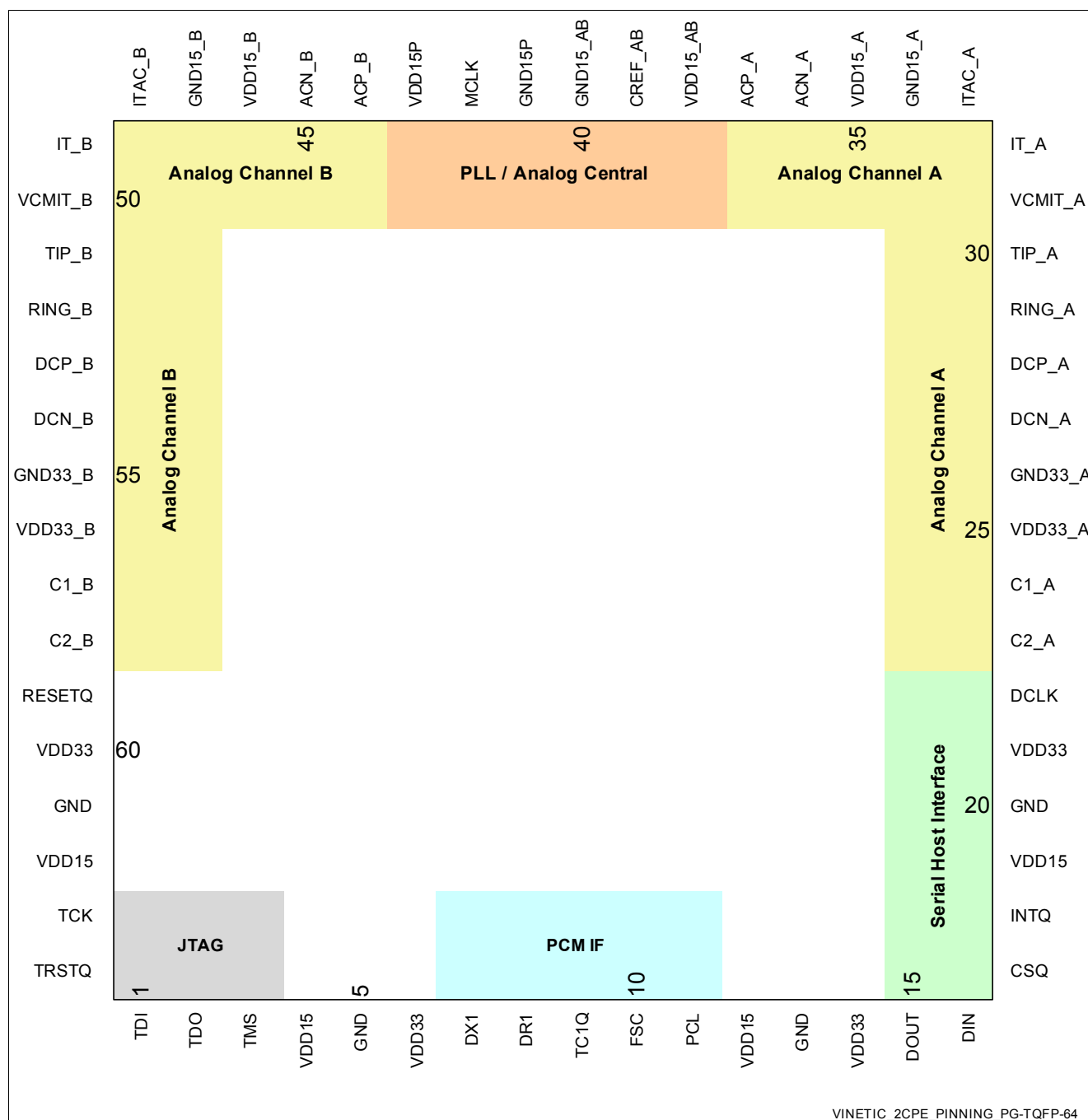


Figure 5 PG-TQFP-64-8 Pin Diagram (Top View) for VINETIC®-2CPE

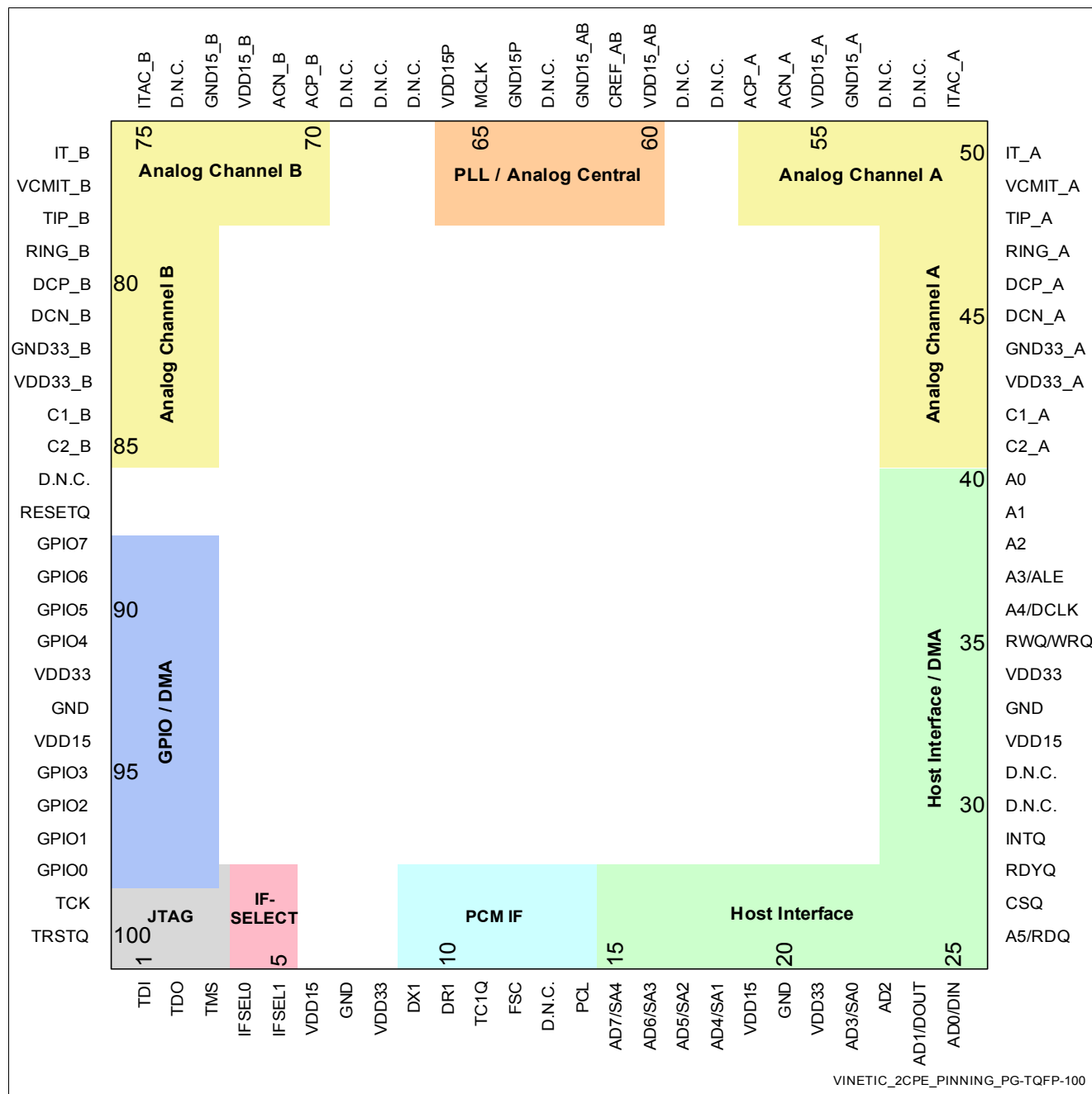


Figure 6 PG-TQFP-100-3 and PG-TQFP-100-18 Pin Diagram (Top View) for VINETIC®-2CPE

2.2 VINETIC®-1CPE Pin Diagrams

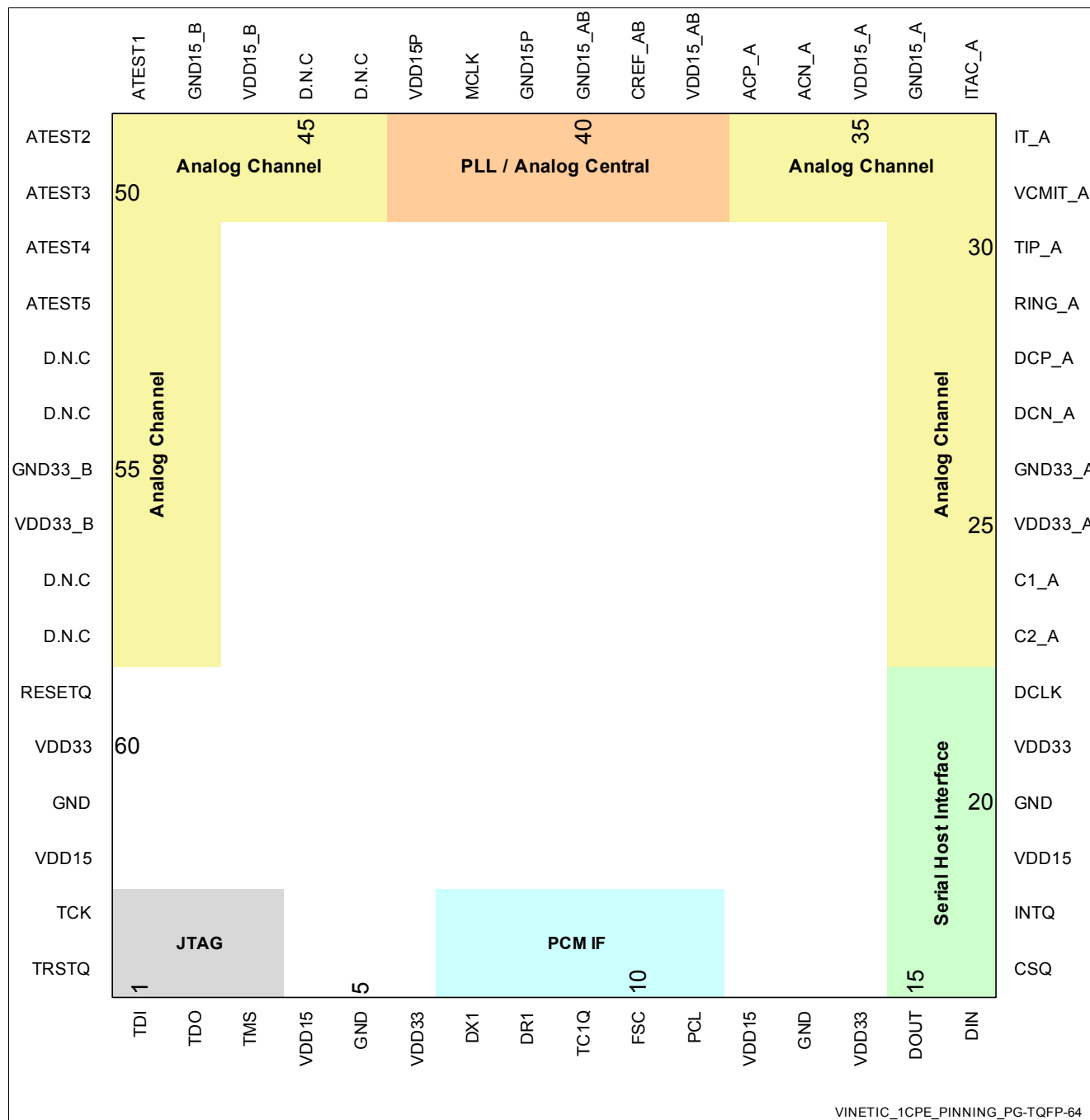


Figure 7 PG-TQFP-64-8 Pin Diagram (Top View) for VINETIC®-1CPE

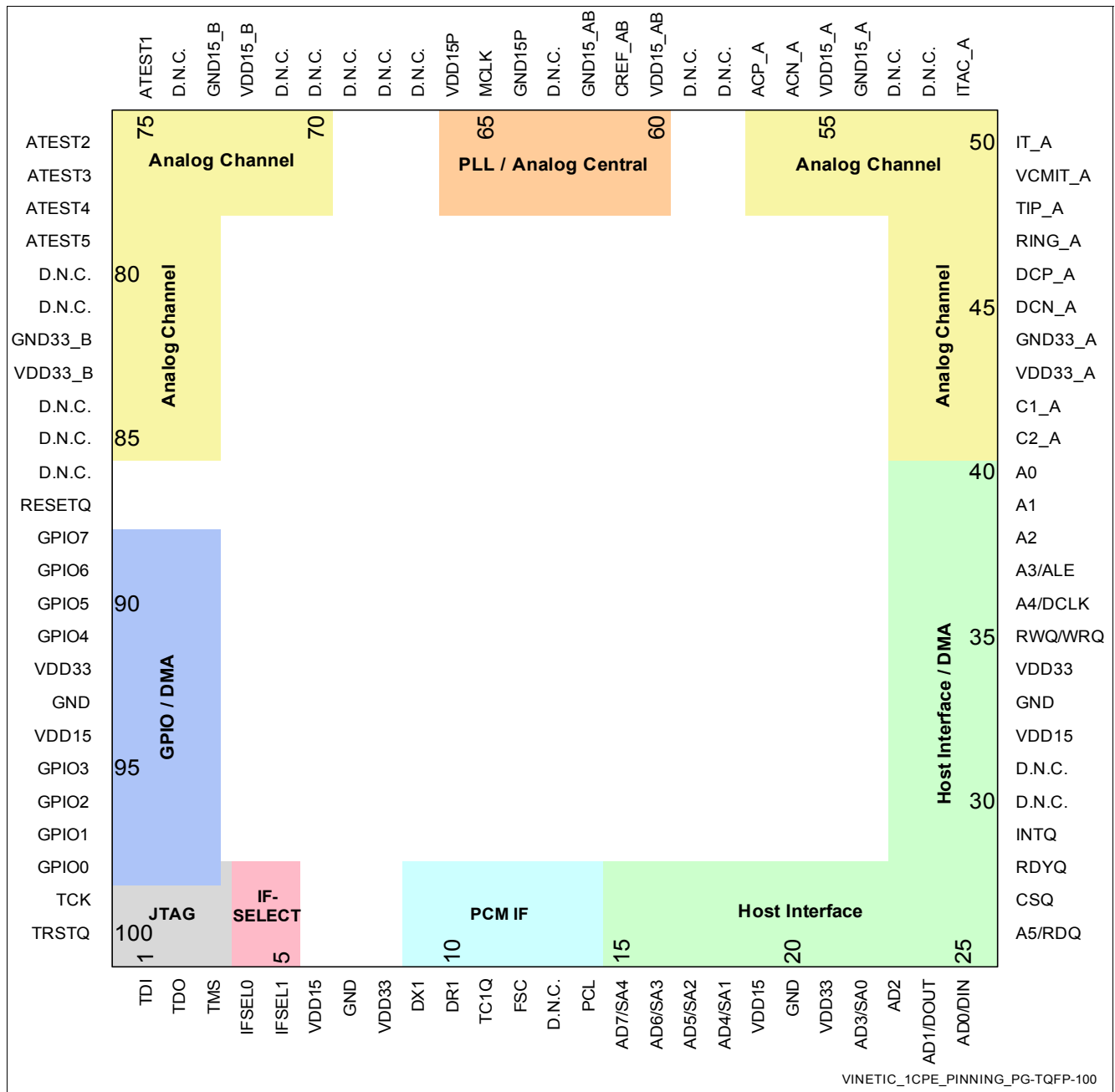


Figure 8 PG-TQFP-100-3 and PG-TQFP-100-18 Pin Diagram (Top View) for VINETIC®-1CPE

2.3 VINETIC®-2CPE Pins Sorted by Function

Table 1 Abbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or output. Analog levels.
PWR	Power
GND	Ground
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 2 Abbreviations for Buffer Type

Abbreviations	Description
PU	Pull-up
OD	Open-Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).

2.3.1 Common Pins for Analog Line Module (Channels A, B)

Table 3 Common Pins for Analog Line Module (Channels A, B)

Pin No.		Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Function
PG-TQFP-64-8	PG-TQFP-100-3/-18				
39	61	CREF_AB	AI/O	-	Connection to external capacitor for low-pass filtering of the reference voltage
40	62	GND15_AB	GND	-	Common ground for bias block
38	60	VDD15_AB	PWR	-	1.5 V power supply for bias

1) For explanation of abbreviations see [Table 1](#)

2) For explanation of abbreviations see [Table 2](#)

2.3.2 Pins for Analog Line Module (Channels A, B)

Table 4 Pins for Analog Line Module (Channels A, B)

Pin No.		Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Function
PG-TQFP-64-8	PG-TQFP-100-3/-18				
29 52	47 79	RING_A RING_B	AI	-	Analog input for measurement the voltage on ring line
30 51	48 78	TIP_A TIP_B	AI	-	Analog input for measurement the voltage on tip line
37 44	57 70	ACP_A ACP_B	AO	-	Differential two-wire AC output voltage controlling the RING/TIP pins at the SLIC
36 45	56 71	ACN_A ACN_B	AO	-	Differential two-wire AC output voltage controlling the RING/TIP pins at the SLIC
28 53	46 80	DCP_A DCP_B	AO	-	Differential two-wire DC output voltage controlling the RING/TIP pins at the SLIC
27 54	45 81	DCN_A DCN_B	AO	-	Differential two-wire DC output voltage controlling the RING/TIP pins at the SLIC
25 56	43 83	VDD33_A VDD33_B	PWR	-	3.3 V analog power supply
35 46	55 72	VDD15_A VDD15_B	PWR	-	1.5 V power supply
26 55	44 82	GND33_A GND33_B	GND	-	Analog ground 3.3 V
34 47	54 73	GND15_A GND15_B	GND	-	Analog ground 1.5 V
32 49	50 76	IT_A IT_B	AI	-	Transversal current input (AC + DC)
33 48	51 75	ITAC_A ITAC_B	AI	-	Transversal current input (AC)

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Pin Description
Table 4 Pins for Analog Line Module (Channels A, B) (cont'd)

Pin No.		Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Function
PG-TQFP-64-8	PG-TQFP-100-3/-18				
31 50	49 77	VCMIT_A VCMIT_B	AI	-	Reference pin for transversal/longitudinal current sensing
23 58	41 85	C2_A C2_B	AO	-	Ternary logic output controlling the SLIC operation mode
24 57	42 84	C1_A C1_B	AI/O	-	Ternary logic output controlling the SLIC operation mode; indicating thermal overload of a SLIC if a current of typically 150 µA is drawn out by the SLIC's C1 pin

1) For explanation of abbreviations see [Table 1](#)

2) For explanation of abbreviations see [Table 2](#)

2.3.3 General Pins

Table 5 General Pins

Pin No.		Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Function
PG-TQFP-64-8	PG-TQFP-100-3/-18				
59	87	RESETQ	I	-	Hardware reset for the whole chip (low active)
42	65	MCLK	I	-	Master clock for the PLL input. The MCLK clock can vary from 512 kHz to 8192 kHz in multiples of 512 kHz. This pin must be directly connected to PCL.
–	13, 30, 31, 52, 53, 58, 59, 63, 67, 68, 69, 74, 86	D.N.C.	NC	-	Do not connect

1) For explanation of abbreviations see [Table 1](#)

2) For explanation of abbreviations see [Table 2](#)

2.3.4 General-Purpose Input/Output Pins

Table 6 General-Purpose Input/Output Pins¹⁾

Pin No.		Pin Name	Pin Type ²⁾	Buffer Type ³⁾	Function
PG-TQFP-64-8	PG-TQFP-100-3/-18				
–	98	GPIO0	I/O	OD, PP, PU ⁴⁾	General-Purpose I/O 0
–	97	GPIO1	I/O	OD, PP, PU ⁴⁾	General-Purpose I/O 1
–	96	GPIO2	I/O	OD, PP, PU ⁴⁾	General-Purpose I/O 2
–	95	GPIO3	I/O	OD, PP, PU ⁴⁾	General-Purpose I/O 3
–	91	GPIO4	I/O	OD, PP, PU ⁴⁾	General-Purpose I/O 4
–	90	GPIO5	I/O	OD, PP, PU ⁴⁾	General-Purpose I/O 5
–	89	GPIO6	I/O	OD, PP, PU ⁴⁾	General-Purpose I/O 6
–	88	GPIO7	I/O	OD, PP, PU ⁴⁾	General-Purpose I/O 7

1) If a GPIO pin is not used, it should be connected to ground via a 10 kΩ resistor. If guaranteed that it is never configured as an output, this pin can directly be connected to ground.

2) For explanation of abbreviations see [Table 1](#)

3) For explanation of abbreviations see [Table 2](#)

4) Buffer Type is programmable, after reset the pull-up is disabled and the pin is configured as an input

2.3.5 Test-Mode Selection/JTAG (Boundary Scan) Interface Pins

Table 7 Test-Mode Selection/JTAG (Boundary Scan) Interface Pins

Pin No.		Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Function
PG-TQFP-64-8	PG-TQFP-100-3/-18				
1	1	TDI	I	-	JTAG data input ³⁾
3	3	TMS	I	-	JTAG test-mode switch ⁴⁾
63	99	TCK	I	-	JTAG clock ⁴⁾
2	2	TDO	O	TS	JTAG data output ³⁾
64	100	TRSTQ	I	-	JTAG reset ⁴⁾

1) For explanation of abbreviations see [Table 1](#)

2) For explanation of abbreviations see [Table 2](#)

3) Pull-up resistor of 10 kΩ must be applied

4) Pull-down resistor of 10 kΩ must be applied

2.3.6 Interface-Type Selection Pins

Table 8 Interface-Type Selection Pins

Pin No.		Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Function
PG-TQFP-64-8	PG-TQFP-100-3/-18				
–	4	IFSEL0	I	PU	Interface-select pin 0
–	5	IFSEL1	I	PU	Interface-select pin 1

1) For explanation of abbreviations see [Table 1](#)

2) For explanation of abbreviations see [Table 2](#)

2.3.7 PCM Interface Pins

Table 9 PCM Interface Pins

Pin No.		Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Function
PG-TQFP-64-8	PG-TQFP-100-3/-18				
7	9	DX1	I/O	TS	PCM interface data output
8	10	DR1	I/O	TS	PCM interface data input
9	11	TC1Q	O	OD	Control pin for external driver

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Pin Description
Table 9 PCM Interface Pins (cont'd)

Pin No.		Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Function
PG-TQFP-64-8	PG-TQFP-100-3/-18				
10	12	FSC	I	-	Frame synchronization for PCM interface and PLL input
11	14	PCL	I	-	Input for the PCM interface data clock PCLK. The PCL clock can vary from 512 kHz to 8192 kHz in multiples of 512 kHz. This pin must be directly connected to MCLK.

1) For explanation of abbreviations see [Table 1](#)

2) For explanation of abbreviations see [Table 2](#)

2.3.8 Host Interface Pins

Table 10 Host Interface Pins

Pin No.		Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Signal Name			
PG-TQFP-64-8	PG-TQFP-100-3/-18				Intel Multi-plexed Mode	Intel Demulti-plexed Mode	Motorola	SPI
–	15	AD7/SA4	I/O	TS	A7/DIO7	DIO7	DATA7	SA4
–	16	AD6/SA3	I/O	TS	A6/DIO6	DIO6	DATA6	SA3
–	17	AD5/SA2	I/O	TS	A5/DIO5	DIO5	DATA5	SA2
–	18	AD4/SA1	I/O	TS	A4/DIO4	DIO4	DATA4	SA1
–	22	AD3/SA0	I/O	TS	A3/DIO3	DIO3	DATA3	SA0
–	23	AD2	I/O	TS	A2/DIO2	DIO2	DATA2	GND
15	24	AD1/DOUT	I/O	TS	A1/DIO1	DIO1	DATA1	DOUT ³⁾
16	25	AD0/DIN	I/O	TS	A0/DIO0	DIO0	DATA0	DIN ⁴⁾
–	26	A5/RDQ	I	-	RDQ	RDQ	ADDR5	GND
17	27	CSQ	I	-	CSQ	CSQ	CSQ	CSQ
–	28	RDYQ	O	OD	RDYQ	RDYQ	RDYQ	D.N.C.
18	29	INTQ	O	OD	INTQ	INTQ	INTQ	INTQ
–	35	RWQ/WRQ	I	-	WRQ	WRQ	RD/WRQ	GND
22	36	A4/DCLK	I	-	GND	A4	ADDR4	DCLK
–	37	A3/ALE	I	-	ALE	A3	ADDR3	GND
–	38	A2	I	-	GND	A2	ADDR2	GND
–	39	A1	I	-	GND	A1	ADDR1	GND
–	40	A0	I	-	GND	A0	ADDR0	GND

1) For explanation of abbreviations see [Table 1](#)

2) For explanation of abbreviations see [Table 2](#)

3) As the DOUT of the VINETIC® is set to high impedance for CSQ = high level, a pull-up resistor of 10 kΩ should be applied.

4) If the driver for the DIN signal may have high impedance, a pull-up resistor of 10 kΩ should be applied.

2.3.9 Digital Power/Ground Pins

Table 11 Digital Power/Ground Pins

Pin No.		Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Function
PG-TQFP-64-8	PG-TQFP-100-3/-18				
4 12 19 62	6 19 32 94	VDD15	PWR	-	1.5 V power supply for the digital part
43	66	VDD15P	PWR	-	1.5 V power supply for the PLL. The PLL is most important for the overall performance of the chip. Special care should be taken with respect to the filtering of the PLL power supply.
6 14 21 60	8 21 34 92	VDD33	PWR	-	Digital 3.3 V power supply for I/O pads
5 13 20 61	7 20 33 93	GND	GND	-	Digital ground
41	64	GND15P	GND	-	PLL ground Connect the PLL ground to a high quality ground.

1) For explanation of abbreviations see [Table 1](#)

2) For explanation of abbreviations see [Table 2](#)

2.4 VINETIC®-1CPE Pins Sorted by Function

2.4.1 Pins for Analog Line Module

Table 12 Pins for Analog Line Module

Pin No.		Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Function
PG-TQFP-64-8	PG-TQFP-100-3/-18				
39	61	CREF_AB	AI/O	-	Connection to external capacitor for low-pass filtering of the reference voltage
40	62	GND15_AB	GND	-	Common ground for bias block
38	60	VDD15_AB	PWR	-	1.5 V power supply for bias
29	47	RING_A	AI	-	Analog input for measurement the voltage on ring line
30	48	TIP_A	AI	-	Analog input for measurement the voltage on tip line
37	57	ACP_A	AO	-	Differential two-wire AC output voltage controlling the RING/TIP pins at the SLIC
36	56	ACN_A	AO	-	Differential two-wire AC output voltage controlling the RING/TIP pins at the SLIC
28	46	DCP_A	AO	-	Differential two-wire DC output voltage controlling the RING/TIP pins at the SLIC
27	45	DCN_A	AO	-	Differential two-wire DC output voltage controlling the RING/TIP pins at the SLIC
25	43	VDD33_A	PWR	-	3.3 V analog power supply
56	83	VDD33_B			
35	55	VDD15_A	PWR	-	1.5 V power supply
46	72	VDD15_B			
26	44	GND33_A	GND	-	Analog ground 3.3 V
55	82	GND33_B			
34	54	GND15_A	GND	-	Analog ground 1.5 V
47	73	GND15_B			
32	50	IT_A	AI	-	Transversal current input (AC + DC)
33	51	ITAC_A	AI	-	Transversal current input (AC)
31	49	VCMIT_A	AI	-	Reference pin for transversal/longitudinal current sensing
23	41	C2_A	AO	-	Ternary logic output controlling the SLIC operation mode
24	42	C1_A	AI/O	-	Ternary logic output controlling the SLIC operation mode; indicating thermal overload of a SLIC if a current of typically 150 µA is drawn out by the SLIC's C1 pin.

1) For explanation of abbreviations see [Table 1](#)

2) For explanation of abbreviations see [Table 2](#)

2.4.2 General Pins

Table 13 General Pins

Pin No.		Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Function
PG-TQFP-64-8	PG-TQFP-100-3/-18				
59	87	RESETQ	I	-	Hardware reset for the whole chip (active low)
42	65	MCLK	I	-	Master clock for the PLL input. The MCLK clock can vary from 512 kHz to 8192 kHz in multiples of 512 kHz. This pin must be directly connected to PCL.
48 49 50 51 52	75 76 77 78 79	ATEST1 ATEST2 ATEST3 ATEST4 ATEST5	NU	-	Analog test pins. These pins have to be connected together externally (shortcut).
44, 45, 53, 54, 57, 58	13, 30, 31, 52, 53, 58, 59, 63, 67, 68, 69, 70, 71, 74, 80, 81, 84, 85, 86	D.N.C.	NC	-	Do not connect

1) For explanation of abbreviations see [Table 1](#)

2) For explanation of abbreviations see [Table 2](#)

2.4.3 General-Purpose Input/Output Pins

Table 14 General-Purpose Input/Output Pins¹⁾

Pin No.		Pin Name	Pin Type ²⁾	Buffer Type ³⁾	Function
PG-TQFP-64-8	PG-TQFP-100-3/-18				
–	98	GPIO0	I/O	OD, PP, PU ⁴⁾	General-Purpose I/O 0
–	97	GPIO1	I/O	OD, PP, PU ⁴⁾	General-Purpose I/O 1
–	96	GPIO2	I/O	OD, PP, PU ⁴⁾	General-Purpose I/O 2
–	95	GPIO3	I/O	OD, PP, PU ⁴⁾	General-Purpose I/O 3
–	91	GPIO4	I/O	OD, PP, PU ⁴⁾	General-Purpose I/O 4
–	90	GPIO5	I/O	OD, PP, PU ⁴⁾	General-Purpose I/O 5
–	89	GPIO6	I/O	OD, PP, PU ⁴⁾	General-Purpose I/O 6
–	88	GPIO7	I/O	OD, PP, PU ⁴⁾	General-Purpose I/O 7

1) If a GPIO pin is not used, it should be connected to ground via a 10 kΩ resistor. If guaranteed that it is never configured as an output, this pin can directly be connected to ground.

2) For explanation of abbreviations see [Table 1](#)

- 3) For explanation of abbreviations see [Table 2](#)
 4) Buffer type is programmable. After reset the pull-up is disabled and the pin is configured as an input

2.4.4 Test-Mode Selection/JTAG (Boundary Scan) Interface Pins

Table 15 Test-Mode Selection/JTAG (Boundary Scan) Interface Pins

Pin No.		Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Function
PG-TQFP-64-8	PG-TQFP-100-3/-18				
1	1	TDI	I	-	JTAG data input ³⁾
3	3	TMS	I	-	JTAG test-mode switch ⁴⁾
63	99	TCK	I	-	JTAG clock ⁴⁾
2	2	TDO	O	TS	JTAG data output ³⁾
64	100	TRSTQ	I	-	JTAG reset ⁴⁾

- 1) For explanation of abbreviations see [Table 1](#)
 2) For explanation of abbreviations see [Table 2](#)
 3) Pull-up resistor of 10 kΩ must be applied
 4) Pull-down resistor of 10 kΩ must be applied

2.4.5 Interface-Type Selection Pins

Table 16 Interface-Type Selection Pins

Pin No.		Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Function
PG-TQFP-64-8	PG-TQFP-100-3/-18				
–	4	IFSEL0	I	PU	Interface-select pin 0
–	5	IFSEL1	I	PU	Interface-select pin 1

- 1) For explanation of abbreviations see [Table 1](#)
 2) For explanation of abbreviations see [Table 2](#)

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Pin Description

2.4.6 PCM Interface Pins

Table 17 PCM Interface Pins

Pin No.		Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Function
PG-TQFP-64-8	PG-TQFP-100-3/-18				
7	9	DX1	I/O	TS	PCM interface data output (tristate)
8	10	DR1	I/O	TS	PCM interface data input
9	11	TC1Q	O	OD	Control pin for external driver (open drain)
10	12	FSC	I	-	Frame synchronization for PCM interface and PLL input
11	14	PCL	I	-	Input for the PCM interface data clock PCLK. The PCL clock can vary from 512 kHz to 8192 kHz in multiples of 512 kHz. This pin must be directly connected to MCLK.

1) For explanation of abbreviations see [Table 1](#)

2) For explanation of abbreviations see [Table 2](#)

2.4.7 Host Interface Pins

Table 18 Host Interface Pins

Pin No.		Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Signal Name			
PG-TQFP-64-8	PG-TQFP-100-3/-18				Intel Multi-plexed Mode	Intel Demulti-plexed Mode	Motorola	SPI
–	15	AD7/SA4	I/O	TS	A7/DIO7	DIO7	DATA7	SA4
–	16	AD6/SA3	I/O	TS	A6/DIO6	DIO6	DATA6	SA3
–	17	AD5/SA2	I/O	TS	A5/DIO5	DIO5	DATA5	SA2
–	18	AD4/SA1	I/O	TS	A4/DIO4	DIO4	DATA4	SA1
–	22	AD3/SA0	I/O	TS	A3/DIO3	DIO3	DATA3	SA0
–	23	AD2	I/O	TS	A2/DIO2	DIO2	DATA2	GND
15	24	AD1/DOUT	I/O	TS	A1/DIO1	DIO1	DATA1	DOUT ³⁾
16	25	AD0/DIN	I/O	TS	A0/DIO0	DIO0	DATA0	DIN ⁴⁾
–	26	A5/RDQ	I	-	RDQ	RDQ	ADDR5	GND
17	27	CSQ	I	-	CSQ	CSQ	CSQ	CSQ
–	28	RDYQ	O	OD	RDYQ	RDYQ	RDYQ	D.N.C.
18	29	INTQ	O	OD	INTQ	INTQ	INTQ	INTQ
–	35	RWQ/WRQ	I	-	WRQ	WRQ	RD/WRQ	GND
22	36	A4/DCLK	I	-	GND	A4	ADDR4	DCLK
–	37	A3/ALE	I	-	ALE	A3	ADDR3	GND
–	38	A2	I	-	GND	A2	ADDR2	GND

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Pin Description
Table 18 Host Interface Pins (cont'd)

Pin No.		Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Signal Name			
PG-TQFP-64-8	PG-TQFP-100-3/-18				Intel Multi-plexed Mode	Intel Demulti-plexed Mode	Motorola	SPI
–	39	A1	I	–	GND	A1	ADDR1	GND
–	40	A0	I	–	GND	A0	ADDR0	GND

1) For explanation of abbreviations see [Table 1](#)

2) For explanation of abbreviations see [Table 2](#)

3) As the DOUT of the VINETIC® is set to high impedance for CSQ = high level, a pull-up resistor of 10 kΩ should be applied.

4) If the driver for the DIN signal may have high impedance, a pull-up resistor of 10 kΩ should be applied.

2.4.8 Digital Power/Ground Pins

Table 19 Digital Power/Ground Pins

Pin No.		Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Function
PG-TQFP-64-8	PG-TQFP-100-3/-18				
4 12 19 62	6 19 32 94	VDD15	PWR	–	1.5 V power supply for the digital part
43	66	VDD15P	PWR	–	1.5 V power supply for the PLL. The PLL is most important for the overall performance of the chip. Special care should be taken with respect to the filtering of the PLL supply.
6 14 21 60	8 21 34 92	VDD33	PWR	–	Digital 3.3 V power supply for I/O pads
5 13 20 61	7 20 33 93	GND	GND	–	Digital ground
41	64	GND15P	GND	–	PLL ground Connect the PLL ground to a high quality ground.

1) For explanation of abbreviations see [Table 1](#)

2) For explanation of abbreviations see [Table 2](#)

3 Hardware Behavior and Handling

3.1 Block Diagram VINETIC®-2CPE/-1CPE

Figure 9 is a the block diagram of the VINETIC®-2CPE/-1CPE.

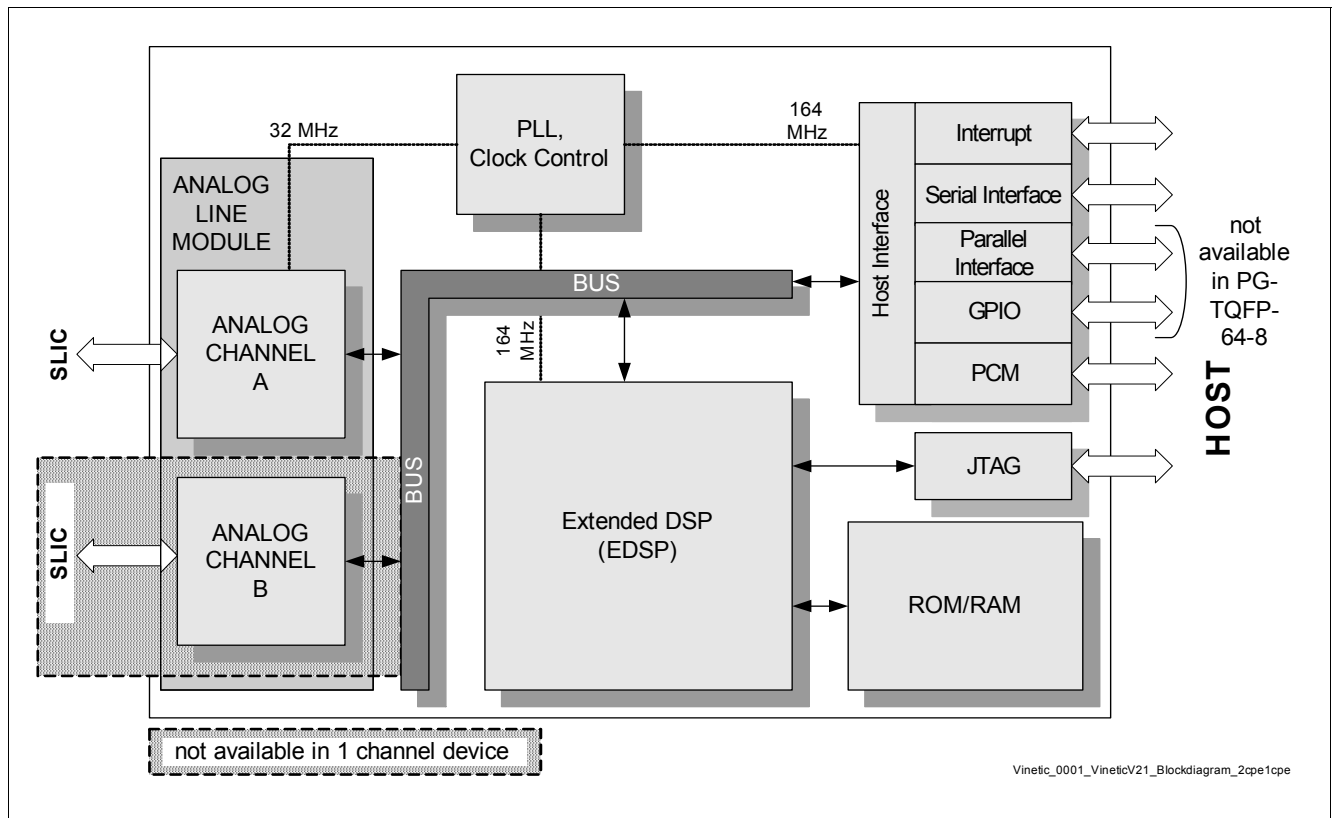


Figure 9 Block Diagram VINETIC®-2CPE/-1CPE

3.2 Clocking

The VINETIC®-2CPE/-1CPE needs the following clocks: master clock (MCLK), frame synchronization clock (FSC), and PCM interface clock (PCL).

MCLK has to fulfill the specification described in [Table 21](#) and [Figure 10](#) and has to be phase-locked to FSC. The FSC has to fulfill the specification described in [Chapter 4.3](#).

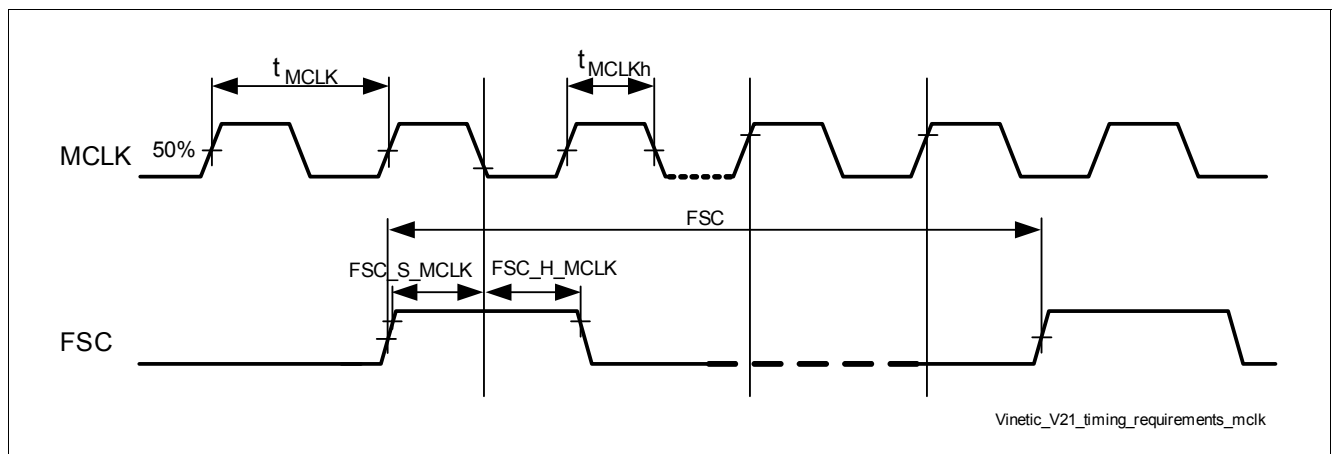
PCL must be directly connected to MCLK and has to fulfill the specification described in [Table 31](#).

All clocks have to be provided regardless of the application. Even though the PCM interface might not be used, the clocks on MCLK, PCL and FSC have to be provided at all times to ensure correct operation of the device.

Clock failure bits (see [Figure 11](#)) of the VINETIC®-2CPE/-1CPE are able to indicate a clock synchronization problem. The bit SYNC-FAIL detects a clock divider synchronization failure and the bit MCLK-FAIL reports a PLL synchronization failure. In case of unlock of the PLL, all clocks are internally shut down and the chip operation is stopped. The current Analog Line Module (ALM) mode will be frozen.

Table 20 Clocks

Pin	Description	Frequency
MCLK	Master clock (mandatory), only multiples of 512 kHz are allowed. Has to be phase-locked to FSC. For timing requirements of the MCLK signal, refer to Table 21 .	$64 \cdot f_{FSC}$ to $1024 \cdot f_{FSC}$ in steps of $64 \cdot f_{FSC}$
FSC	Frame synchronization clock (mandatory), Synchronizes internal clocks and voice interface.	$f_{FSC} = 8 \text{ kHz}$
PCL (PCM)	Clock for voice (PCM) interface (mandatory), only multiples of 512 kHz are allowed. The PCL pin must be directly connected to the MCLK pin.	$64 \cdot f_{FSC}$ to $1024 \cdot f_{FSC}$ in steps of $64 \cdot f_{FSC}$ depending on the number of time slots (see Table 31).
TCK	Clock for boundary scan controller (optional)	1 MHz to 10 MHz


Figure 10 Timing Requirements MCLK
Table 21 Timing Requirements MCLK

Parameter	Symbol	Values			Note /Test Condition
		Min.	Typ.	Max.	
Period MCLK ¹⁾	t_{PCL}	1/8192	–	1/512	ms
Frequency tolerance		-100	–	100	ppm
MCLK high time	t_{PCLh}	$0.4 \times t_{MCLK}$	–	$0.6 \times t_{MCLK}$	μs
Period FSC ¹⁾	t_{FSC}	–	125	–	μs
FSC setup time	$t_{FSC_S_MCLK}$	10	–	–	ns
FSC hold time	$t_{FSC_H_MCLK}$	40	–	$t_{FSC} - t_{MCLK} - t_{FSC_S_MCLK}^{2)}$	ns
MCLK jitter phase noise density 1 kHz frequency offset		–	–	-80	dBc ³⁾ /Hz

1) The MCLK frequency must be an integer multiple of the FSC frequency ($n \cdot 64 \cdot f_{FSC}$, $n = 1..16$).

2) This is to ensure that the FSC can be sampled low at least for one t_{MCLK} within t_{FSC} .

3) dBc = dB carrier.

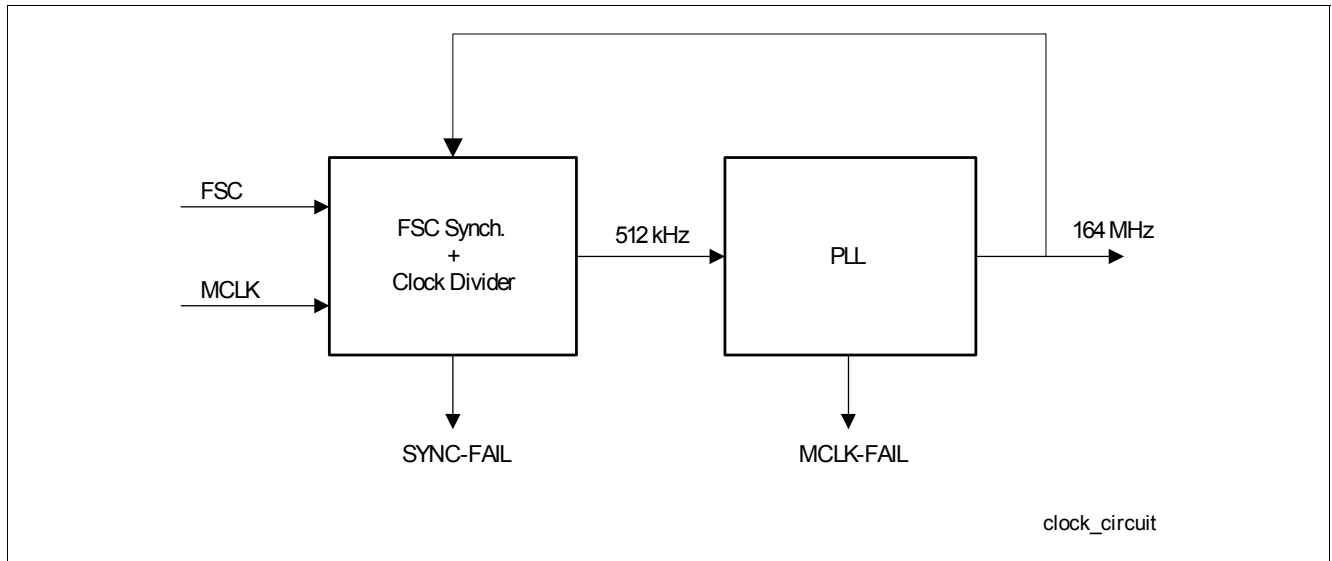


Figure 11 Clock Fail Bits

3.3 Reset

It is mandatory to apply a hardware reset after the power-up sequence.

A hardware reset of the VINETIC®-2CPE/-1CPE requires setting the signal at the RESETQ input pin to low level for at least 20 μs ($t_{\text{res}} \geq 20 \mu\text{s}$). RESETQ has a spike rejection function that will safely suppress spikes with a duration of less than 2 μs ($t_{\text{rej}} \leq 2 \mu\text{s}$).

By pulling the RESETQ input pin to low, the chip will be reset (see Figure 12) and the following actions will be performed:

- All I/O pins are deactivated (tristate high impedance)
- All outputs are inactive (e.g. DX1)
- The internal PLL is stopped
- VCMIT is floating
- The ternary pins C1_x¹⁾ and C2_x¹⁾, controlling the SLIC operation mode, are actively driven with 0 V.
- Internal clocks are deactivated
- The chip is in a Reset State

With the rising edge of the reset signal all external clocks need to be stable already, then the following actions are performed:

- Clock detection
- PLL synchronization
- Activation of reset routine: the internal reset routine requires approximately 16 frames ($16 \times 125 \mu\text{s} = 2 \text{ ms}$) to be finished (including PLL start-up and clock synchronization).
- After the reset routine has finished, the ALM will be in PDH (Power Down High Impedance) mode.
- No interrupt will be generated at the end of the reset routine.
- First access to the VINETIC®-2CPE/-1CPE is possible after 2 ms.

Figure 12 shows the reset sequence for the hardware reset caused by a signal at RESETQ pin.

1) x = A, B

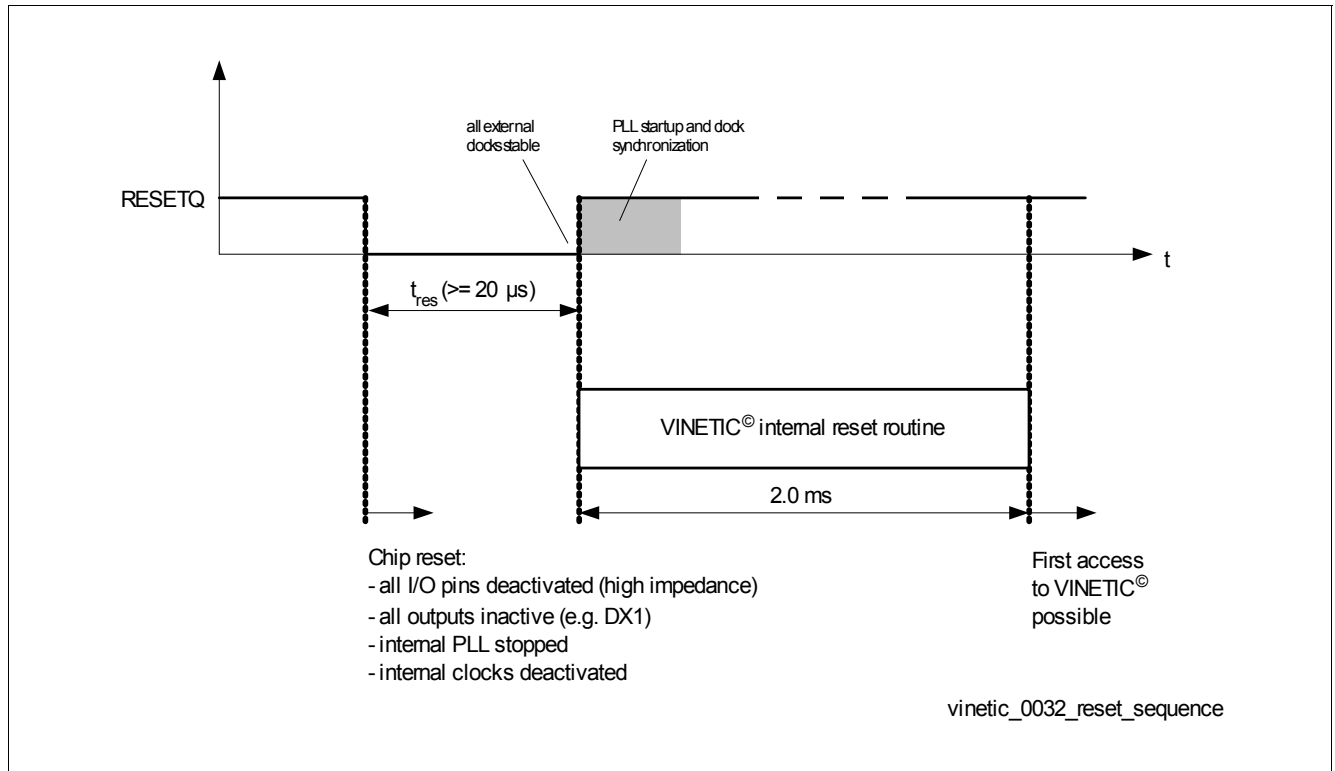


Figure 12 VINETIC® Reset Sequence

3.4 Test Modes of the VINETIC®-2CPE/-1CPE

3.4.1 Boundary Scan Test

The Boundary Scan Test (BST) is a standardized method for testing boards, also providing a standard interface to communicate with test circuits on an IC such as the VINETIC®-2CPE/-1CPE. The boundary scan standard specifies a four-wire interface using the four signals TDI, TDO, TCK and TMS. Additionally, an optional test reset signal TRSTQ is available.

These four (or five) dedicated signals on the test access port (TAP), are connected to the TAP controller inside the VINETIC®-2CPE/-1CPE. The TAP controller is a state machine clocked with the rising edge of TCK and the state transitions are controlled by TMS. The VINETIC®-2CPE/-1CPE supports fully IEEE 1149.1 compliant boundary scans that creates Boundary Scan Description Language (BSDL) files.

Boundary Scan Description Language (BSDL) is a standard way to describe the features and behavior of an IC such as the VINETIC®-2CPE/-1CPE that are capable of IEEE 1149.1-compliant boundary scans. It is also a standard way to pass information to test-generation software.

4 Interface Description

For programming the VINETIC® and performing data transfer from/to the VINETIC®, a parallel interface or a serial microcontroller interface can be used. Additionally, the VINETIC® has an interface to PCM data.

VINETIC® 8-bit Parallel Interfaces

- The parallel interface can be operated in Intel 8-bit mode (multiplexed/demultiplexed) or in 8-bit Motorola mode.

VINETIC® Serial Interfaces

- The VINETIC® serial microcontroller interface (μ C interface = SCI) is compatible with the Motorola SPI and the Infineon SCI.

VINETIC® PCM Interface

- The VINETIC® PCM interface has two PCM highways that are internally cross-connected, and can be operated together with the serial μ C interface or the parallel interface.

The VINETIC®-2CPE/-1CPE supports the most widely used microcontrollers: e.g. MPC850, MPC860, MPC8260, C165UTAH, MIPS and ARM derivatives, etc. All parallel and serial interfaces (host interfaces) use the same (multiplexed) pins. The desired interface type is selected by means of pin-strapping with the pins IFSEL0 and IFSEL1 for the PG-TQFP-100-3 and PG-TQFP-100-18. With PG-TQFP-64-8, only the serial interface is available.

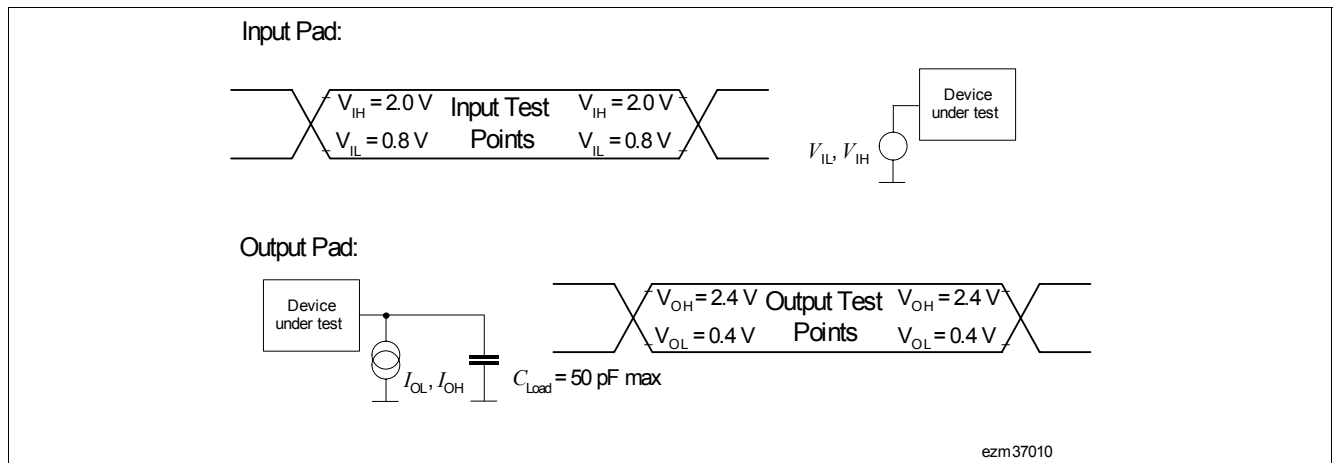
Note: Host interface and PCM interface can be used in parallel.

Table 22 shows the possible interface configurations:

Table 22 Interface Configurations

No.	Interface Type	IFSEL1	IFSEL0
1.	8-bit Intel Multiplexed	0	0
2.	8-bit Intel Demultiplexed	0	1
3.	8-bit Motorola	1	0
4.	SCI	1	1

Note: MCLK, PCL and FSC always have to be supplied even if no PCM interface is used.

Input/Output Waveform for AC Interface Timing Characteristics

Figure 13 Waveform for AC Tests

During AC-testing, the CMOS inputs are driven at a low level of 0.8 V and a high level of 2.0 V. The CMOS outputs are measured at 0.4 V and 2.4 V respectively.

4.1 Intel/Motorola-Mode Parallel Interfaces

4.1.1 Control for Intel/Motorola-Interfaces

The VINETIC®-2CPE/-1CPE uses five (Intel Demultiplexed Mode), six (Motorola Mode) or eight (Intel Multiplexed Mode) address bits. In the demultiplexed mode, the address information is taken from the pins A0 ... A4 (Intel Demultiplexed Mode) or from the pins A0 ... A5 (Motorola Mode). In the multiplexed mode, the address information is taken from the pins AD0 ... AD7 (Intel Multiplexed Mode).

4.1.2 Pin Description, Intel Interface

Table 23 Intel Demultiplexed Mode Interface Pins

Signal Name	Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Function
CSQ	CSQ	I	-	Chip select input, start of data transfer with WRQ/RDQ (active low)
WRQ	RWQ/WRQ	I	-	Data-strobe input write (active low)
RDQ	A5/RDQ	I	-	Data-strobe input read (active low)
RDYQ	RDYQ	O	OD	Ready line (active low)
A[4:0]	A4..0	I	-	Address lines
DIO[7:0]	AD7..0	I/O	TS	Data bus

1) For explanation of abbreviations, see [Table 1](#)

2) For explanation of abbreviations see [Table 2](#)

Table 24 Intel Multiplexed Mode Interface Pins

Signal Name	Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Function
ALE	A3/ALE	I	-	Address latch enable
CSQ	CSQ	I	-	Chip select input, start of data transfer with WRQ/RDQ (active low)
WRQ	RWQ/WRQ	I	-	Data-strobe input write (active low)
RDQ	A5/RDQ	I	-	Data-strobe input read (active low)
RDYQ	RDYQ	O	OD	Ready line (active low)
A[7:0], DIO[7:0]	AD7..0	I/O	TS	Address or Data bus

1) For explanation of abbreviations, see [Table 1](#)

2) For explanation of abbreviations see [Table 2](#)

4.1.3 Timing, Intel Demultiplexed Mode

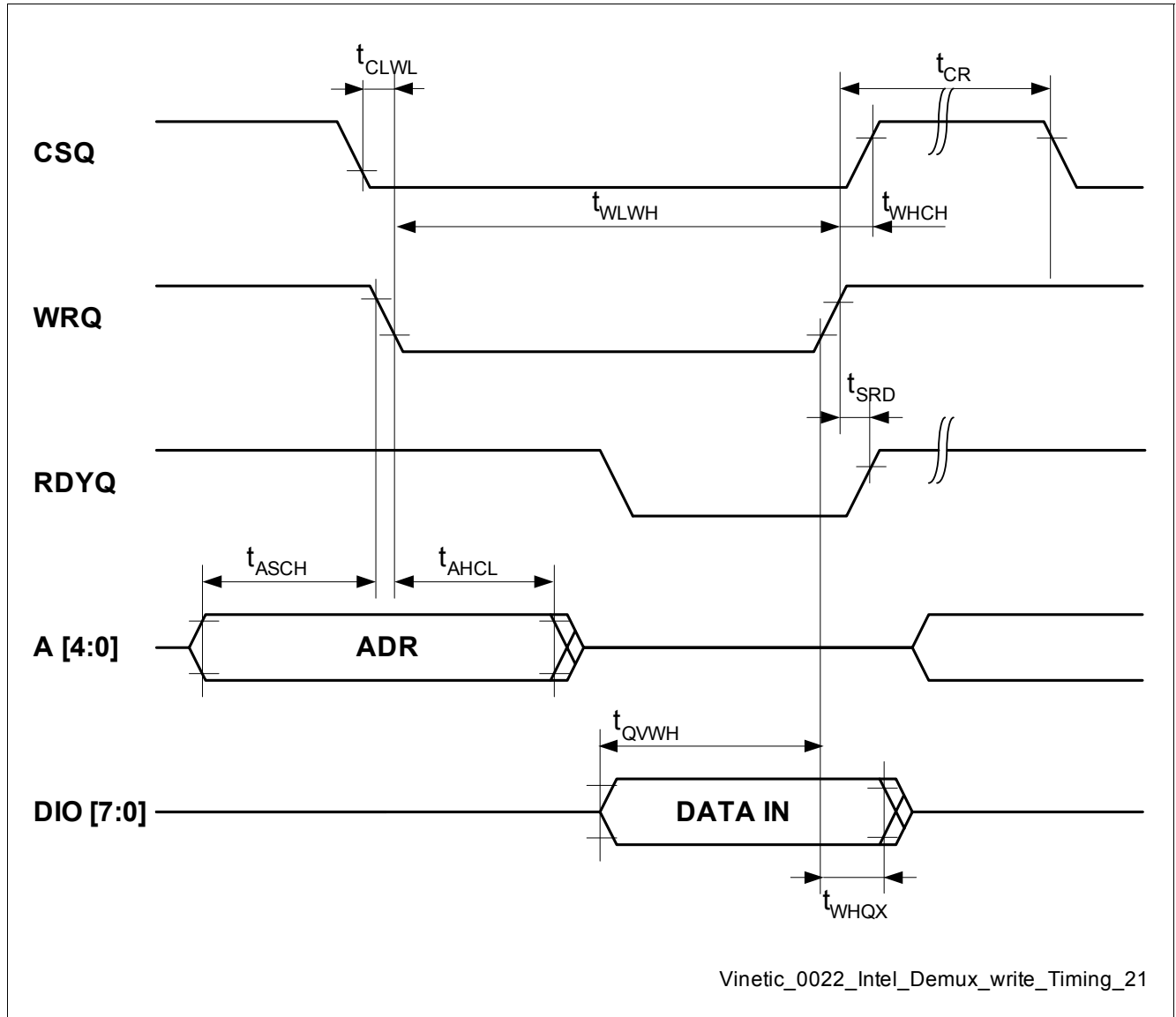


Figure 14 Write Access, Intel Demultiplexed Mode

Intel Demultiplexed: little-endian¹⁾.

¹⁾ Low-order byte is stored at the lower address and high-order byte is stored at the higher address.

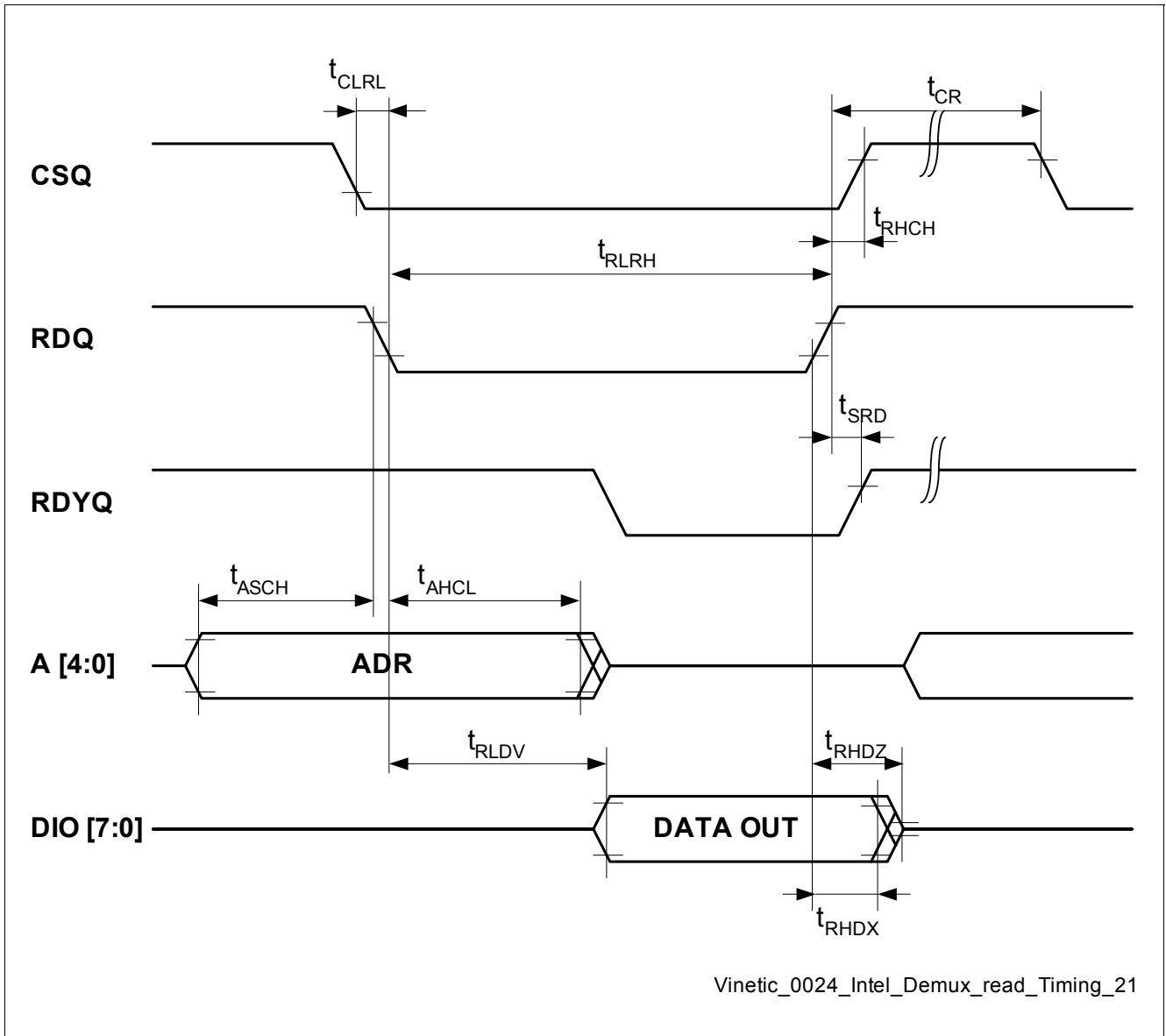


Figure 15 Read Access, Intel Demultiplexed Mode

Note: In the Intel Demultiplexed Mode the chip internal address latch signal is derived from an or-connection of the signals CSQ and WRQ for a write access and of the signals CSQ and RDQ for a read access respectively.

4.1.4 Timing, Intel Multiplexed Mode

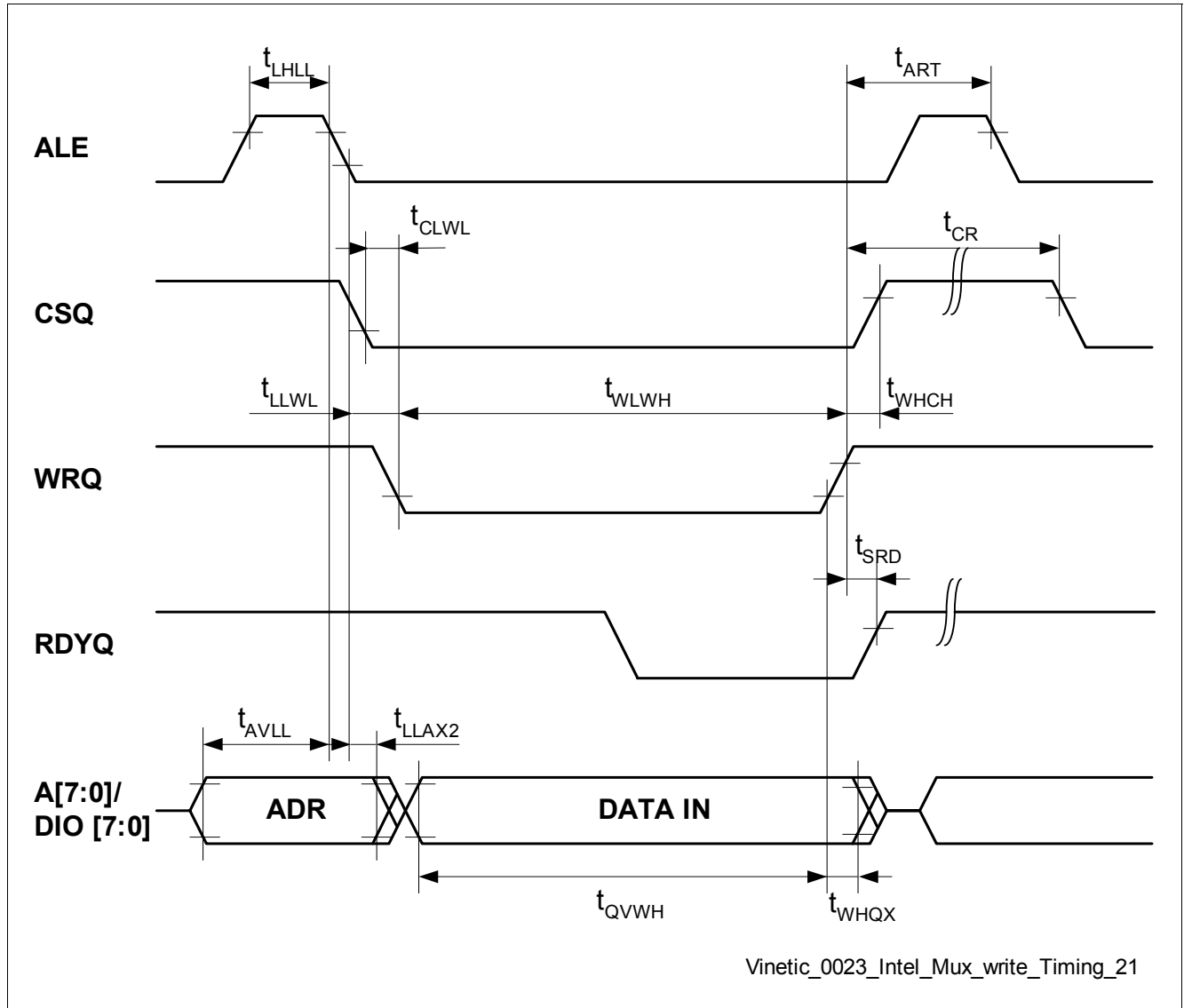
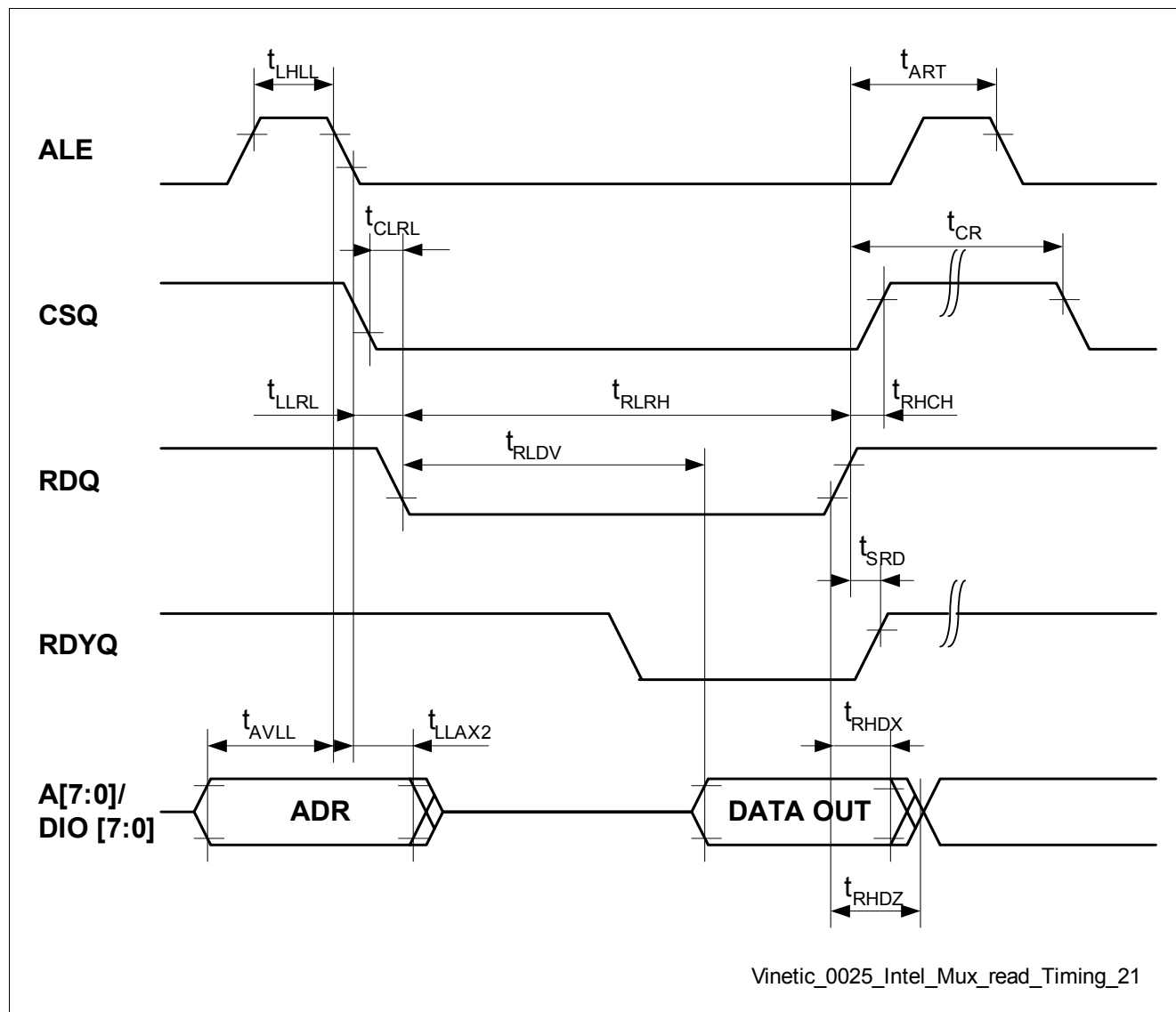


Figure 16 Write Access, Intel Multiplexed Mode

Intel Multiplexed: little-endian¹⁾.

1) Low-order byte is stored at the lower address and high-order byte is stored at the higher address.


Figure 17 Read Access, Intel Multiplexed Mode
Table 25 Timing Specification, Intel Multiplexed/Demultiplexed Mode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ALE high time	t_{LHLL}	20	—	—	ns	—
Address setup to ALE	t_{AVLL}	10	—	—	ns	—
Address hold after ALE inactive	t_{LLAX2}	10	—	—	ns	—
Address recovery time	t_{ART}	50	—	—	ns	—
Address setup to CSQ	t_{ASCH}	10	—	—	ns	—
Address hold after CSQ	t_{AHCL}	10	—	—	ns	—
RDQ active to valid data out	t_{RLDV}	—	—	50	ns	—
Data hold after RDQ inactive	t_{RHDX}	0	—	—	ns	—
Data float after RDQ inactive	t_{RHDZ}	—	—	10	ns	—
Data setup before WRQ inactive	t_{QVWH}	20	—	—	ns	—

Table 25 Timing Specification, Intel Multiplexed/Demultiplexed Mode (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data hold after WRQ inactive	t_{WHQX}	2.5	–	–	ns	–
RDQ active after ALE inactive	t_{LLRL}	20	–	–	ns	–
WRQ active after ALE inactive	t_{LLWL}	0	–	–	ns	–
RDQ pulse width	t_{RLRH}	70	–	–	ns	–
WRQ pulse width	t_{WLWH}	60	–	–	ns	–
CSQ low to WRQ low ¹⁾	t_{CLWL}	0	–	–	ns	–
WRQ high to CSQ high ¹⁾	t_{WHCH}	0	–	–	ns	–
CSQ low to RDQ low ¹⁾	t_{CLRL}	0	–	–	ns	–
RDQ high to CSQ high ¹⁾	t_{RHCH}	0	–	–	ns	–
Strobe signal to RDYQ delay time	t_{SRD}	–	–	10	ns	–
Command recovery time	t_{CR}	20	–	–	ns	–

1) These parameters are for reference only; they can also be negative. The control inputs RDQ and WRQ are OR-gated internally with CSQ. If the active CSQ is shorter (embedded), the active RDQ or WRQ always refer to the resulting OR-gated signal.

4.1.5 Pin Description, Motorola Interface

Table 26 Motorola Interface Pins

Signal Name	Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Function
ADDR[5:0]	A5/RDQ, A4/DCLK, A3/ALE, A2, A1, A0	I	-	Address lines
DATA[7:0]	AD7..0	I/O	TS	Data bus
CSQ	CSQ	I	-	Chip select, data strobe with RD/WRQ (active low)
RD/WRQ	RWQ/WRQ	I	-	Read/write, data-strobe signal. (read → active high, write → active low)
RDYQ	RDYQ	O	OD	Ready line (active low)

1) For explanation of abbreviations, see [Table 1](#)

2) For explanation of abbreviations see [Table 2](#)

Motorola: big-endian¹⁾.

1) High-order byte is stored at the lower address and the low-order byte at the higher address.

4.1.6 Timing, Motorola Interface

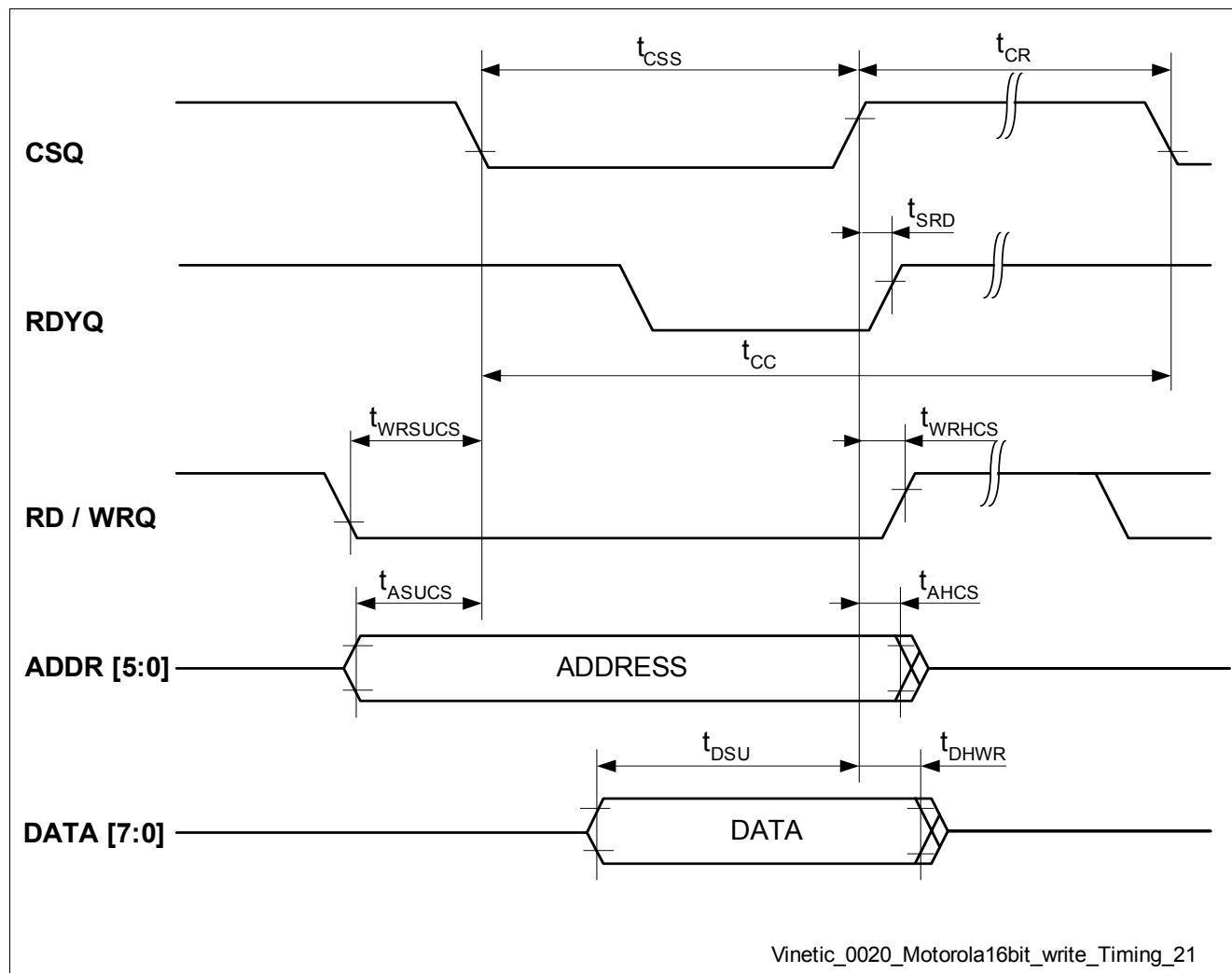
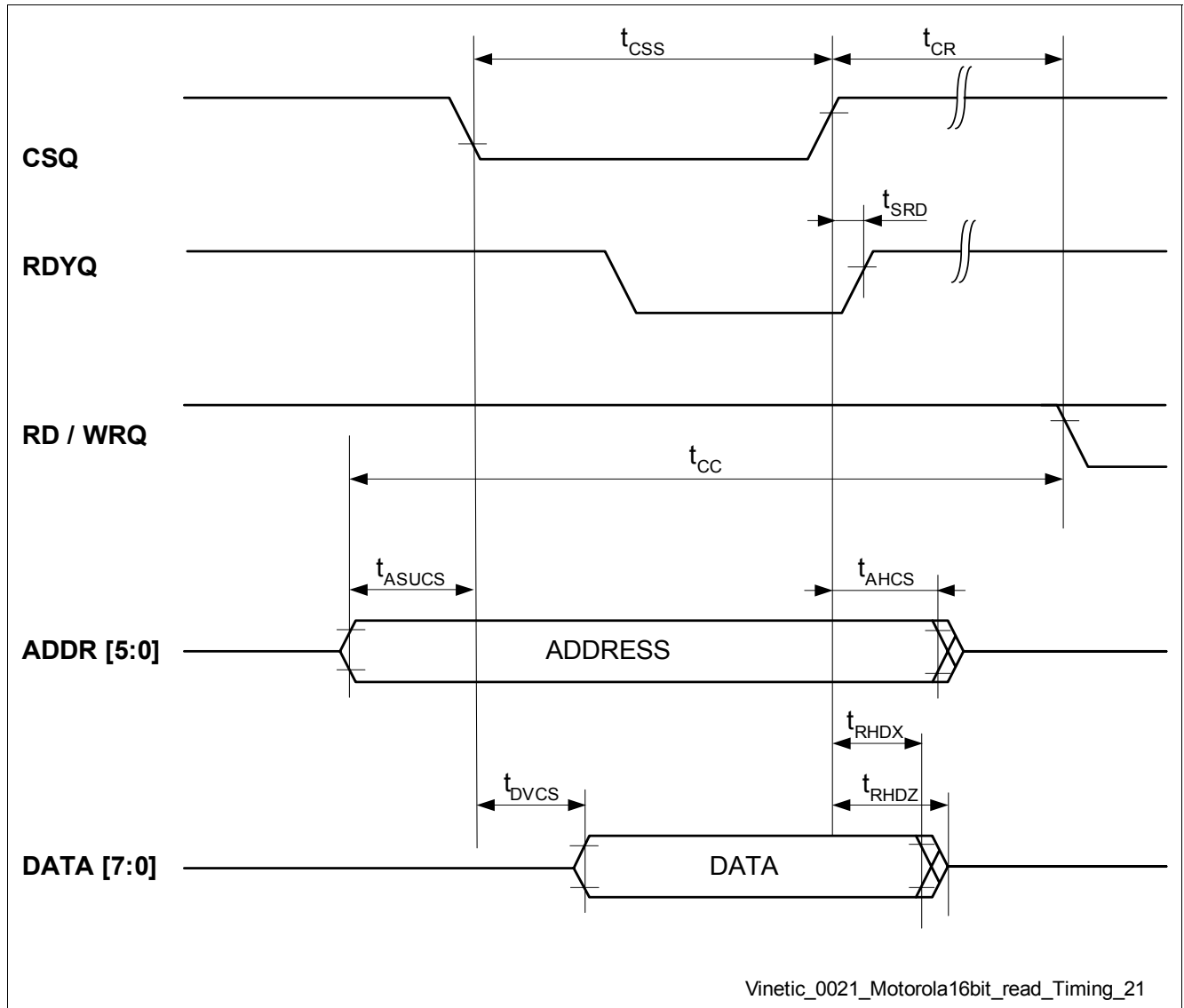


Figure 18 Write Access, Motorola Mode


Figure 19 Read Access, Motorola Mode
Table 27 Timing Specifications for the Motorola Mode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
CSQ strobe-pulse width	t_{CSS}	70 ¹⁾	—	—	ns	—
Address setup time to CSQ	t_{ASUCS}	5	—	—	ns	—
Write setup time to CSQ	t_{WRSUCS}	5	—	—	ns	—
Write hold time to CSQ	t_{WRHCS}	5	—	—	ns	—
Data setup time to CSQ strobe	t_{DSU}	10	—	—	ns	—
Data hold time after write access	t_{DHWR}	2.5	—	—	ns	—
Strobe signal to RDYQ delay time	t_{SRD}	—	—	10	ns	—
Command recovery time	t_{CR}	20	—	—	ns	—
Command cycle time	t_{CC}	90	—	—	ns	—
Data valid after CSQ	t_{DVCS}	—	—	50	ns	—

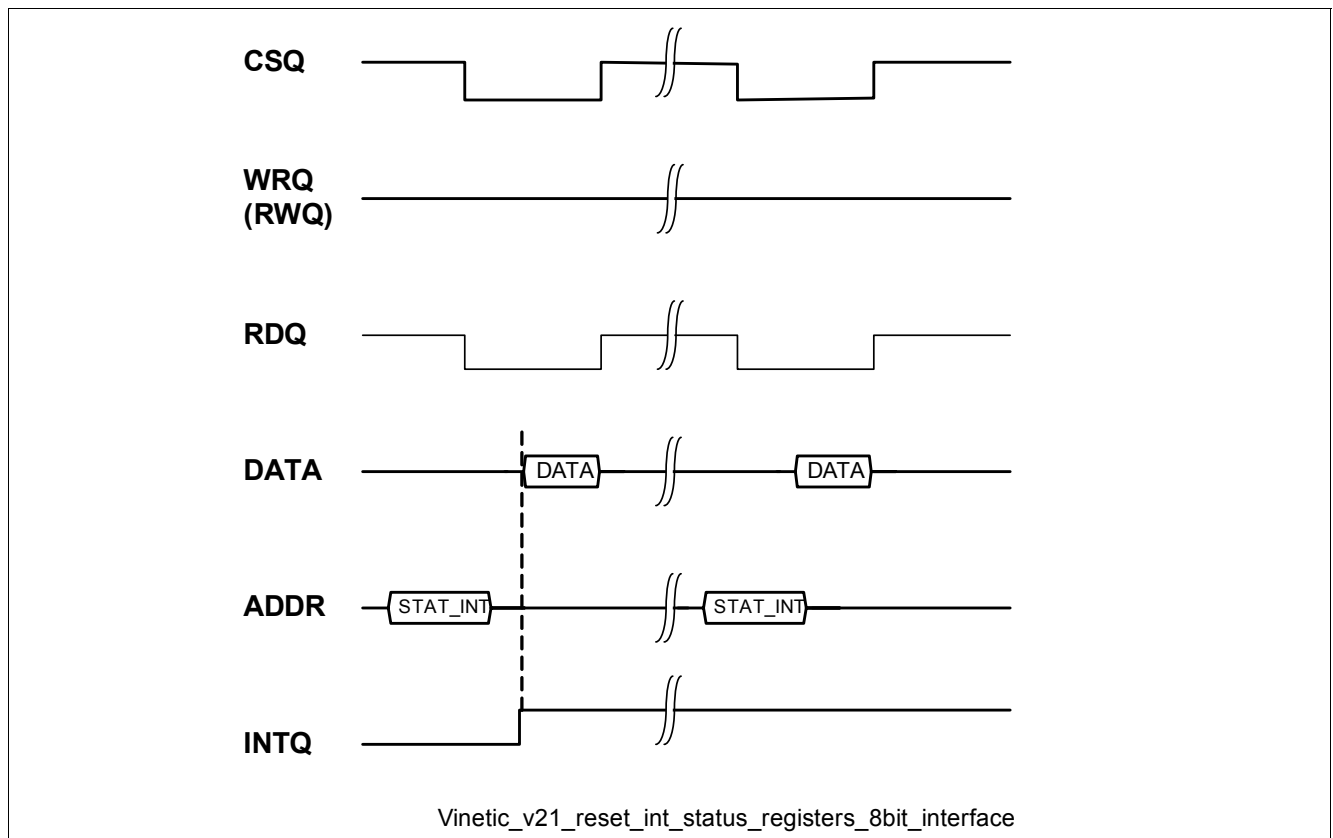
Table 27 Timing Specifications for the Motorola Mode (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data hold after read access	t_{RHDX}	0	–	–	ns	–
Data float after read access	t_{RHDZ}	–	–	10	ns	–
Address hold time to CSQ	t_{AHCS}	10	–	–	ns	–

1) If RDYQ is used, these values may be lower.

4.1.7 Reset of Interrupt Status Registers in Case of 8-Bit Interfaces

All interrupt status bits are cleared by reading respectively writing the associated interrupt register. If any 8-bit interface is used, the interrupt status register is cleared when the first byte of the register is read by the host controller. **Figure 20** shows that the INTQ line is released after reading the first byte of the interrupt status register. This means that the INTQ line is deasserted before the read command is finished.


Figure 20 VINETIC® Reset Interface Status Registers, 8-Bit Interface

4.2 SCI/SPI Interface

The SCI interface of the VINETIC®-2CPE/-1CPE represents one mode of the SPI interface of the Motorola PowerQUICC® family (SPI slave mode). The data are serialized with the MSB first.

Note: The VINETIC®-2CPE/-1CPE always works as a slave.

4.2.1 Pin Description, SCI/SPI Interface

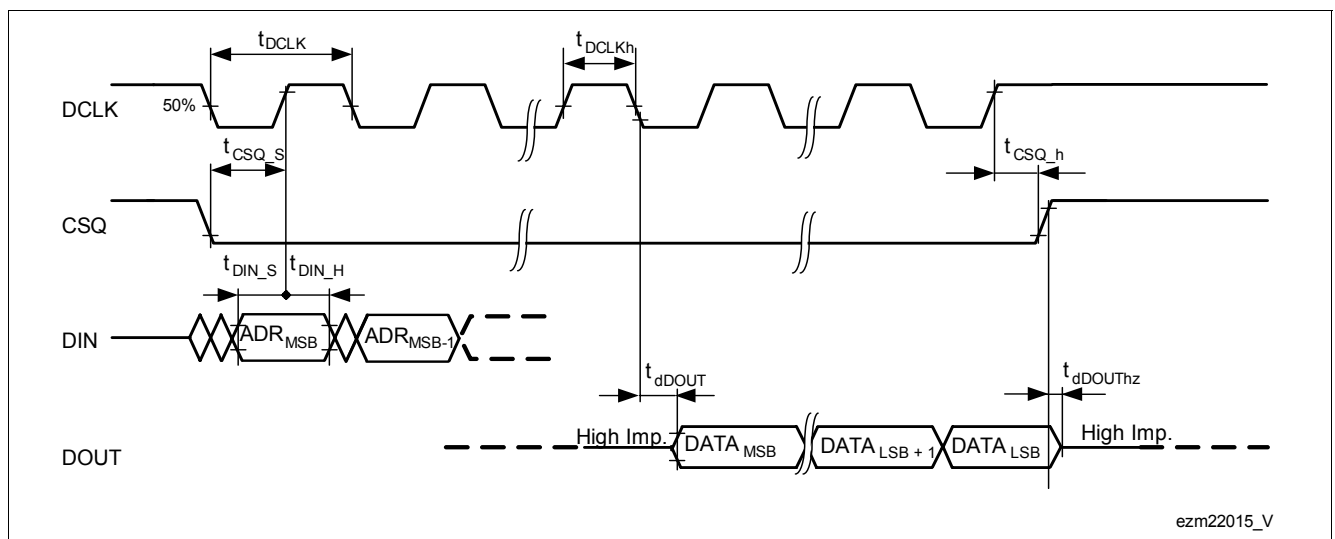
Table 28 SCI/SPI Interface Pins

Signal Name	Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Function
CSQ	CSQ	I	-	Chip select signal starting a read or write access to VINETIC®-2CPE/-1CPE
DCLK	A4/DCLK	I	-	Data Clock supplied to VINETIC®-2CPE/-1CPE
DIN	AD0/DIN	I	-	Data input carries data from the master device to the VINETIC®-2CPE/-1CPE
DOUT	AD1/DOUT	O	TS	Data output carries data from VINETIC®-2CPE/-1CPE to a master device
SA[4:0]	SA4...SA0	I		SCI Slave address

1) For explanation of abbreviations, see [Table 1](#)

2) For explanation of abbreviations see [Table 2](#)

4.2.2 Timing, SCI/SPI Interface


Figure 21 SCI/SPI Interface Timing

Note: In case of SCI/SPI, the RDYQ line has no function. The data clock DCLK must only be applied during the data transfer

Table 29 Timing Values, SCI/SPI Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Period DCLK	t_{DCLK}	1/8192	—	—	ms	—
DCLK high time	t_{DCLKh}	$0.4 \times t_{DCLK}$	$0.5 \times t_{DCLK}$	$0.6 \times t_{DCLK}$	μs	—
CSQ setup time	t_{CSQ_s}	10	—	—	ns	—
CSQ hold time	t_{CSQ_h}	30	—	—	ns	—
DIN setup time	t_{DIN_s}	10	—	—	ns	—

Table 29 Timing Values, SCI/SPI Interface (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DIN hold time	t_{DIN_h}	10	–	–	ns	–
DOUT delay time ¹⁾	t_{dDOUT}	40	–	$t_{dDOUT_min} + 0.4[ns/pF] \times C_{Load}[pF]$	ns	–
DOUT delay time to high Z	$t_{dDOUThz}$	–	–	10	ns	–

1) All delay times are made up by two components: an intrinsic time (min.-time) caused by internal processing, and a second component caused by external circuitry (C_{Load})

4.3 PCM Interface

The serial PCM interface is used to transfer A-Law or μ -Law or ADPCM-compressed voice data. The PCM interface can also transfer linear data. In this case, two successive time slots are used. The five signals of the PCM interface are used as follows (internally two cross-connected PCM highways available):

4.3.1 Pin Description, PCM Interface

Table 30 PCM Interface Pins

Signal Name	Pin Name	Pin Type ¹⁾	Buffer Type ²⁾	Function
PCLK	PCL	I	–	PCM interface data clock
FSC	FSC	I	–	Frame synchronization for PCM interface and PLL input
DX1	DX1	I/O	TS	PCM interface data output
DR1	DR1	I/O	TS	Data input for highway one of PCM interface
TC1Q	TC1Q	O	OD	Control pin for external driver

1) For explanation of abbreviations, see [Table 1](#)

2) For explanation of abbreviations see [Table 2](#)

The FSC pulse identifies the beginning of a receive and transmit frame for both highways (see [Figure 22](#)). The PCLK clock signal synchronizes the data transfer on the DX1 and DR1 lines. In each active time slot, bytes are serialized with the MSB first. As a default setting, the rising edge indicates the start of the bit, while the falling edge is used to latch the contents of the received data on DR1. If double-clock rate is selected (PCLK clock rate is twice the data rate), the first rising edge indicates the start of a bit, while, by default, the second falling edge is used to latch the contents of the data line DR1.

The VINETIC®-2CPE/-1CPE allows for flexible programming of the PCM interface. For more information, see [\[5\]](#).

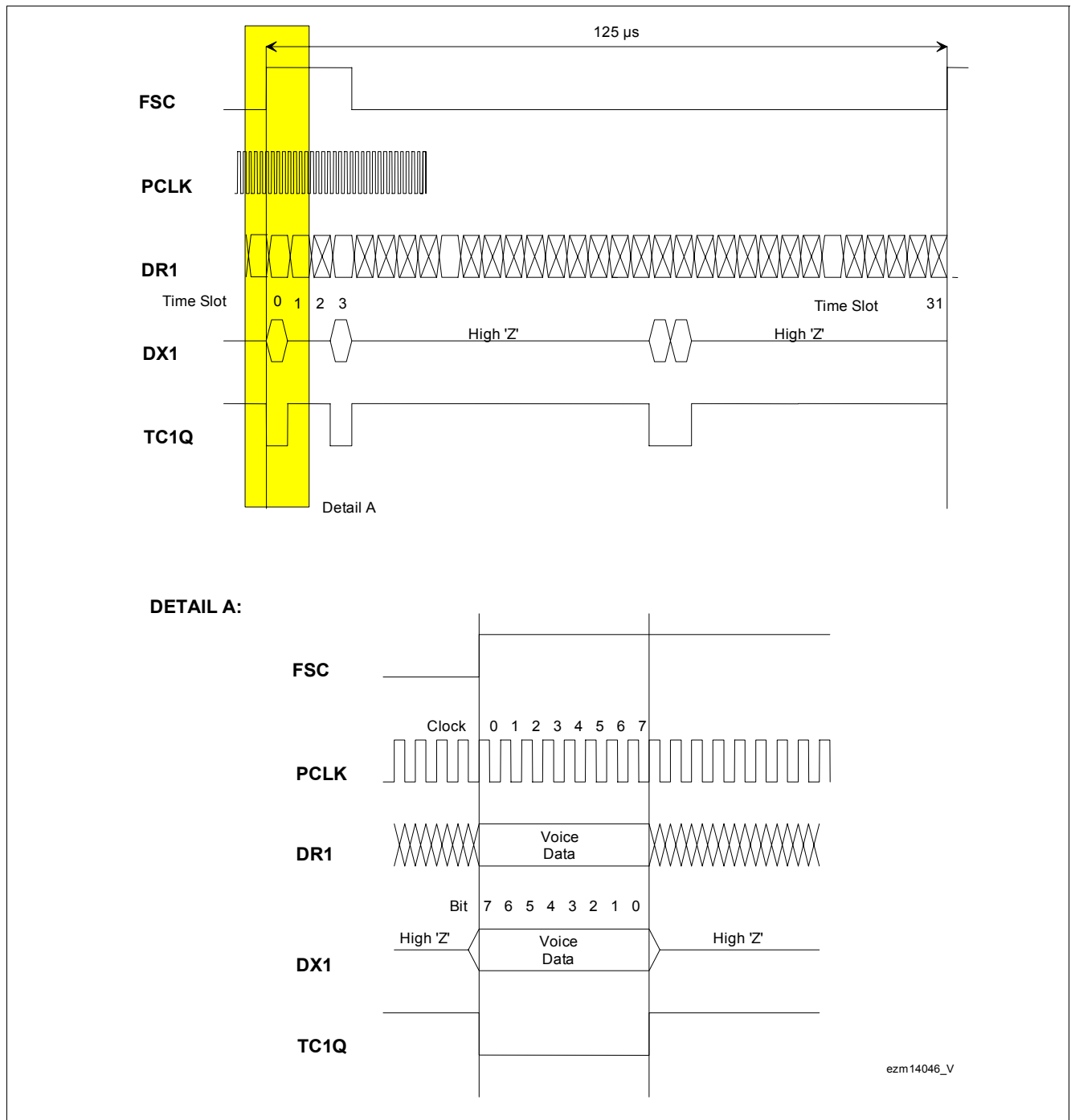


Figure 22 General PCM Interface Timing

The data rate of the interface can vary from 256 kbit/s to 8192 kbit/s. A frame may consist of up to 128 time slots of 8 bits each. The time slot assignment for each VINETIC®-2CPE/-1CPE channel can be programmed. Receive and transmit time slots can also be programmed individually (see [5]).

When the VINETIC®-2CPE/-1CPE is transmitting data on DX1, the TC1Q pin is switched to low to enable an external connected driving device.

Table 31 shows PCM interface frequency examples; other frequencies between 512 kHz and 8.192 MHz are also possible (such as 1536 kHz). The number of valid time slots is defined by the formulas at the end of **Table 31**:

Table 31 VINETIC®-2CPE/-1CPE PCM Interface Configuration

Clock Rate PCLK [kHz]	Single/Double Clock [1/2]	Time Slots [per highway]	Data Rate [kbit/s]
512	2	4	256
512	1	8	512
1024	2	8	512
1024	1	16	1024
2048	2	16	1024
2048	1	32	2048
4096	2	32	2048
4096	1	64	4096
8192	2	64	4096
8192	1	128	8192
$f = n \cdot 64 \cdot f_{FSC}, n \in [1, 16]^{1)}$	1	$f/64$	f
$f = n \cdot 64 \cdot f_{FSC}, n \in [1, 16]^{1)}$	2	$f/128$	$f/2$

1) n ... integer values, $f_{FSC} = 8 \text{ kHz}$

4.3.2 Timing, PCM Interface

4.3.2.1 Single-Clocking Mode

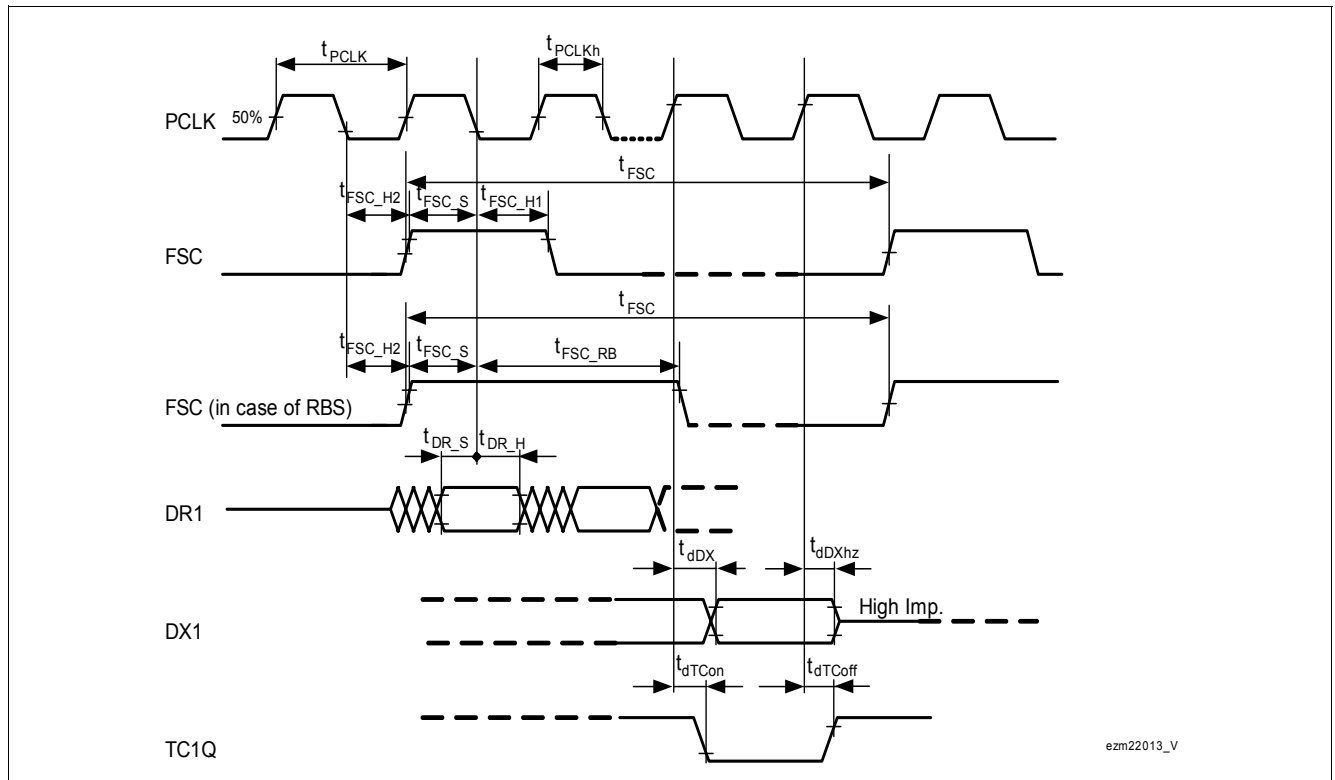


Figure 23 PCM Interface Timing – Single-Clocking Mode

Table 32 Timing Values, PCM Interface (Single-Clocking Mode)

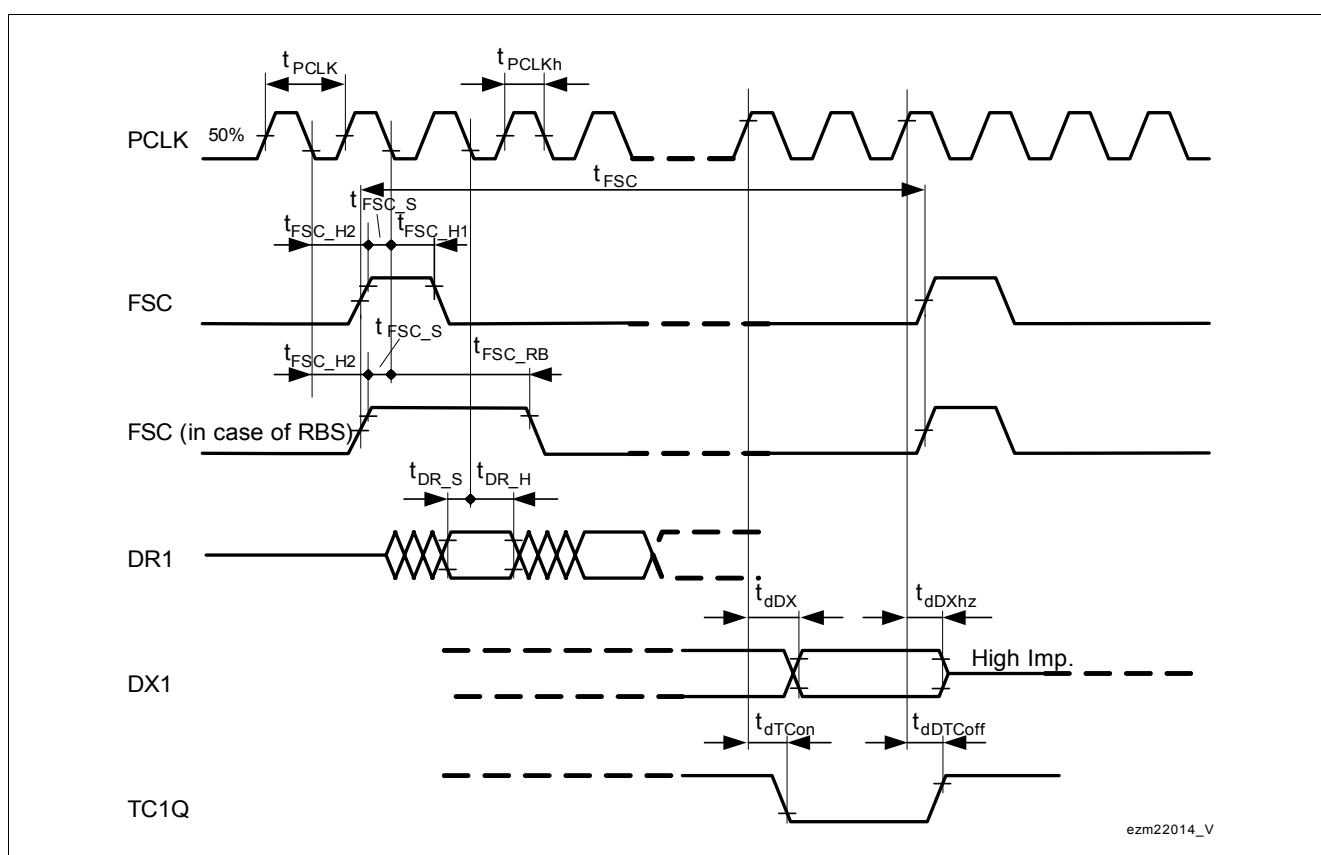
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Period PCLK ¹⁾	t_{PCLK}	1/8192	–	1/512	ms	–
PCLK high time	t_{PCLKh}	$0.4 \times t_{PCLK}$	–	$0.6 \times t_{PCLK}$	μ s	–
Period FSC ¹⁾	t_{FSC}	–	125	–	μ s	–
FSC setup time	t_{FSC_S}	10	–	–	ns	–
FSC hold time 1	t_{FSC_H1}	40	–	$t_{FSC} - t_{PCLK} - t_{FSC_S}$ ²⁾	ns	–
FSC hold time in case of RBS	t_{FSC_RB}	$t_{FSC_H1} + t_{PCLK}$	–	$t_{FSC} + 2 \times t_{PCLK} - t_{FSC_S}$ ²⁾	ns	–
FSC hold time 2	t_{FSC_H2}	40	–	–	ns	–
DR1 setup time	t_{DR_S}	10	–	–	ns	–
FSC jitter time		–	–	$\pm 0.2 \times t_{PCLK}$	ms	–
DR1 hold time	t_{DR_H}	10	–	–	ns	–
DX1 delay time ³⁾	t_{dDX}	25	–	$t_{dDX_min} + 0.4[\text{ns/pF}] \times C_{Load}[\text{pF}]$	ns	–
DX1 delay time to high Z	t_{dDXhz}	–	–	50	ns	–

Table 32 Timing Values, PCM Interface (Single-Clocking Mode) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TC1Q delay time on	t_{dTCon}	25	—	$t_{dTCon_min} + 0.4[ns/pF] \times C_{Load}[pF]$	ns	—
TC1Q delay time off	t_{dTCoFF}	25	—	$t_{dTCoFF_min} + 2 \times R_{Pullup}[k\Omega] \times C_{Load}[pF]$	ns	—

- 1) The PCLK frequency must be an integer multiple of the FSC frequency ($n \times 64 \times f_{FSC}$, $n = 1..16$).
- 2) This is to ensure that the FSC can be sampled low at least for one t_{PCLK} within t_{FSC} .
- 3) All delay times are made up of two components: an intrinsic time (min-time), caused by internal processing, and a second component caused by external circuitry (C_{Load} , $R_{Pullup} > 1.5\text{ k}\Omega$)

4.3.2.2 Double-Clocking Mode


Figure 24 PCM Interface Timing – Double-Clocking Mode
Table 33 Timing Values PCM Interface (Double-Clocking Mode)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Period PCLK ¹⁾	t_{PCLK}	1/8192	—	1/512	ms	—
PCLK high time	t_{PCLKh}	$0.4 \times t_{PCLK}$	—	$0.6 \times t_{PCLK}$	μs	—
Period FSC ¹⁾	t_{FSC}	—	125	—	μs	—

Table 33 Timing Values PCM Interface (Double-Clocking Mode) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FSC setup time	t_{FSC_S}	10	—	—	ns	—
FSC hold time 1	t_{FSC_H1}	40	—	$t_{FSC} - t_{PCLK} - t_{FSC_S}^{2)}$	ns	—
FSC hold time 2	t_{FSC_H2}	40	—	—	ns	—
FSC hold time in case of RBS	t_{FSC_RB}	$t_{FSC_H1} + t_{PCLK}$	—	$t_{FSC} + 2 \times t_{PCLK} - t_{FSC_S}^{2)}$	ns	—
FSC jitter time		—	—	$\pm 0.2 \times t_{PCLK}$	ms	—
DR1 setup time	t_{DR_S}	10	—	—	ns	—
DR1 hold time	t_{DR_H}	10	—	—	ns	—
DX1 delay time ³⁾	t_{dDX}	25	—	$t_{dDX_min} + 0.4[ns/pF] \times C_{Load}[pF]$	ns	—
DX1 delay time to high Z	t_{dDXhz}	—	—	50	ns	—
TC1Q delay time on	t_{dTCon}	25	—	$t_{dTCon_min} + 0.4[ns/pF] \times C_{Load}[pF]$	ns	—
TC1Q delay time off	t_{dTCoFF}	25	—	$t_{dTCoFF_min} + 2 \times R_{Pullup}[k\Omega] \times C_{Load}[pF]$	ns	—

1) The PCLK frequency must be an integer multiple of the FSC frequency ($n \times 64 \times f_{FSC}$, $n = 1..16$).

2) This is to ensure that the FSC can be sampled low at least for one t_{PCLK} within t_{FSC} .

3) All delay times are made up of two components: an intrinsic time (min-time), caused by internal processing, and a second component caused by external circuitry (C_{Load} , $R_{Pullup} > 1.5 \text{ k}\Omega$)

4.4 Test Interface (JTAG Interface)

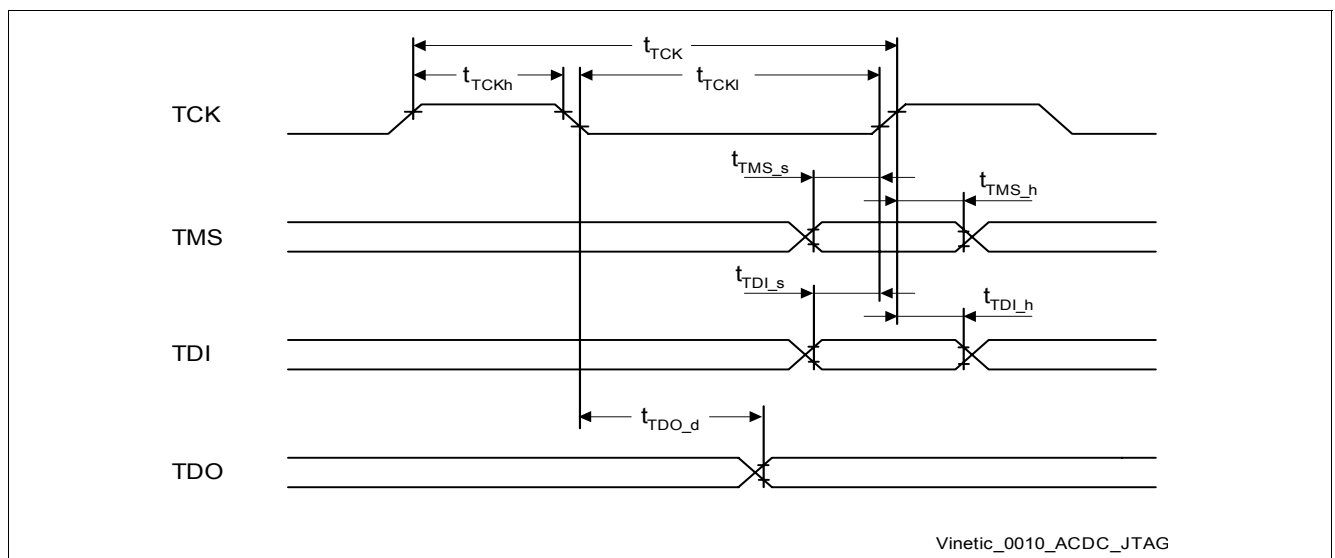

Figure 25 Test Interface (JTAG Interface) Timing

Table 34 Test Interface (JTAG Interface) Clocks

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK Clock Period	t_{TCK}	100	–	–	ns	Pin TCK
TCK High Time	t_{TCKh}	40	–	–	ns	–
TCK Low Time	t_{TCKl}	40	–	–	ns	–

Table 35 Test Interface (JTAG Interface) Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TMS setup time	t_{TMS_s}	40	–	–	ns	Pin TMS
TMS hold time	t_{TMS_h}	40	–	–	ns	–
TDI setup time	t_{TDI_s}	40	–	–	ns	Pin TDI
TDI hold time	t_{TDI_h}	40	–	–	ns	–
Hold: TRSTQ after TCK	t_{TRSTQ_h}	10	–	–	ns	Pin TRSTQ
TDO valid delay	t_{TDO_d}	100	–	$t_{dDOUT_min} + 0.4[ns/pF] \times C_{Load}[pF]$	ns	Pin TDO

4.5 SLIC Interface

The SLIC-DC (PEF 4268) Version 1.2 and the SLIC-E (PEB 4265, PEB 4365) Version 2.1 are controlled by ternary logic signals via the C1_x¹⁾ and C2_x¹⁾ pins.

For application circuits, please refer to [\[3\]](#).

1) x stands for A, B or just for A - the 2 or 1 analog channels of the VINETIC®-2CPE/-1CPE

5 Electrical Characteristics

5.1 Absolute Maximum Ratings VINETIC®-2CPE/-1CPE

Table 36 Absolute Maximum Ratings VINETIC®-2CPE/-1CPE

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply pins VDD15, VDD15_i ¹⁾ , VDD15P referred to the corresp. ground pins GND, GND15_i ¹⁾ , GND15P	—	−0.3	—	1.65	V	—
Supply pins VDD33, VDD33_x ²⁾ referred to the corresponding ground pins GND, GND33_x ²⁾	—	−0.3	—	3.63	V	—
Ground pins GND15_i ¹⁾ (GND33_x ²⁾) referred to any other ground pins GND15_j ¹⁾ , GND15P (GND33_y ²⁾)	—	−0.3	—	0.3	V	—
Supply pins VDD15, VDD15_i ¹⁾ referred to any other supply pin VDD15_j ¹⁾ , VDD15P	—	−0.3	—	0.3	V	—
Analog input and output pins Pins RING_x ²⁾ , TIP_x ²⁾ , IT_x ²⁾ , VCMIT_x ²⁾ , ITAC_x ²⁾ , ACP_x ²⁾ , ACN_x ²⁾	— —	−0.3 −0.3	— —	3.63 1.65	V V	$V_{DD33_x} = 3.3 \text{ V}$ $V_{DD15_i} = V_{DD15P} = 1.5 \text{ V}$ $V_{GND15_i} = V_{GND15P} = V_{GND33_x} = 0 \text{ V}$
Digital input and output pins	—	−0.3	—	3.63	V	$V_{DD33} = 3.3 \text{ V}$, $V_{DD15} = 1.5 \text{ V}$, $V_{GND} = 0 \text{ V}$
Digital input leakage current per pin	I_L	−50	—	50	μA	$0 \leq V_{in} \leq V_{DD33}$
DC input or output current at any input or output pin	—	—	—	100	mA	(free from latch-up)
Storage temperature	T_{STG}	−55	—	125	°C	—
Ambient temperature under bias	T_A	0	—	85	°C	—
Maximum junction temperature	T_J	—	—	125	°C	—
Power dissipation ³⁾	P_D	—	—	0.8	W	PG-TQFP-100-3 and PG-TQFP-100-18
				1.1	W	PG-TQFP-64-8

ESD Robustness

Table 36 Absolute Maximum Ratings VINETIC®-2CPE/-1CPE

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ESD voltage	—	—	—	2	kV	Human body model ⁴⁾
ESD voltage, all pins	—	—	—	0.5	kV	SDM (Socketed Device Model) ⁵⁾

- 1) i, j = A, AB, B
2) x, y = A, B
3) According to JEDEC (four-layer board)
4) MIL STD 883D, method 3015.7 and ESD Assn. Standard S5.1-1993
5) EOS/ESD Assn. Standard DS5.3-1993

5.2 Operating Range VINETIC®-2CPE/-1CPE

$$V_{\text{GND}} = V_{\text{GND15_A}} = V_{\text{GND15_B}} = V_{\text{GND15_AB}} = V_{\text{GND15P}} = V_{\text{GND33_A}} = V_{\text{GND33_B}} = 0 \text{ V}$$

Table 37 Operating Range VINETIC®-2CPE/-1CPE

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply pins VDD15, VDD15_i ¹⁾ , VDD15P referred to the corresp. ground pins GND, GND15_i ¹⁾ , GND15P		1.425	1.5	1.575	V	—
Supply pins VDD33, VDD33_x ²⁾ referred to the corresponding ground pins GND, GND33_x ²⁾		3.135	3.3	3.465	V	—
Analog input pins RING_x ²⁾ , TIP_x ²⁾ , IT_x ²⁾ referred to the corresp. pin VCMIT_x ²⁾		−0.5	—	0.5	V	$V_{\text{DD15_i}} = 1.5 \text{ V}$
Analog input pin ITAC_x ²⁾ referred to the corresp. pin VCMIT_x ²⁾		−0.11	—	0.11	V	$V_{\text{DD15_i}} = 1.5 \text{ V}$
Analog output pins: DCP_x ²⁾ , DCN_x ²⁾ ACP_x ²⁾ , ACN_x ²⁾ C1_x ²⁾ , C2_x ²⁾ referred to the corresp. ground pins GND15_x ²⁾ , GND33_x ²⁾		0.25 0.2 0	— — —	2.75 1.2 3.3	V V V	$V_{\text{DD33_x}} = 3.3 \text{ V}$, $V_{\text{DD15_i}} = 1.5 \text{ V}$ $R_{\text{Load}} > 100 \text{ k}\Omega$ $R_{\text{Load}} > 20 \text{ k}\Omega$ $I_{\text{Load}} < 220 \mu\text{A}$
Analog pin VCMIT_x ²⁾ referred to the corresp. ground pin GND15_x ²⁾		—	0.7	—	V	$V_{\text{DD15_AB}} = 1.5 \text{ V}$
Analog pin for passive devices CREF_AB referred to the corresp. ground pin GND15_AB		0.5	0.7	0.9	V	$V_{\text{DD15_AB}} = 1.5 \text{ V}$

Digital input/output pins (I/O pins, GPIO pins)

High-level input voltage	V_{IH}	2.0	—	3.6	V	$V_{\text{OUT}} \geq V_{\text{OH}} (\text{min})$
Low-level input voltage	V_{IL}	−0.3	—	0.8	V	$V_{\text{OUT}} \leq V_{\text{OL}} (\text{max})$

Table 37 Operating Range VINETIC®-2CPE/-1CPE (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
High-level output voltage	V_{OH}	2.4	–	–	V	$I_{OH} = -3 \text{ mA}$
Low-level output voltage	V_{OL}	–	–	0.4	V	$I_{OL} = 3 \text{ mA}$
Average input leakage current per pin	I_{IL}	–	–	20	μA	$V_{DD33} = 3.3 \text{ V}$, $V_{GND} = 0 \text{ V}$; all other pins are floating, $V_{IN} = 0 \text{ V}$ or 3.3 V , V_{IN} for pins RING _{x²} , TIP _{x²} = 0 V or 1.5 V
Input capacitance at digital signal pins (except RING _{x²} , TIP _{x²})		–	–	5	pF	–
Input transition rise or fall time at digital signal pins (except RING _{x²} , TIP _{x²})		0	–	5	ns	–
Pull-up resistor on chip	$R_{\text{pull-up}}$	–	500	–	k Ω	–
Digital input pins (IFSEL0, IFSEL1)³⁾						
Pull up current ⁴⁾		–3	–6.6	–15	μA	$V_{\text{pin}} = 0 \text{ V}$
Analog input pins (RING_{x²}, TIP_{x²})						
Input impedance (RING _{x²} , TIP _{x²}): single input measurement (RING _{x²} , TIP _{x²} to GND15 _{x²})	$R_{\text{RTinS}}^{5)}$	600	750	900	k Ω	
Input impedance (RING _{x²} , TIP _{x²}): differential measurement (RING _{x²} to TIP _{x²})	$R_{\text{RTinD}}^{5)}$	1200	1500	1800	k Ω	
Input impedance (RING _{x²} , TIP _{x²}): differential measurement (RING _{x²} , TIP _{x²} to VCMIT _{x²})	$R_{\text{RTinD}}^{5)}$	800	1000	1200	k Ω	
Ambient temperature under bias	T_A	0	–	85	°C	–
Junction temperature under bias	T_J	0	–	125	°C	–

1) i = A, AB, B

2) x = A, B

3) only available in PG-TQFP-100-3 and PG-TQFP-100-18

4) On chip pull-up resistor

5) Not subject for production test - verified by design/characterization

5.2.1 Thermal Resistance VINETIC®-2CPE/-1CPE

Table 38 Thermal Resistance VINETIC®-2CPE/-1CPE

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Junction to case	R_{th}	–	10	–	K/W	PG-TQFP-100-3 and PG-TQFP-100-18
		–	12.5	–		PG-TQFP-64-8
Junction to Ambient for 4 Layer- 100x100 JEDEC Board	R_{th}	–	44.1	–	K/W	PG-TQFP-100-3 and PG-TQFP-100-18
		–	35.3	–		PG-TQFP-64-8

5.2.2 Power Consumption VINETIC®-2CPE/-1CPE

$T_A = 0\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$, unless otherwise stated.

$$V_{DD15} = V_{DD15_A} = V_{DD15_B} = V_{DD15_AB} = V_{DD15P} = 1.5\text{ V} \pm 5\%$$

$$V_{DD33} = V_{DD33_A} = V_{DD33_B} = 3.3\text{ V} \pm 5\%$$

$$V_{GND} = V_{GND15_A} = V_{GND15_B} = V_{GND15_AB} = V_{GND15P} = V_{GND33_A} = V_{GND33_B} = 0\text{ V}$$

Table 39 Power Consumption VINETIC®-2CPE

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power consumption in operation modes ¹⁾						
Deep Sleep	$P_{DDSleep}$	—	20	t.b.d.	mW	—
Power down (PDH) all channels	$P_{DDPDH, 1.5\text{ V}}$	—	60	t.b.d.	mW	Basic EDSP load of ~20 Mcycles/s included, EDSP Idle Mode on
	$P_{DDPDH, 3.3\text{ V}}$	—	10 ²⁾	t.b.d.	mW	
On-Hook (ONHOOK) all channels	$P_{DDONHK, 1.5\text{ V}}$	—	62	t.b.d.	mW	Basic EDSP load of ~20 Mcycles/s included, EDSP Idle Mode on
	$P_{DDONHK, 3.3\text{ V}}$	—	10 ²⁾	t.b.d.	mW	
Active one channel, Power Down (PDH) other channel	$P_{DDACTPDH, 1.5\text{ V}}$	—	98 ³⁾	t.b.d.	mW	Basic EDSP load plus 1ch. ALM and PCM load of ~26 Mcycles/s included, EDSP Idle Mode on
	$P_{DDACTPDH, 3.3\text{ V}}$	—	20 ²⁾	t.b.d.	mW	
Active one channel, On-Hook (ONHOOK) other channel	$P_{DDACTPDH, 1.5\text{ V}}$	—	100 ³⁾	t.b.d.	mW	Basic EDSP load plus 1ch. ALM and PCM load of ~26 Mcycles/s included, EDSP Idle Mode on
	$P_{DDACTPDH, 3.3\text{ V}}$	—	20 ²⁾	t.b.d.	mW	
Active (ACT) all channels	$P_{DDACT, 1.5\text{ V}}$	—	125 ³⁾	t.b.d.	mW	Basic EDSP load plus 2ch. ALM and PCM load of ~26 Mcycles/s included, EDSP Idle Mode on
	$P_{DDACT, 3.3\text{ V}}$	—	25 ²⁾	t.b.d.	mW	

Table 39 Power Consumption VINETIC®-2CPE (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EDSP module ⁴⁾						
Active	$P_{\text{DDEDS},1.5\text{ V}}$	—	1.5	—	mW/Mcycles	EDSP power consumption, max. EDSP load: 163.8 Mcycles/s

- 1) To calculate total power consumption, the values for both supply voltages (3.3 V and 1.5 V) have to be summed up.
- 2) Depends on the external load.
- 3) Depends on the EDSP load used.
- 4) For estimation of power consumption with different EDSP loads.

Table 40 Power Consumption VINETIC®-1CPE

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power consumption in operation modes ¹⁾						
Deep Sleep	$P_{DDDSleep}$	—	20	t.b.d.	mW	—
Power down (PDH)	$P_{DDPDH,1.5\text{ V}}$	—	56	t.b.d.	mW	Basic EDSP load of ~20 Mcycles/s included, EDSP Idle Mode on
	$P_{DDPDH,3.3\text{ V}}$	—	10 ²⁾	t.b.d.	mW	
On-Hook (ONHOOK)	$P_{DDONHK,1.5\text{ V}}$	—	58	t.b.d.	mW	Basic EDSP load of ~20 Mcycles/s included, EDSP Idle Mode on
	$P_{DDONHK,3.3\text{ V}}$	—	10 ²⁾	t.b.d.	mW	
Active (ACT)	$P_{DDACT,1.5\text{ V}}$	—	90 ³⁾	t.b.d.	mW	Basic EDSP load plus 1ch. ALM and PCM load of ~26 Mcycles/s included, EDSP Idle Mode on
	$P_{DDACT,3.3\text{ V}}$	—	20 ²⁾	t.b.d.	mW	
EDSP module ⁴⁾						
Active	$P_{DDEDSP,1.5\text{ V}}$	—	1.5	t.b.d.	mW/Mcycles	EDSP power consumption, max. EDSP load: 263.8 Mcycles/s

- 1) To calculate total power consumption, the values for both supply voltages (3.3 V and 1.5 V) have to be summed up.
- 2) Depends on the external load.
- 3) Depends on the EDSP load used.
- 4) For estimation of power consumption with different EDSP loads.

5.2.3 Power-On Sequence VINETIC®-2CPE/-1CPE

No power-on sequence must be performed for the VDD15¹⁾ and VDD33²⁾ supply voltages. It is mandatory to apply the signal voltages after the VDD15 and VDD33 voltages are supplied and stable.

5.3 Transmission Characteristics VINETIC®-2CPE/-1CPE

The AC transmission characteristics are specified in [5] and are referred to a complete system including the SLIC-DC Version 1.2 and external components.

1) VDD15, VDD15_A, VDD15_B, VDD15_AB

2) VDD33, VDD33_A, VDD33_B

6 Package Outlines

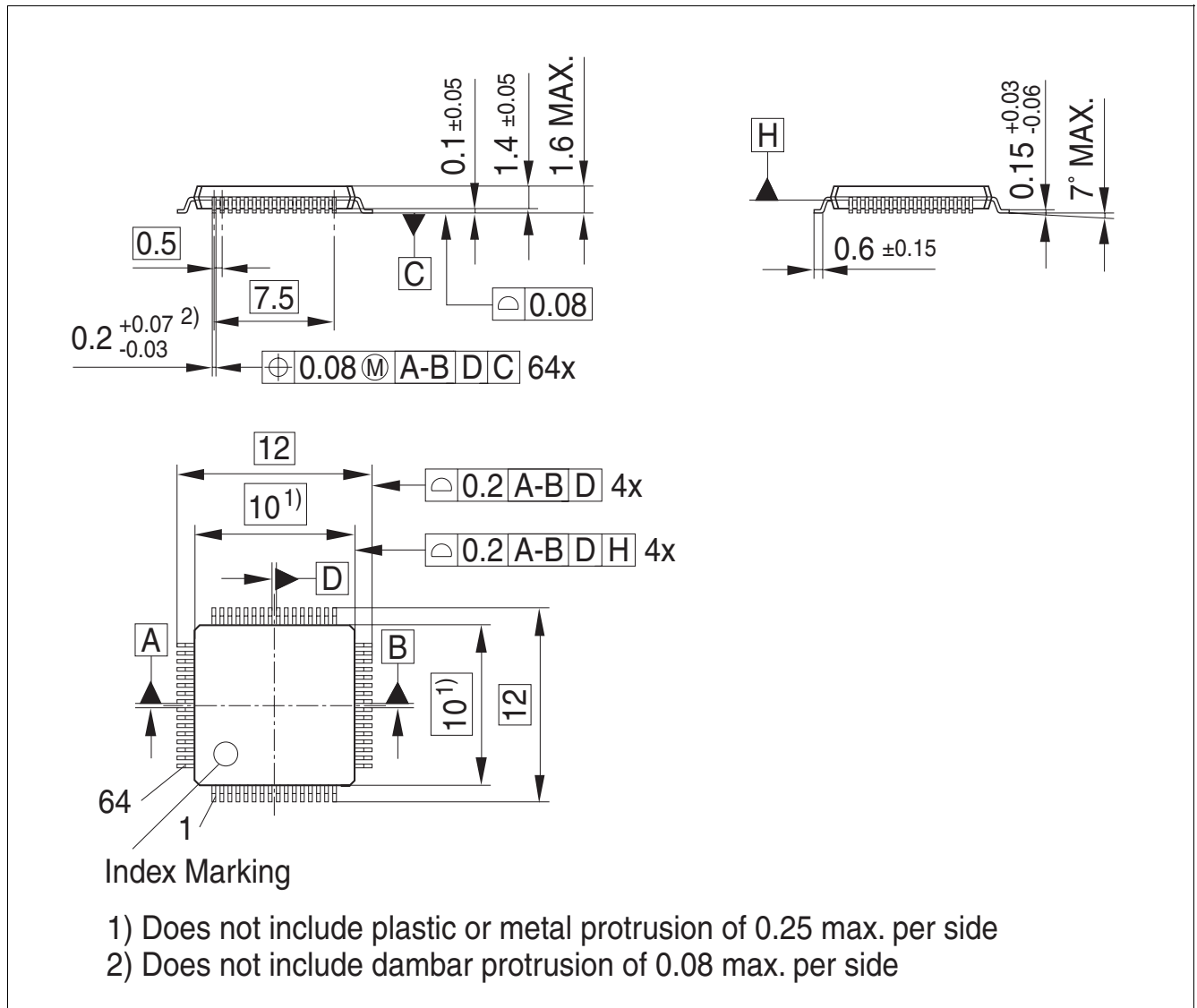


Figure 26 PG-TQFP-64-8 (Plastic Green Thin Quad Flat Package)

Dimensions in mm

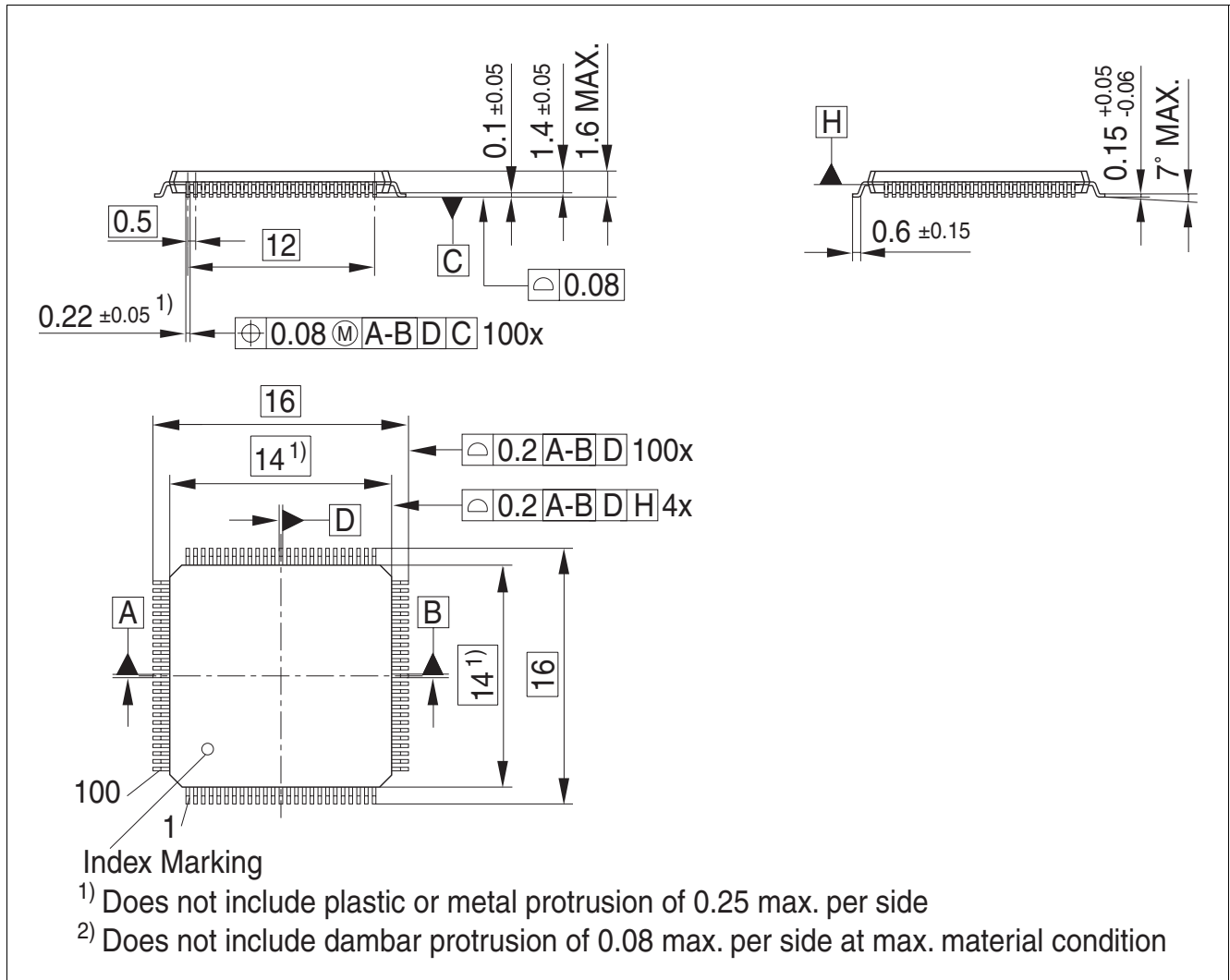


Figure 27 PG-TQFP-100-3 and PG-TQFP-100-18 (Plastic Green Thin Quad Flat Package)

Attention: The dimensions of the PG-TQFP-100-3 and PG-TQFP-100-18 packages are identical.

Dimensions in mm

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Terminology

A

A/D	Analog to digital
AAL2	ATM Adaption Layer 2
AC	Alternative Current
ADC	Analog Digital Converter
AITDF	Advanced Integrated Test and Diagnostic Functions
ALM	Analog Line Module
ATD	Answering Tone Detector
ATM	Asynchronous Transfer Mode

C

CAS	Channel Associated Signaling
CNG	Comfort Noise Generation
Codec	Coder Decoder
CPE	Customer Premises Equipment
CRAM	Coefficient RAM

D

DAA	Data Access Arrangement
DAC	Digital Analog Converter
DC	Direct Current
DSP	Digital Signal Processor
DTMF	Dual Tone Multi Frequency

E

EXP	Expander
-----	----------

F

FRR	Frequency Response Receive filter
FRX	Frequency Response Transmit filter
FSK	Frequency Shift Keying
FXO	Foreign eXchange Office
FXS	Foreign eXchange Subscriber

G

GPIO	General Purpose Input/Output
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H

HW	Hardware
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I

IAD	Integrated Access Device
ITU	International Telecommunication Union
IP	Internet Protocol
ISDN	Integrated Services Digital Network

J

JTAG	Joint Test Action Group
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L

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LSSGR	Local area transport access Switching System Generic Requirements
N	
NG-DLC	Next Generation Digital Loop Carrier
NT	Network Terminal
P	
PBX	Private Branch eXchange
PCM	Pulse Code Modulation
POTS	Plain Old Telephone Service
R	
RAM	Random Access Memory
RBS	Robbed Bit Signaling
RTCP	Real-time Transport Control Protocol
RTP	Real-time Transport Protocol
S	
SLIC	Subscriber Line Interface Circuit (same for all versions)
SOHO	Small Office/Home Office
T	
TG	Tone Generator
TH	Transhybrid Balancing
TS	Time Slot
TTX	Teletax (Metering)
U	
UTD	Universal Tone Detection
UTG	Universal Tone Generator
V	
VAD	Voice Activity Detection
VINETIC®	Voice and Internet Enhanced Telephony Interface Concept
VINETICOS	Voice and Internet Enhanced Telephony Interface Concept Coefficients Calculation Software
VoATM	Voice over ATM
VoDSL	Voice over DSL
VoIP	Voice over IP
X	
xDSL	(all flavors of) Digital Subscriber Line

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References

- [1] VINETIC®-2CPE (PEB 3332) Version 1.4 Prel. Data Sheet Rev. 3.0, 2005-07-18
- [2] VINETIC®-CPE Version 2.1 Device Driver Prel. User's Manual Driver and API Rev. 1.0, in preparation
- [3] VINETIC®-2CPE/-1CPE (PEB 3332/-3331) Version 2.1 Hardware Design Guide Rev. 1.0, in preparation
- [4] VINETIC®-CPE Version 2.1 Device Driver Porting and Integration Guide Rev. 1.0, in preparation
- [5] VINETIC®-CPE Version 2.1 Prel. User's Manual System Description Rev. 1.0, in preparation

Note: Preliminary Draft Versions of Documents are available on request for [\[2\]](#), [\[3\]](#) and [\[4\]](#) until the documents are released.

Attention: Please refer to the latest revision of the documents.

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