August 2006

VINETIC®-CPE

Voice over IP Processor for Customer Premises Equipment

VINETIC®-2ATA (PEB 3342), Version 2.2
VINETIC®-1ATA (PEB 3341), Version 2.2
VINETIC®-CL (PEB 3340), Version 2.2
VINETIC®-0 (PEB 3320), Version 2.2

Preliminary

Data Sheet

Revision 1.0

Communication Solutions

Never stop thinking

Edition 2006-08-07

Published by
Infineon Technologies AG
81726 München, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”). With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

VINETIC®-CPE, Voice over IP Processor for Customer Premises Equipment
CONFIDENTIAL
Revision History: 2006-08-07, Revision 1.0

Previous Version: VINETIC®-2ATA/-1ATA/-CL/-0 Version 2.1 Prel. Data Sheet Rev. 1.0, 2006-03-07

Page	Subjects (major changes since last revision)
all	Chip version changed from Version 2.1 to Version 2.2
10	**"Family Overview" on Page 10**: PG-TQFP-64-8 and PG-TQFP-100-3 removed
11	**"Integrated DSP Features" on Page 11**: 4-channel Line Echo Cancellation added
12	**"CODEC/SLIC Features" on Page 12**: DC feeding capability added
36	**Table 17 "Absolute Maximum Rating Parameters NOT VALID for VINETIC®-CL/VINETIC®-0" on Page 36**: DCP_x and DCN_x added (missing in previous revision)
37	**Table 19 "Power Consumption Parameters for VINETIC®-CL/VINETIC®-0" on Page 37**: Max. Values added for Power Consumption (values were "tbd" in previous revision)
39	**"Literature References" on Page 39** updated

Trademarks

ABM®, ACE®, AOP®, Arcofi®, ASM®, ASP®, BlueMoon®, BlueNIX®, C166®, DuSLIC®, ELIC®, Epic®, FALC®, GEMINAX®, Idec®, INCA®, IOM®, Ipat®-2, IPVD®, Isac®, Itac®, IWE®, IWORX®, M-GOLD®, MUSAC®, MuSLIC®, OCTALFALC®, OCTAT®, POTSWIRE®, QUADFALC®, QUAT®, SCOUT®, SCT®, SEROCCO®, S-GOLD®, SICAT®, SICOFI®, SIDEC®, SIEGET®, SLICOFI®, SMARTI®, SOCRATES®, VDSLite®, VINETIC®, 10BaseS® are registered trademarks of Infineon Technologies AG.

ConverGate™, DIGITAPE™, DUALFALC™, EasyPort™, S-GOLDlite™, S-GOLD2™, S-GOLD3™, VINAX™, WildPass™, 10BaseV™, 10BaseVX™ are trademarks of Infineon Technologies AG.

Microsoft® and Visio® are registered trademarks of Microsoft Corporation. Linux® is a registered trademark of Linus Torvalds. FrameMaker® is a registered trademark of Adobe Systems Incorporated. APOXI® is a registered trademark of Comneon GmbH & Co. OHG. PrimeCell®, RealView®, ARM® are registered trademarks of ARM Limited. OakDSPCore®, TeakLite® DSP Core, OCEM® are registered trademarks of ParthusCeva Inc.

IndoorGPS™, GL-20000™, GL-LN-22™ are trademarks of Global Locate. ARM926EJ-S™, ADS™, Multi-ICE™ are trademarks of ARM Limited.

Table of Contents

List of Figures

List of Tables

Preface

This Preliminary Data Sheet describes the following members of the VINETIC® CPE (Customer Premises Equipment) codec family:

- VINETIC®-2ATA/-1ATA (PEB 3342/-3341) Version 2.2,
- VINETIC®-CL (PEB 3340) Version 2.2,
- VINETIC®-0 (PEB 3320) Version 2.2

This document can only be used together with the latest revision VINETIC®-2CPE/-1CPE (PEB/PEF 3332/-3331) Version 2.2 Prel. Data Sheet Rev. 1.0, 2006-07-07 (further refered to as **[1]**):

If the information in **[1]** is valid for this document, only a reference is used.

If the information in **[1]** is incomplete or not applicable, please follow the instructions within this document.

To simplify matters, the following synonyms and shortcuts are used:

VINETIC®-x

Synonym used for the CODEC versions VINETIC®-2ATA/-1ATA Version 2.2, VINETIC®-CL Version 2.2 and VINETIC®-0 Version 2.2.

SLIC

Synonym used for SLIC-DC Version 1.2.

PG-TQFP-100

Synonym used for the package PG-TQFP-100-18

PG-TQFP-64

Synonym used for the package PG-TQFP-64-17

i, x

Shortcut for pin names and related voltages

i = A, B, AB; x = A, B

Example: ITAC_x = ITAC_A, ITAC_B

Organization of this Document

This document is divided into 6 chapters. It is organized as follows:

- **Chapter 1**, **Family Overview**
  A general description of the chip set, key features/requirements, and typical applications.
- **Chapter 2**, **Pin Description**
  Pin layout and pin description.
- **Chapter 3**, **Hardware Behavior and Handling**
  Description of clocking, reset behavior, and test modes.
- **Chapter 4**, **Interface Description**
  Parallel (Intel, Motorola) and serial interfaces (PCM, SCI/SPI).
- **Chapter 5**, **Electrical Characteristics**
  Parameters, symbols, and limit values.
- **Chapter 6**, **Package Outlines**
  Illustrations and dimensions of the package outlines.
- **Literature References** and **Standards References**
  List of referenced documents.
- **Terminology**
  List of abbreviations and descriptions of symbols.

CONFIDENTIAL

Voice and Internet Enhanced Telephony Interface Circuit
VINETIC®-2ATA
VINETIC®-1ATA
VINETIC®-CL
VINETIC®-0

PEB 3342
PEB 3341
PEB 3340
PEB 3320

Version 2.2

1 Family Overview

For a detailed overview please refer to [1].

PG-TFQP-64-17

PG-TFQP-100-18

Product Name	Product Type	Package
VINETIC®-2ATA/-1ATA	PEB 3342/-3341 F	PG-TQFP-64-17
	PEB 3342/-3341 HT	PG-TQFP-100-18
VINETIC®-CL	PEB 3340 F	PG-TQFP-64-17
	PEB 3340 HT	PG-TQFP-100-18
VINETIC®-0	PEB 3320 F	PG-TQFP-64-17
	PEB 3320 HT	PG-TQFP-100-18

1.1 Features VINETIC®-2ATA/-1ATA/-CL/-0

Table 1 Features VINETIC®-2ATA/-1ATA/-CL/-0

Feature	-ATA	-CL	-0
Fully programmable 2- and 1-channel CODEC with enhanced signal-processing capabilities	yes	-	-
Glueless interface to the Infineon SLIC-DC Version 1.2	yes	-	-

1.1.1 Integrated DSP Features

Table 2 Integrated DSP Features

Feature	-ATA	-CL	-0
Integrated VoIP DSP with RAM and software download capability	yes	yes	yes
Enhanced signal processing	yes	yes	yes
Voice coding: G.711, G.711 Annex I (Packet Loss Concealment), G.711 Annex II (VAD + CNG), G.723.1, G.726, G.729 A, B, G.729 E, iLBC royalty free vocoder	yes	yes	yes
4(2) VoIP channels with low-bitrate vocoding implemented in 2-channel (1-channel) device	2 chan.	2 chan.	4. chan.
RTP/RTCP packetization (packetization time programmable: 5 to 30 ms encoding, 5 to 60 ms decoding)	yes	yes	yes
Voice Activity Detection (VAD)	yes	yes	yes
Comfort Noise Generation (CNG)	yes	yes	yes
Algorithms for Line Echo Cancellation (LEC) exceeding G.165, G.168, G.168-2002/2004: • 4-channel Near End Line Echo Cancellation (NLEC) up to 16 ms tail length (programmable) • 4-channel Window-Based Line Echo Cancellation (WLEC) up to 128 ms tail length (programmable)	 yes -	 - -	 yes yes
Integrated DTMF generator	yes	yes	yes
Integrated DTMF receiver	yes	yes	yes
Integrated Caller ID (with Frequency Shift Keying (FSK)) generator according to V.23 and Bell 202	yes	yes	yes
Integrated fax/modem detection, In-band tone detection	yes	yes	yes
Multi-party conferencing	yes	yes	yes
T.38 Fax relay support with V.17, V.21, V.27ter, V.29	yes	-	yes
Voice play-out (reordering, fixed and adaptive jitter buffer up to 200 ms, clock synchronization)	yes	yes	yes
Universal Tone Generator (UTG) including all Japanese tones	yes	yes	yes
Call Progress Tone Detector	yes	yes	yes
Caller-ID Detector for V.23 and Bell 202	yes	yes	yes

1.1.2 CODEC/SLIC Features

Table 3 CODEC/SLIC Features

Feature	-ATA	-CL	-0
Specification in accordance with ITU-T Recommendation Q.552 for interface Z [4], ETSI Standard ES 202 971[3] and others	yes	-	-
Internal ringing capability	yes	-	-
Sinusoidal ringing	yes	-	-
Loop start signaling	yes	-	-
Polarity reversal	yes	-	-
Automatic modes for POTS signaling	yes	-	-
DC feeding capability according to ETSI Standard ES 202971 [3] and Telcordia GR-909-CORE [5]	yes	-	-
On-hook transmission	yes	-	-
Direct connection of DAA solution possible (FXO)	yes	-	yes

1.1.3 Interface Features

Table 4 Interface Features

Feature	-ATA	-CL	-0
PCM interface with one PCM highway	yes	yes	yes
Serial control interface, SCI (Infineon) compatible, SPI compatible	yes	yes	yes
Parallel host interface: Intel/Motorola compatible	yes	yes	yes
JTAG interface for boundary scan	yes	yes	yes

1.2 Typical Applications

The VINETIC®-x and SLIC-DC system is dedicated primarily to Customer Premises Equipment (CPE) and provides solutions for the following applications:

Table 5 Typical Applications

Feature	-ATA	-CL	-0
Access Network			
FTTH - VoIP	-	-	yes
WLL - VoIP	-	-	yes
CPE			
Residential Gateway/Home Gateway/Internet Telephony Gateway (ITG) - VoIP	yes	yes	yes
VoIP DECT Phone (base station)	-	yes	-
Integrated Access Device (IAD) - VoIP	yes	-	yes
Integrated Access Device (IAD) - VoIP with DECT	-	yes	-
Cable Modems/Media Terminal Adapter (MTA) - VoIP	yes	-	yes
Analog Telephony Adapter (ATA) - VoIP	yes	-	yes
Router - VoIP	yes	yes	-
SOHO IP PBX	yes	-	yes

1.3 Logic Symbols

1.3.1 Logic Symbols VINETIC®-2ATA

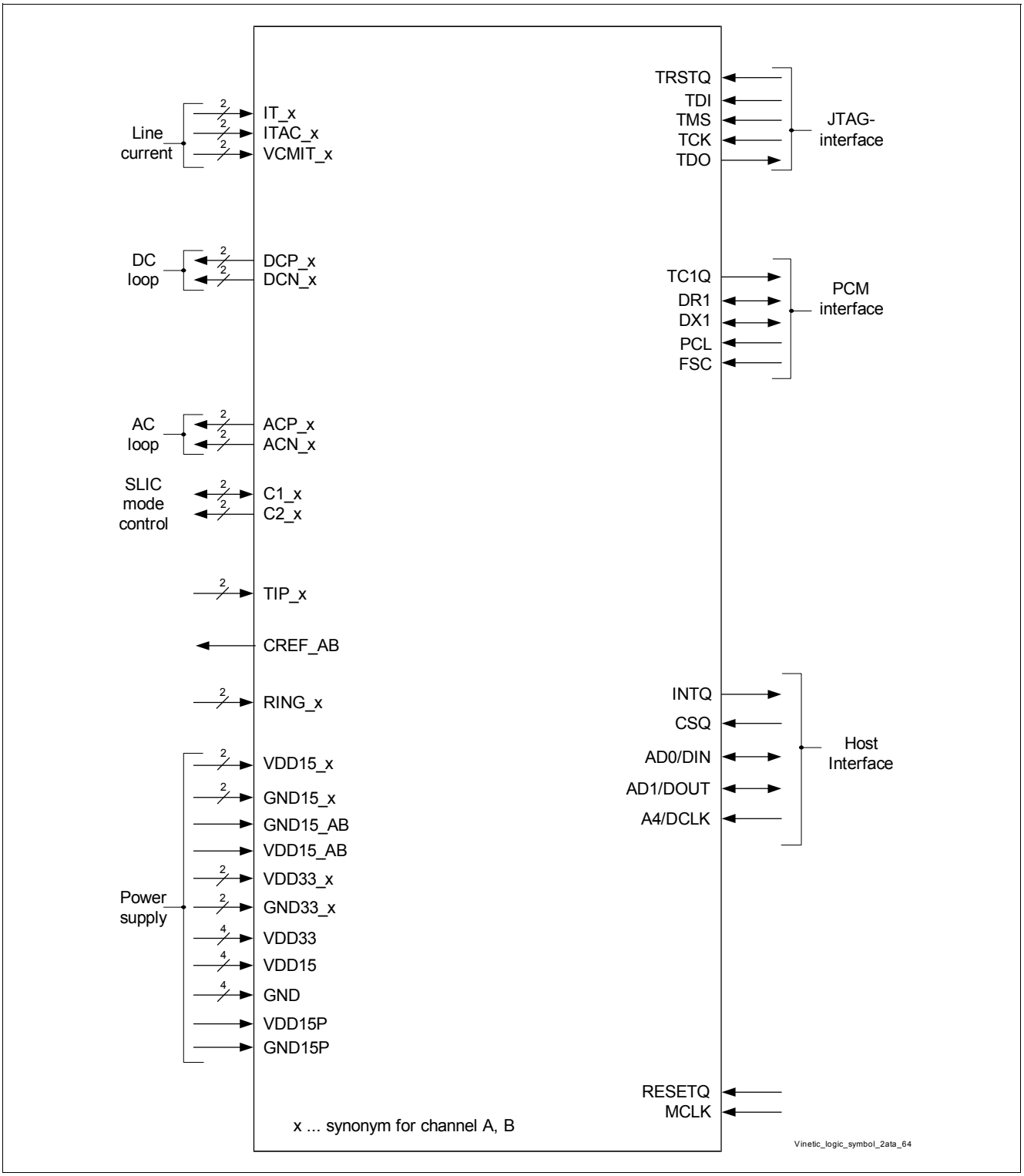

Figure 1 Logic Symbol for VINETIC®-2ATA (PG-TQFP-64)

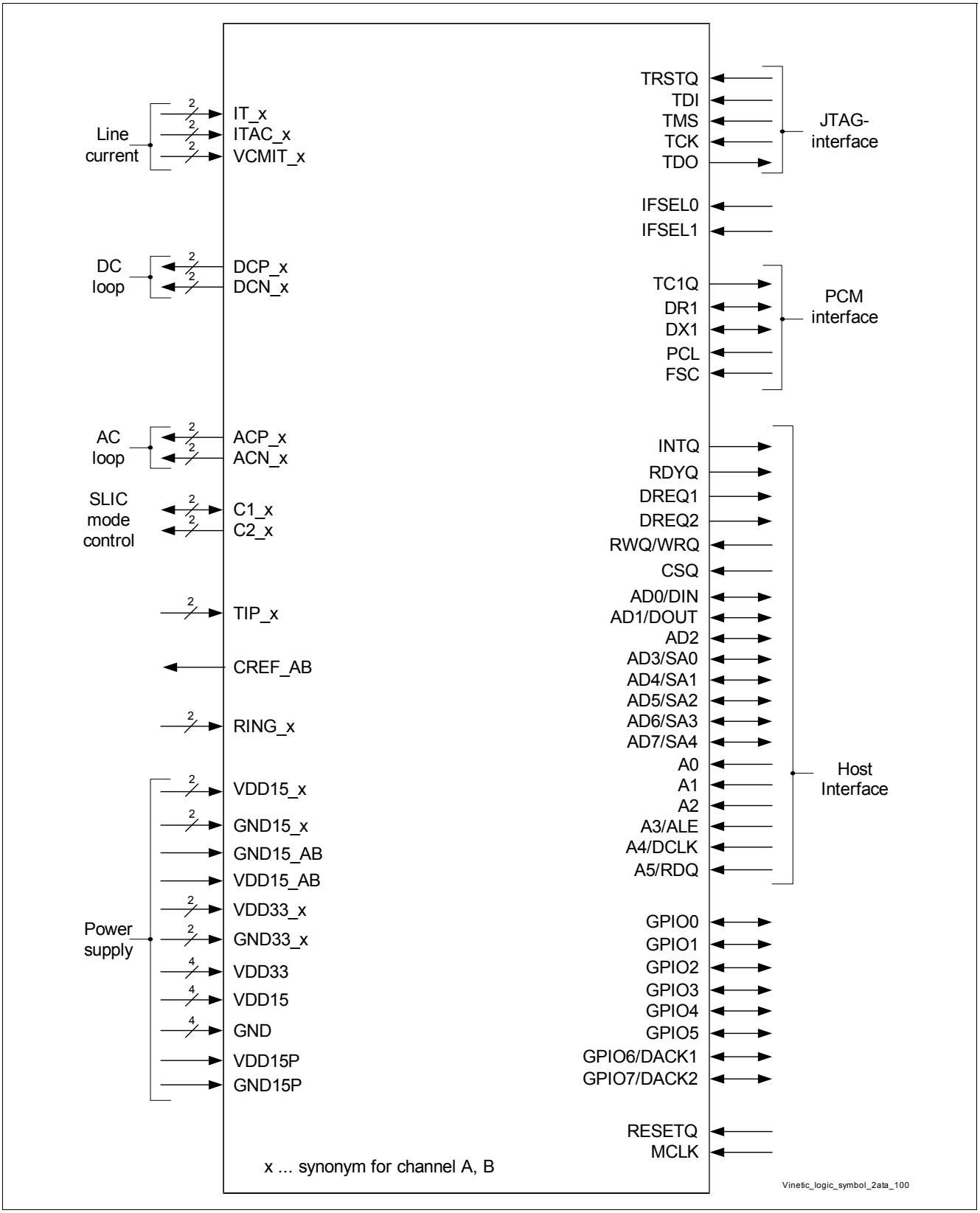

Figure 2 Logic Symbol for VINETIC®-2ATA (PG-TQFP-100)

1.3.2 Logic Symbols VINETIC®-1ATA

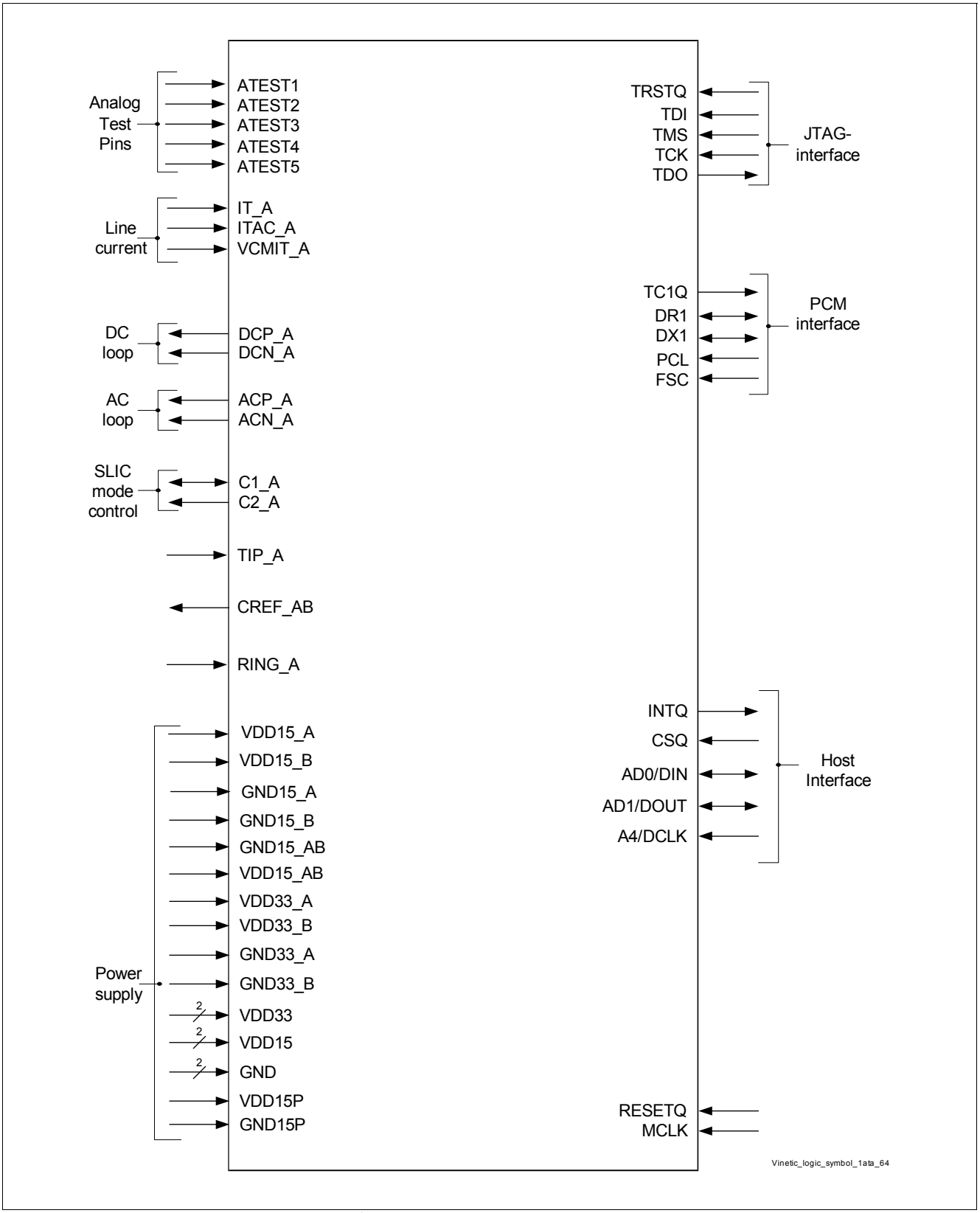

Figure 3 Logic Symbol for VINETIC®-1ATA (PG-TQFP-64)

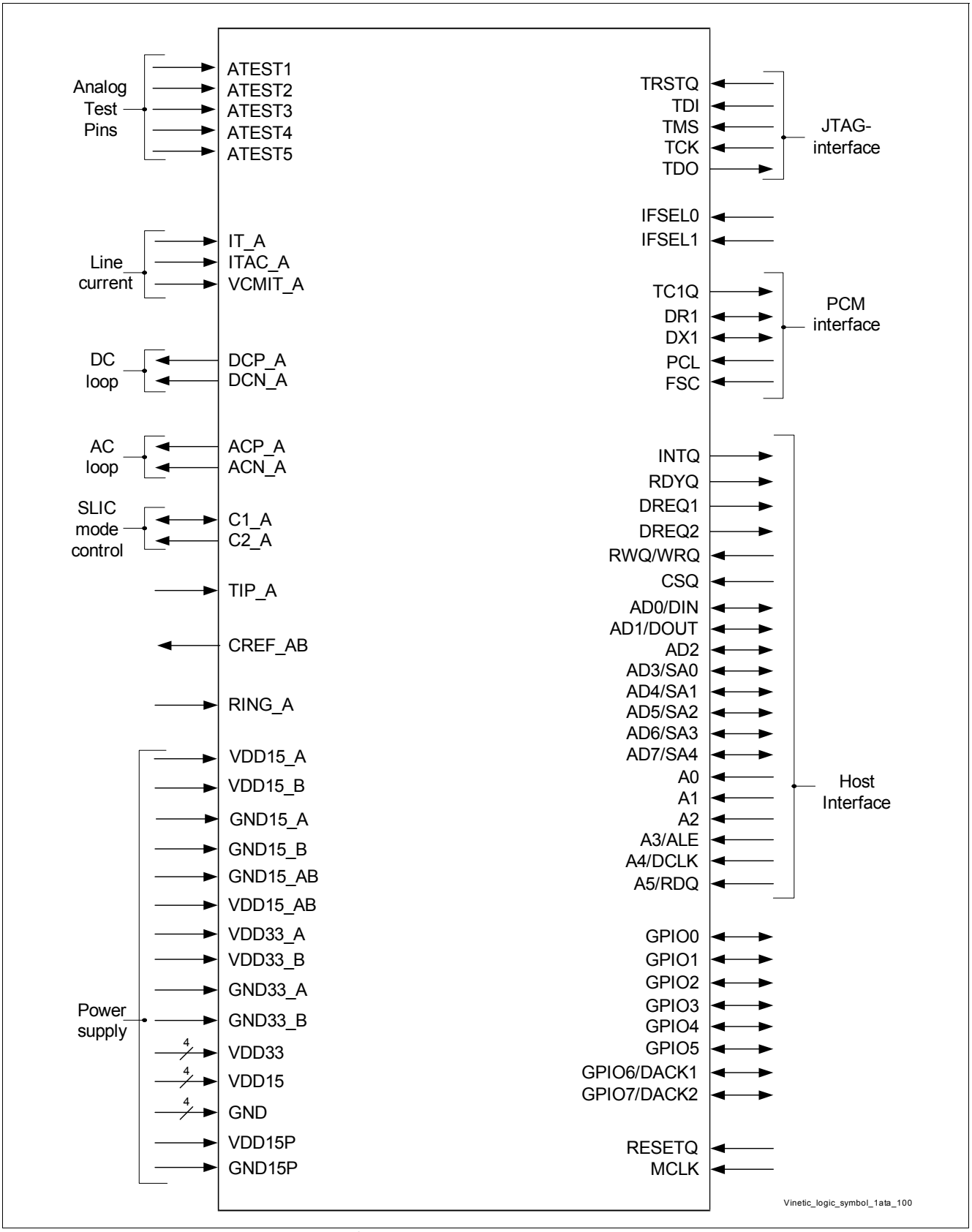

Figure 4 Logic Symbol for VINETIC®-1ATA (PG-TQFP-100)

1.3.3 Logic Symbols VINETIC®-CL and VINETIC®-0

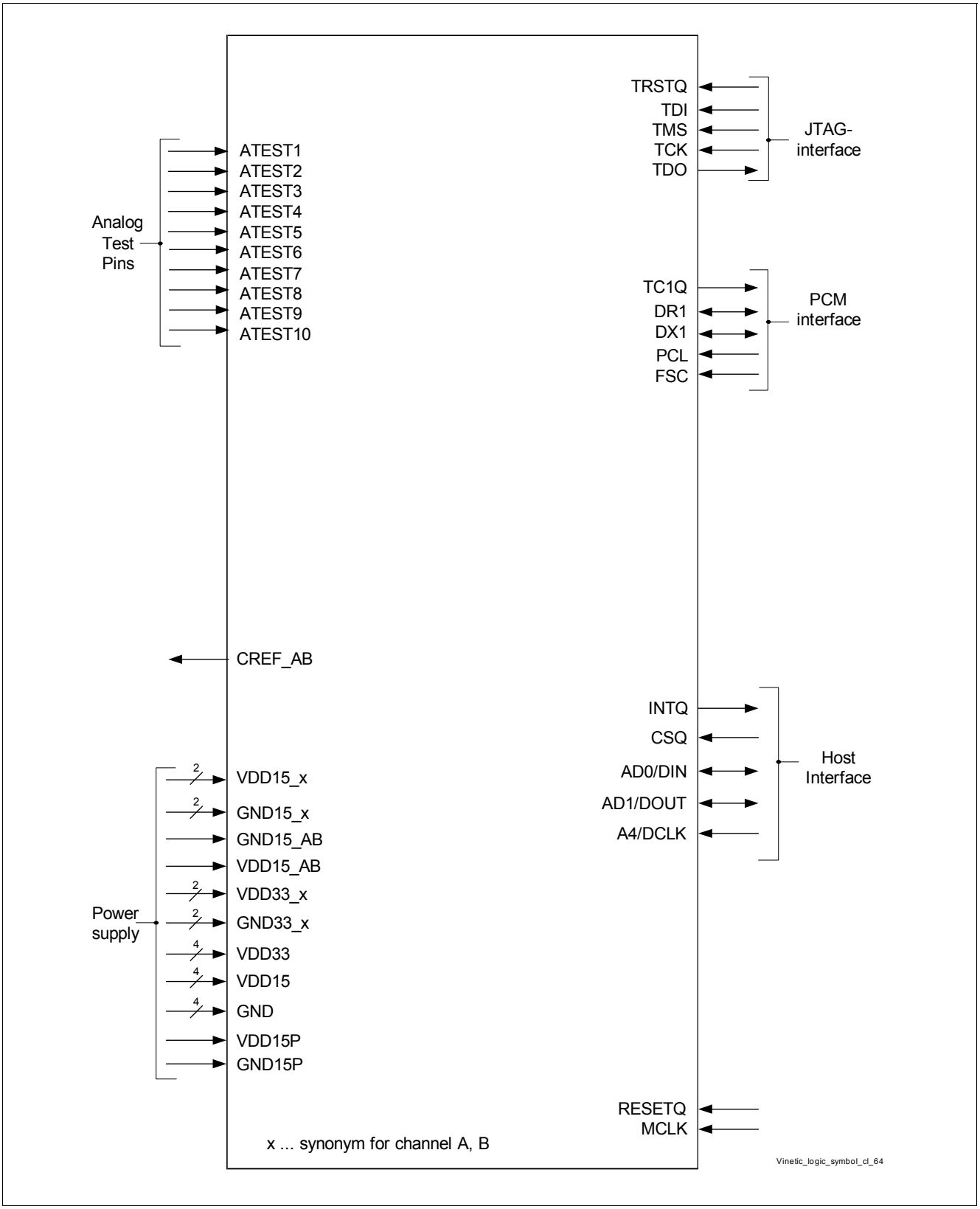

Figure 5 Logic Symbol for VINETIC®-CL and VINETIC®-0 (PG-TQFP-64)

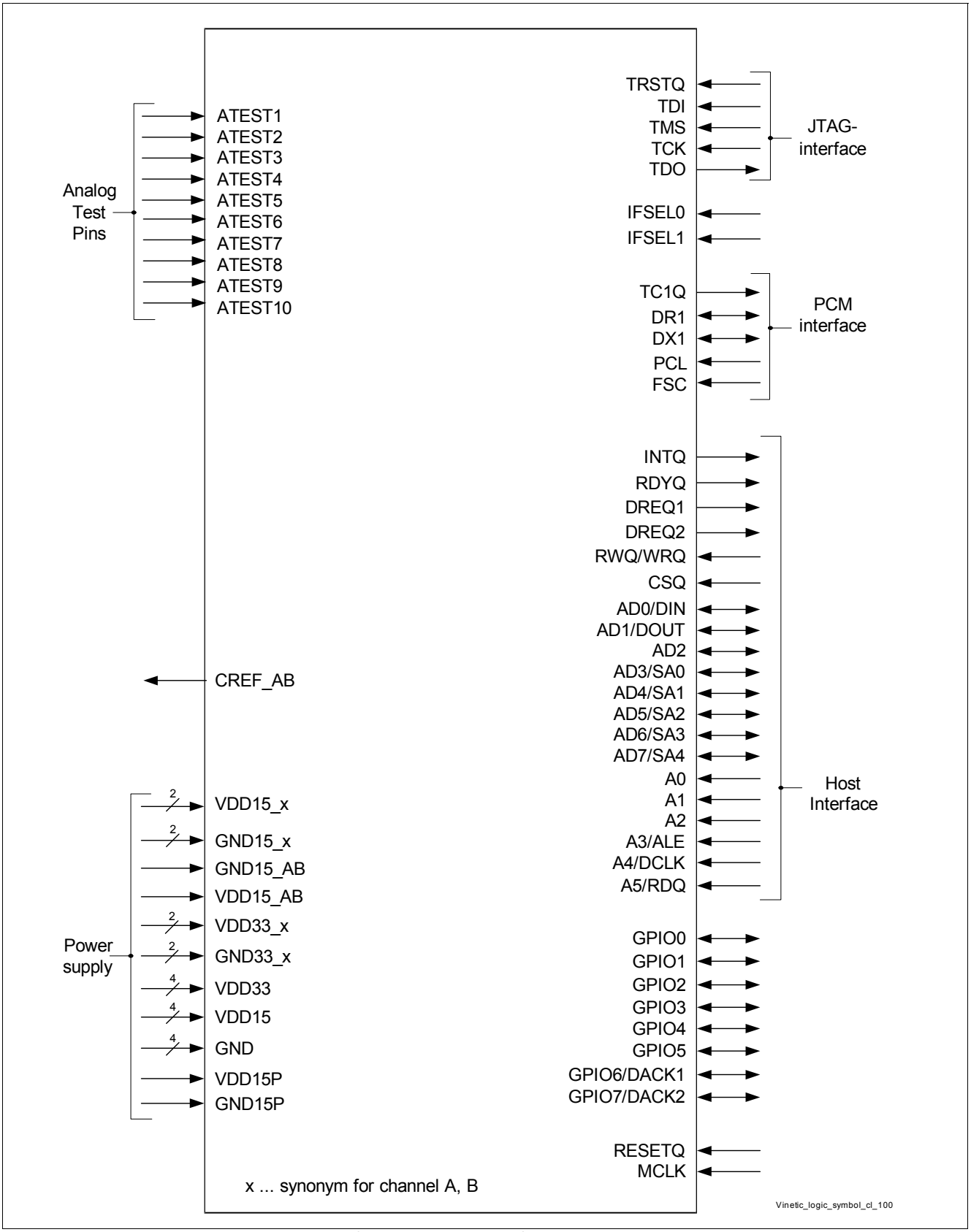

Figure 6 Logic Symbol for VINETIC®-CL and VINETIC®-0 (PG-TQFP-100)

2 Pin Description

2.1 Pin Diagrams

2.1.1 Pin Diagrams for VINETIC®-2ATA

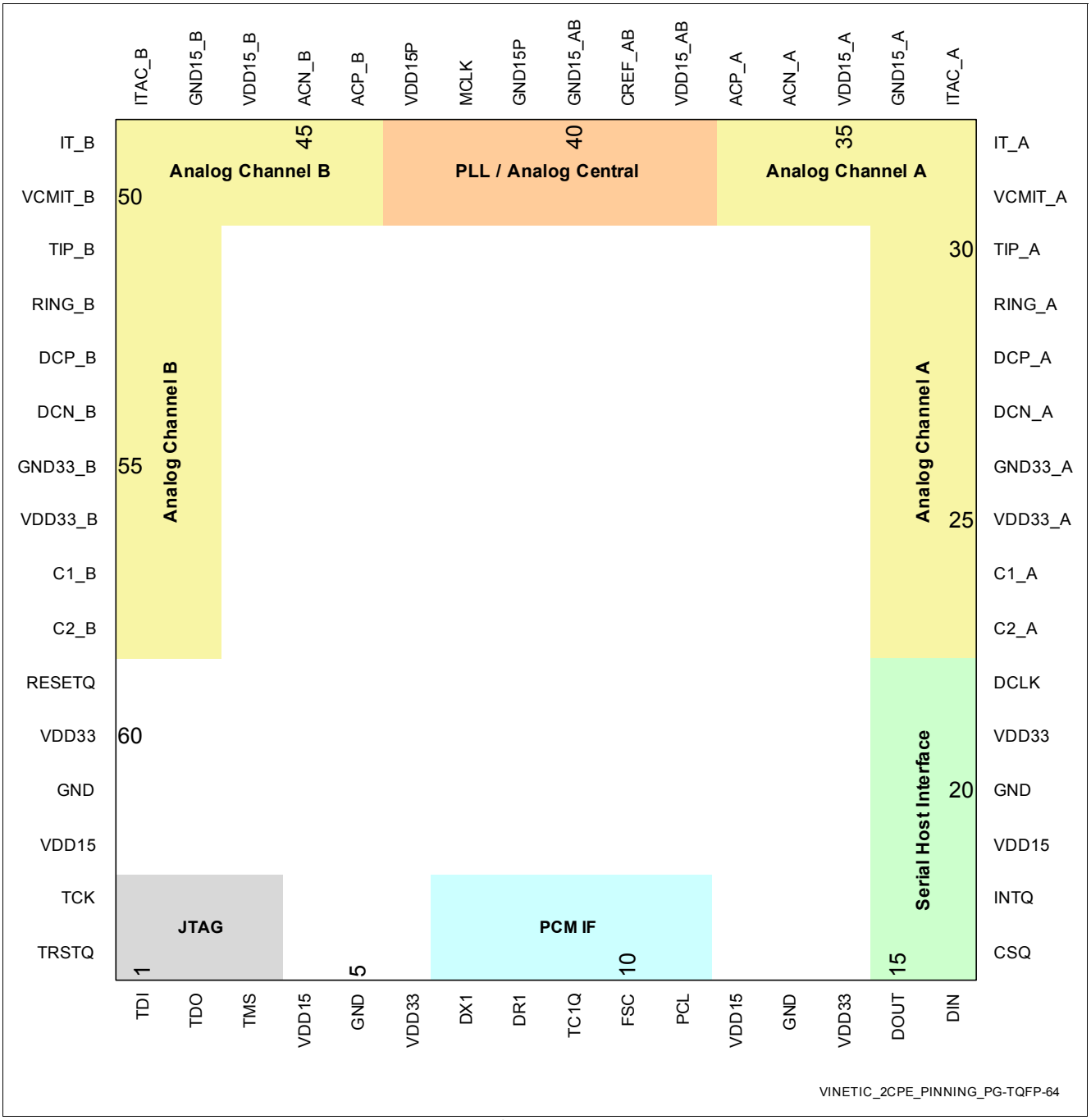

Figure 7 Pin Diagram (Top View) for VINETIC®-2ATA (PG-TQFP-64)

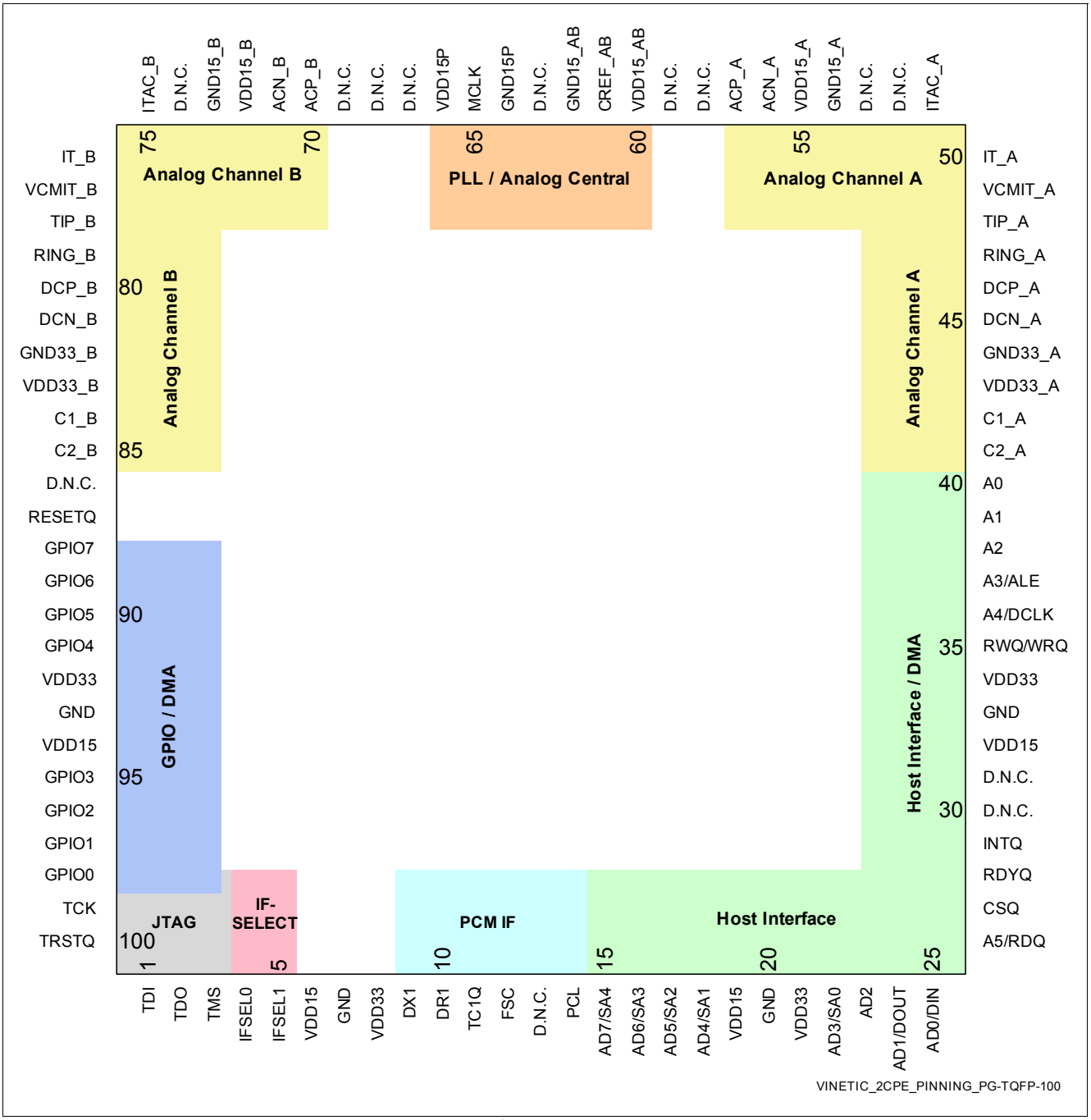

Figure 8 Pin Diagram (Top View) for VINETIC®-2ATA (PG-TQFP-100)

2.2 Pin Diagrams for VINETIC®-1ATA

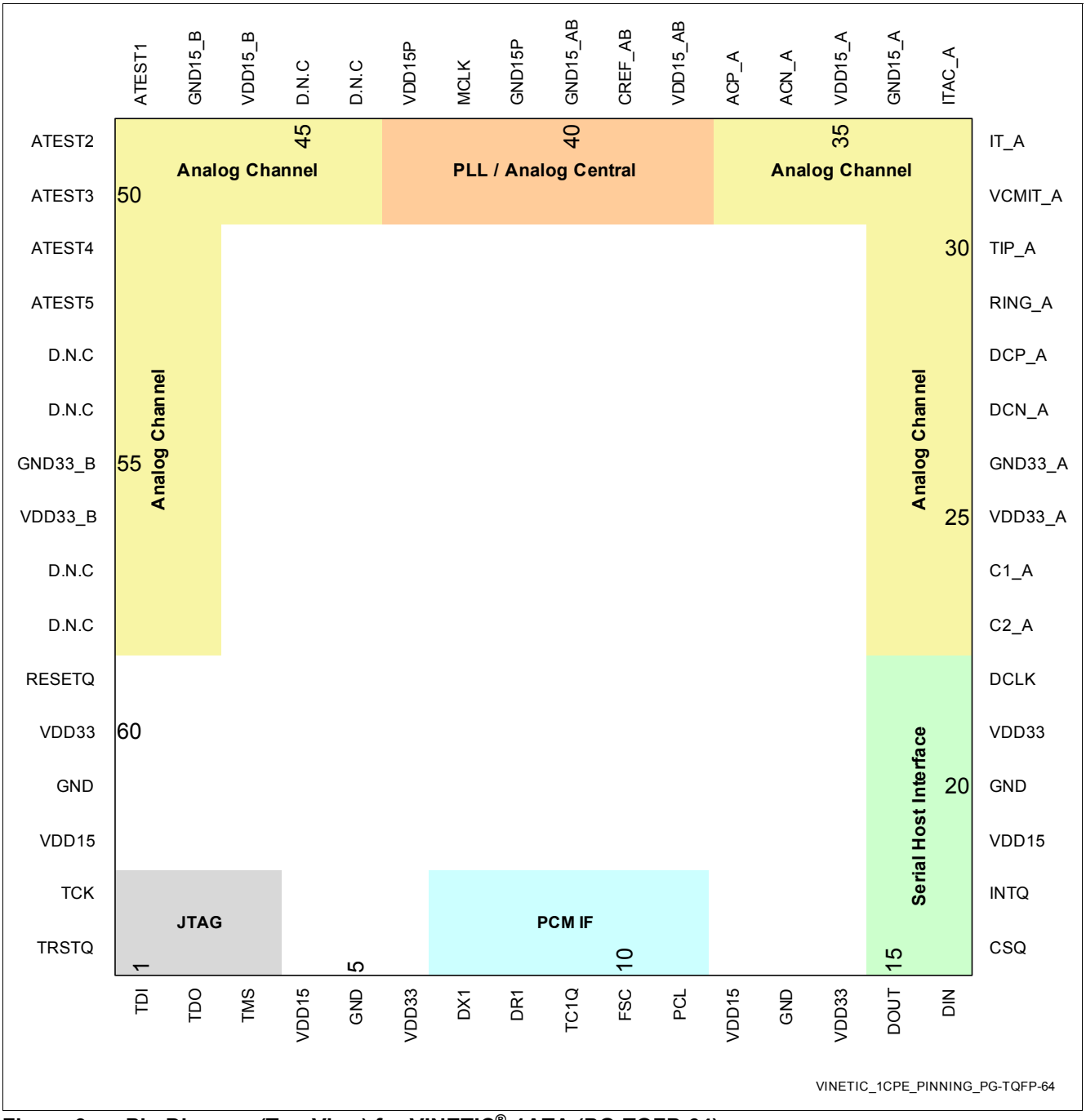

Figure 9 Pin Diagram (Top View) for VINETIC®-1ATA (PG-TQFP-64)

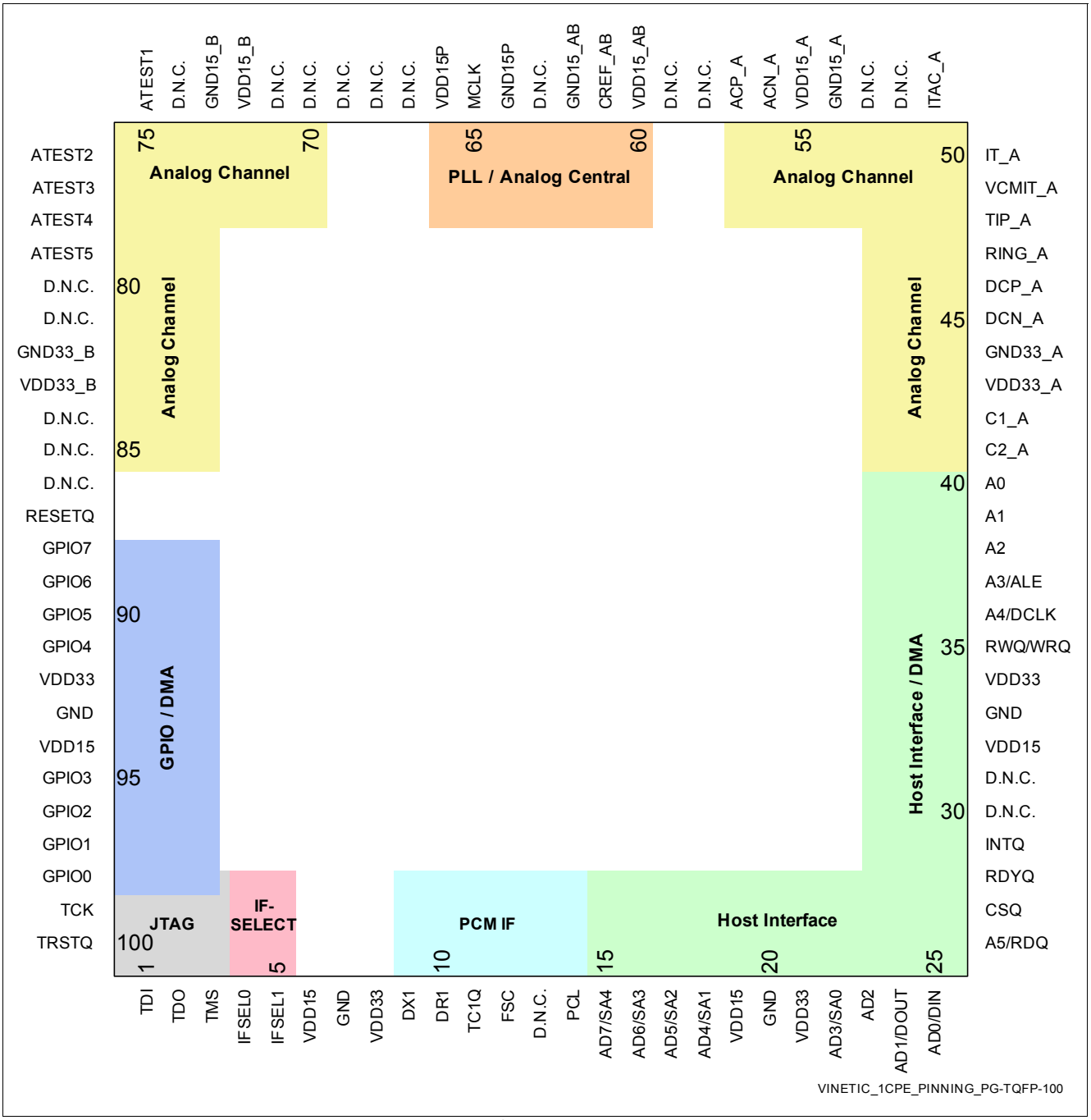

Figure 10 Pin Diagram (Top View) for VINETIC®-1ATA (PG-TQFP-100)

2.3 Pin Diagrams for VINETIC®-CL and VINETIC®-0

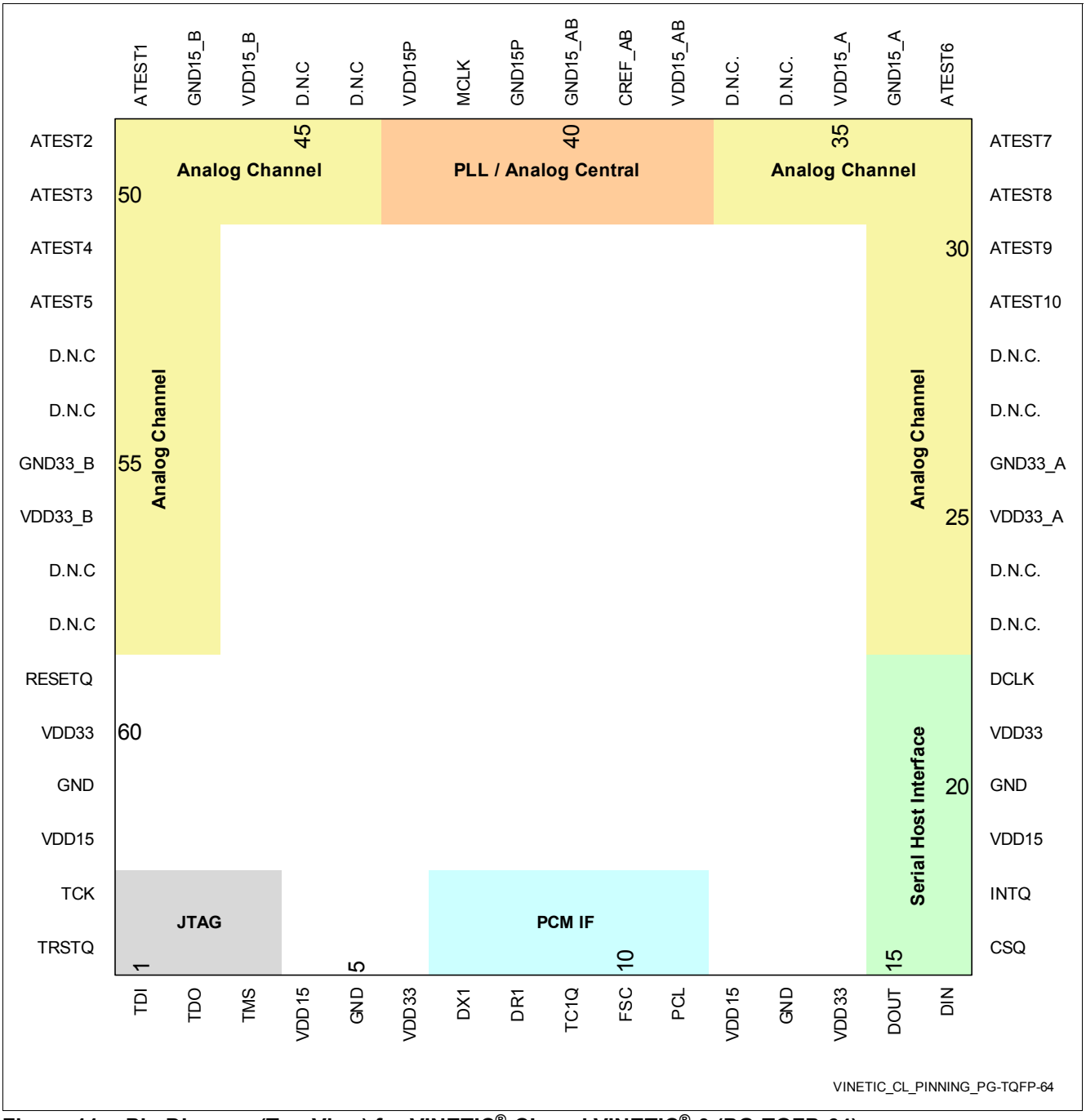

Figure 11 Pin Diagram (Top View) for VINETIC®-CL and VINETIC®-0 (PG-TQFP-64)

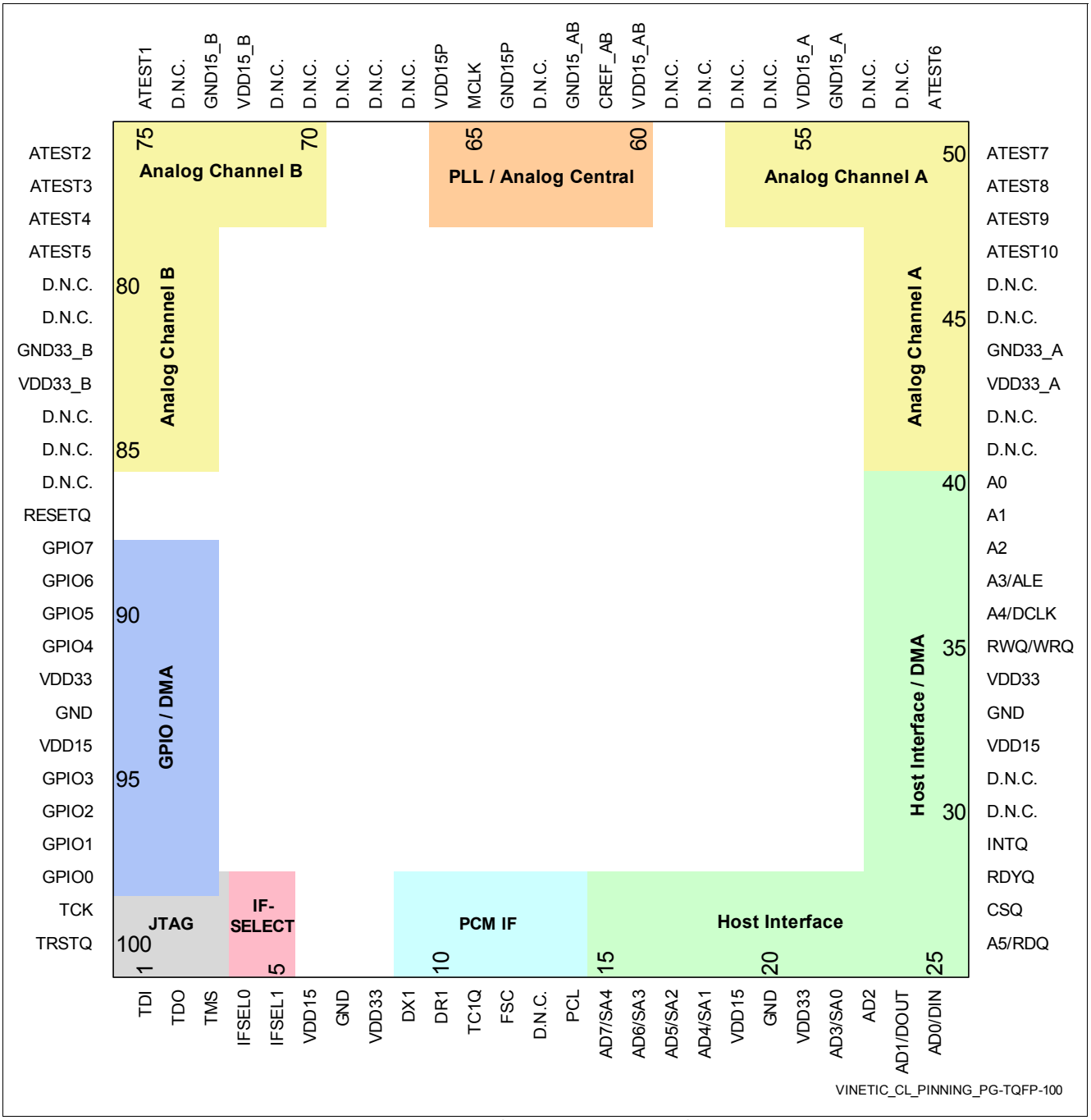

Figure 12 Pin Diagram (Top View) for VINETIC®-CL and VINETIC®-0 (PG-TQFP-100)

2.4 VINETIC®-2ATA/-1ATA/-CL/-0 Pins Sorted by Function

Table 6 Abbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or output. Analog levels.
PWR	Power
GND	Ground
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 7 Abbreviations for Buffer Type

Abbreviations	Description
PU	Pull-up
OD	Open-Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).

2.4.1 Common Pins for Analog Line Module (Channels A, B)

Table 8 Common Pins for Analog Line Module (Channels A, B)

Pin No.		Pin Name	Pin Type[1]	Buffer Type[2]	Function	-2ATA	-1ATA	-CL/-0
64-pin Packages	100-pin Packages							
39	61	CREF_AB	AI/O	-	Connection to external capacitor for low-pass filtering of the reference voltage	y	y	y
40	62	GND15_AB	GND	-	Common ground for bias block	y	y	y
38	60	VDD15_AB	PWR	-	1.5 V power supply for bias	y	y	y

1) For explanation of abbreviations see Table 6

2) For explanation of abbreviations see Table 7

2.4.2 Pins for Analog Line Module (Channels A, B)

Table 9 Pins for Analog Line Module (Channels A, B)

Pin No.		Pin Name	Pin Type[1]	Buffer Type[2]	Function	-2ATA	-1ATA	-CL/-0
64-pin Packages	100-pin Packages							
29 52	47 79	RING_A RING_B	AI	-	Analog input for measurement the voltage on ring line	y y	y -	- -
30 51	48 78	TIP_A TIP_B	AI	-	Analog input for measurement the voltage on tip line	y y	y -	- -
37 44	57 70	ACP_A ACP_B	AO	-	Differential two-wire AC output voltage controlling the RING/TIP pins at the SLIC	y y	y -	- -
36 45	56 71	ACN_A ACN_B	AO	-	Differential two-wire AC output voltage controlling the RING/TIP pins at the SLIC	y y	y -	- -
28 53	46 80	DCP_A DCP_B	AO	-	Differential two-wire DC output voltage controlling the RING/TIP pins at the SLIC	y y	y -	- -
27 54	45 81	DCN_A DCN_B	AO	-	Differential two-wire DC output voltage controlling the RING/TIP pins at the SLIC	y y	y -	- -
25 56	43 83	VDD33_A VDD33_B	PWR	-	3.3 V analog power supply	y y	y y	y y
35 46	55 72	VDD15_A VDD15_B	PWR	-	1.5 V power supply	y y	y y	y y
26 55	44 82	GND33_A GND33_B	GND	-	Analog ground 3.3 V	y y	y y	y y
34 47	54 73	GND15_A GND15_B	GND	-	Analog ground 1.5 V	y y	y y	y y

Table 9 Pins for Analog Line Module (Channels A, B) (cont'd)

Pin No. 64-pin Packages	Pin No. 100-pin Packages	Pin Name	Pin Type[1]	Buffer Type[2]	Function	-2ATA	-1ATA	-CL/-0
32 49	50 76	IT_A IT_B	AI	-	Transversal current input (AC + DC)	y y	y -	- -
33 48	51 75	ITAC_A ITAC_B	AI	-	Transversal current input (AC)	y y	y -	- -
31 50	49 77	VCMIT_A VCMIT_B	AI/O	-	Reference pin for transversal/longitudinal current sensing	y y	y -	- -
23 58	41 85	C2_A C2_B	AO	-	Ternary logic output controlling the SLIC operation mode	y y	y -	- -
24 57	42 84	C1_A C1_B	AI/O	-	Ternary logic output controlling the SLIC operation mode; indicating thermal overload of a SLIC if a current of typically 150 µA is drawn out by the SLIC's C1 pin	y y	y -	- -
48 49 50 51 52 33 32 31 30 29	75 76 77 78 79 51 50 49 48 47	ATEST1 ATEST2 ATEST3 ATEST4 ATEST5 ATEST6 ATEST7 ATEST8 ATEST9 ATEST10	NU	-	Analog test pins. These pins have to be connected together externally (shortcut).	- - - - - - - - - -	y y y y y - - - - -	y y y y y y y y y y

1) For explanation of abbreviations see **Table 6**
2) For explanation of abbreviations see **Table 7**

2.4.3 General Pins

Table 10 General Pins

Pin No.		Pin Name	Pin Type[1]	Buffer Type[2]	Function	-2ATA	-1ATA	-CL/-0
64-pin Packages	100-pin Packages							
59	87	RESETQ	I	-	Hardware reset for the whole chip (low active)	y	y	y
42	65	MCLK	I	-	Master clock for the PLL input. The MCLK clock can vary from 512 kHz to 8192 kHz in multiples of 512 kHz. This pin must be directly connected to PCL.	y	y	y
–	13, 30, 31, 52, 53, 58, 59, 63, 67, 68, 69, 74, 86	D.N.C.	NC	-	Do not connect	y	-	-
44, 45, 53, 54, 57, 58	13, 30, 31, 52, 53, 58, 59, 63, 67, 68, 69, 70, 71, 74, 80, 81, 84, 85, 86					-	y	-
23, 24, 27, 28, 36, 37, 44, 45, 53, 54, 57, 58	13, 30, 31, 41, 42, 45, 46, 52, 53, 56, 57, 58, 59, 63, 67, 68, 69, 70, 71, 74, 80, 81, 84, 85, 86					-	-	y

1) For explanation of abbreviations see **Table 6**
2) For explanation of abbreviations see **Table 7**

2.4.4 General-Purpose Input/Output Pins

Table 11 General-Purpose Input/Output Pins[1)]

Pin No.		Pin Name	Pin Type[2)]	Buffer Type[3)]	Function	-2ATA	-1ATA	-CL/-0
64-pin Packages	100-pin Packages							
–	98	GPIO0	I/O	OD, PP, PU[4)]	General-Purpose I/O 0	y	y	y
–	97	GPIO1	I/O	OD, PP, PU[4)]	General-Purpose I/O 1	y	y	y
–	96	GPIO2	I/O	OD, PP, PU[4)]	General-Purpose I/O 2	y	y	y
–	95	GPIO3	I/O	OD, PP, PU[4)]	General-Purpose I/O 3	y	y	y
–	91	GPIO4	I/O	OD, PP, PU[4)]	General-Purpose I/O 4	y	y	y
–	90	GPIO5	I/O	OD, PP, PU[4)]	General-Purpose I/O 5	y	y	y
–	89	GPIO6	I/O	OD, PP, PU[4)]	General-Purpose I/O 6	y	y	y
–	88	GPIO7	I/O	OD, PP, PU[4)]	General-Purpose I/O 7	y	y	y

1) If a GPIO pin is not used, it should be connected to ground via a 10 kΩ resistor. If guaranteed that it is never configured as an output, this pin can directly be connected to ground.
2) For explanation of abbreviations see **Table 6**
3) For explanation of abbreviations see **Table 7**
4) Buffer Type is programmable, after reset the pull-up is disabled and the pin is configured as an input

2.4.5 Test-Mode Selection/JTAG (Boundary Scan) Interface Pins

Table 12 Test-Mode Selection/JTAG (Boundary Scan) Interface Pins

Pin No.		Pin Name	Pin Type[1)]	Buffer Type[2)]	Function	-2ATA	-1ATA	-CL/-0
64-pin Packages	100-pin Packages							
1	1	TDI	I	-	JTAG data input[3)]	y	y	y
3	3	TMS	I	-	JTAG test-mode switch[4)]	y	y	y
63	99	TCK	I	-	JTAG clock[4)]	y	y	y
2	2	TDO	O	TS	JTAG data output[3)]	y	y	y
64	100	TRSTQ	I	-	JTAG reset[4)]	y	y	y

1) For explanation of abbreviations see **Table 6**
2) For explanation of abbreviations see **Table 7**
3) Pull-up resistor of 10 kΩ must be applied
4) Pull-down resistor of 10 kΩ must be applied

2.4.6 Interface-Type Selection Pins

Table 13 Interface-Type Selection Pins

Pin No.		Pin Name	Pin Type[1]	Buffer Type[2]	Function	-2ATA	-1ATA	-CL/-0
64-pin Packages	100-pin Packages							
–	4	IFSEL0	I	PU	Interface-select pin 0	y	y	y
–	5	IFSEL1	I	PU	Interface-select pin 1	y	y	y

1) For explanation of abbreviations see Table 6
2) For explanation of abbreviations see Table 7

2.4.7 PCM Interface Pins

Table 14 PCM Interface Pins

Pin No.		Pin Name	Pin Type[1]	Buffer Type[2]	Function	-2ATA	-1ATA	-CL/-0
64-pin Packages	100-pin Packages							
7	9	DX1	I/O	TS	PCM interface data output	y	y	y
8	10	DR1	I/O	TS	PCM interface data input	y	y	y
9	11	TC1Q	O	OD	Control pin for external driver	y	y	y
10	12	FSC	I	-	Frame synchronization for PCM interface and PLL input	y	y	y
11	14	PCL	I	-	Input for the PCM interface data clock PCLK. The PCL clock can vary from 512 kHz to 8192 kHz in multiples of 512 kHz. This pin must be directly connected to MCLK.	y	y	y

1) For explanation of abbreviations see Table 6
2) For explanation of abbreviations see Table 7

2.4.8 Host Interface Pins

Table 15 Host Interface Pins

Pin No.		Pin Name	Pin Type[1]	Buffer Type[2]	Signal Name				-2ATA	-1ATA	-CL/-0
64-pin Packages	100-pin Packages				Intel Multi-plexed Mode	Intel Demulti-plexed Mode	Motorola	SPI			
–	15	AD7/SA4	I/O	TS	A7/DIO7	DIO7	DATA7	SA4	y	y	y
–	16	AD6/SA3	I/O	TS	A6/DIO6	DIO6	DATA6	SA3	y	y	y
–	17	AD5/SA2	I/O	TS	A5/DIO5	DIO5	DATA5	SA2	y	y	y
–	18	AD4/SA1	I/O	TS	A4/DIO4	DIO4	DATA4	SA1	y	y	y
–	22	AD3/SA0	I/O	TS	A3/DIO3	DIO3	DATA3	SA0	y	y	y
–	23	AD2	I/O	TS	A2/DIO2	DIO2	DATA2	GND	y	y	y
15	24	AD1/DOUT	I/O	TS	A1/DIO1	DIO1	DATA1	DOUT[3]	y	y	y
16	25	AD0/DIN	I/O	TS	A0/DIO0	DIO0	DATA0	DIN[4]	y	y	y
–	26	A5/RDQ	I	-	RDQ	RDQ	ADDR5	GND	y	y	y
17	27	CSQ	I	-	CSQ	CSQ	CSQ	CSQ	y	y	y
–	28	RDYQ	O	OD	RDYQ	RDYQ	RDYQ	D.N.C.	y	y	y
18	29	INTQ	O	OD	INTQ	INTQ	INTQ	INTQ	y	y	y
–	35	RWQ/WRQ	I	-	WRQ	WRQ	RD/WRQ	GND	y	y	y
22	36	A4/DCLK	I	-	GND	A4	ADDR4	DCLK	y	y	y
–	37	A3/ALE	I	-	ALE	A3	ADDR3	GND	y	y	y
–	38	A2	I	-	GND	A2	ADDR2	GND	y	y	y
–	39	A1	I	-	GND	A1	ADDR1	GND	y	y	y
–	40	A0	I	-	GND	A0	ADDR0	GND	y	y	y

1) For explanation of abbreviations see **Table 6**
2) For explanation of abbreviations see **Table 7**
3) As the DOUT of the VINETIC® is set to high impedance for CSQ = high level, a pull-up resistor of 10 kΩ should be applied.
4) If the driver for the DIN signal may have high impedance, a pull-up resistor of 10 kΩ should be applied.

2.4.9 Digital Power/Ground Pins

Table 16 Digital Power/Ground Pins

Pin No.		Pin Name	Pin Type[1]	Buffer Type[2]	Function	-2ATA	-1ATA	-CL/-0
64-pin Packages	100-pin Packages							
4 12 19 62	6 19 32 94	VDD15	PWR	-	1.5 V power supply for the digital part	y y y y	y y y y	y y y y
43	66	VDD15P	PWR	-	1.5 V power supply for the PLL. The PLL is most important for the overall performance of the chip. Special care should be taken with respect to the filtering of the PLL power supply.	y	y	y
6 14 21 60	8 21 34 92	VDD33	PWR	-	Digital 3.3 V power supply for I/O pads	y y y y	y y y y	y y y y
5 13 20 61	7 20 33 93	GND	GND	-	Digital ground	y y y y	y y y y	y y y y
41	64	GND15P	GND	-	PLL ground Connect the PLL ground to a high quality ground.	y	y	y

1) For explanation of abbreviations see **Table 6**
2) For explanation of abbreviations see **Table 7**

3 Hardware Behavior and Handling

3.1 Block Diagram VINETIC®-2ATA/-1ATA

Figure 13 is the block diagram of the VINETIC®-2ATA/-1ATA.

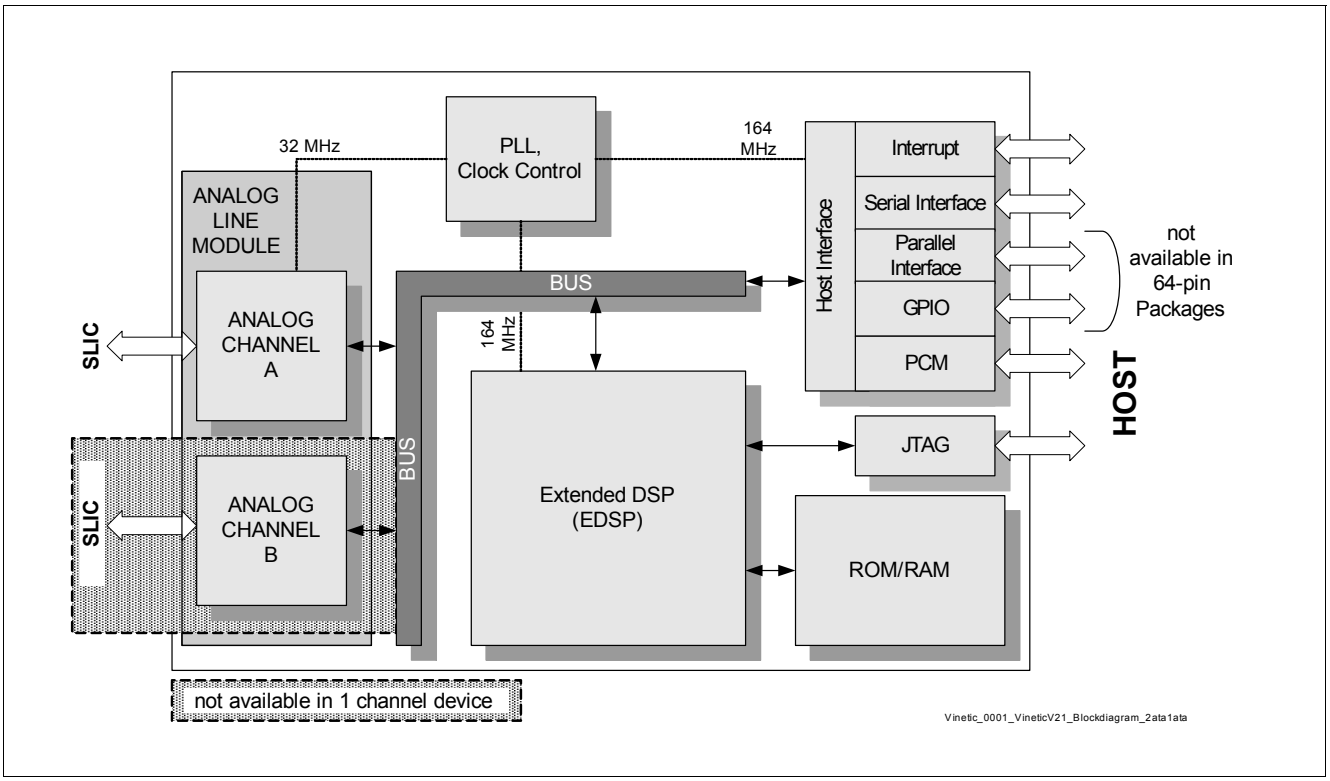

Figure 13 Block Diagram VINETIC®-2ATA/-1ATA

3.2 Block Diagram VINETIC®-CL and VINETIC®-0

Figure 13 is the block diagram of the VINETIC®-CL and the VINETIC®-0.

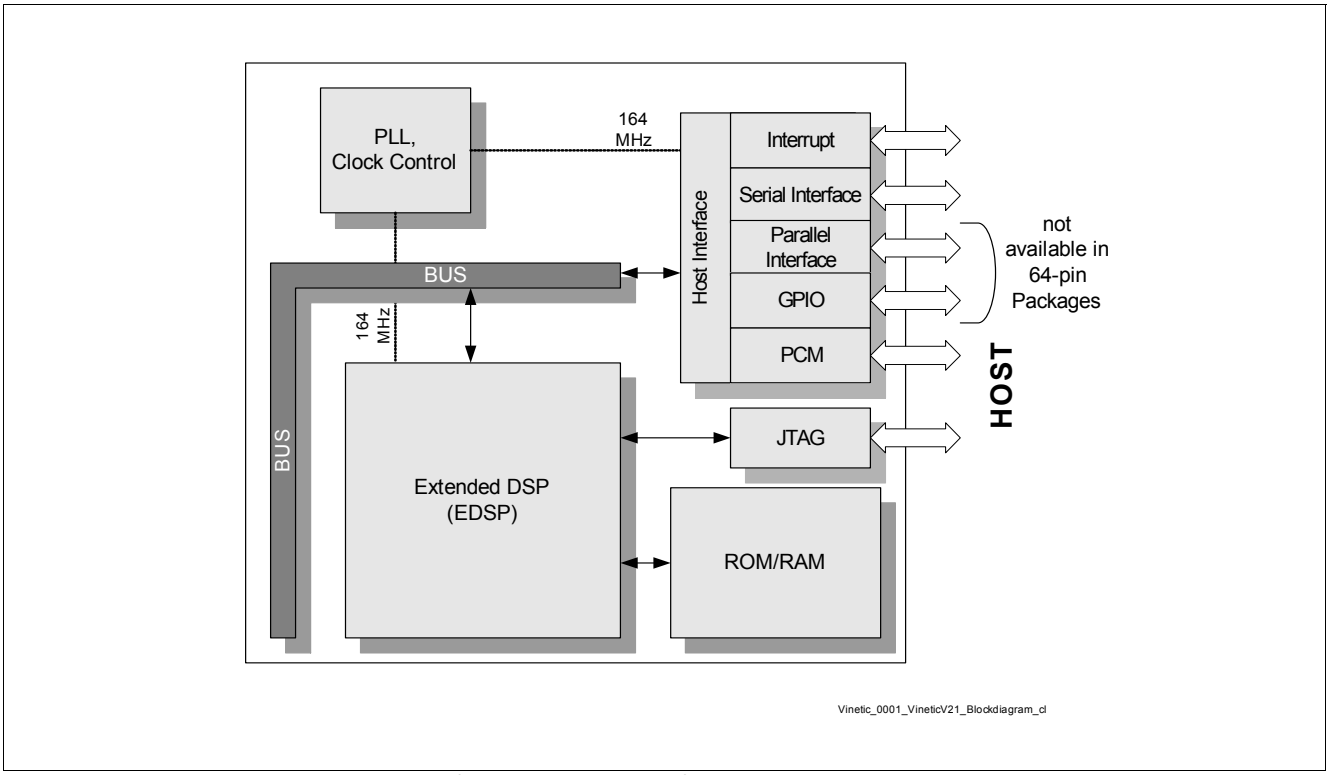

Figure 14 Block Diagram VINETIC®-CL and VINETIC®-0

3.3 Clocking

For a detailed description please refer to **[1]**.

3.4 Reset

For a detailed description please refer to **[1]**.

3.5 Test Modes

For a detailed description please refer to **[1]**.

4 Interface Description

For a detailed description please refer to [1].

4.1 Intel/Motorola-Mode Parallel Interfaces

For a detailed description please refer to [1].

4.2 SCI/SPI Interface

For a detailed description please refer to [1].

4.3 PCM Interface

For a detailed description please refer to [1].

4.4 Test Interface (JTAG Interface)

For a detailed description please refer to [1].

4.5 SLIC Interface (only valid for VINETIC®-2ATA/-1ATA)

The SLIC-DC (PEF 4268) Version 1.2 is controlled by ternary logic signals via the C1_x[1)] and C2_x[1)] pins.

For application circuits, please refer to [2].

Attention: Not valid for VINETIC®-CL and VINETIC®-0.

1) x stands for A, B or just for A - the 2 or 1 analog channels of the VINETIC®-2ATA/-1ATA

5 Electrical Characteristics

VINETIC®-2ATA/-1ATA:

The specifications in [1] may be used without any limitations.

VINETIC®-CL and VINETIC®-0:

The specifications in [1] may be used, but the following parameters are NOT VALID or must be added:

5.1 Absolute Maximum Ratings VINETIC®-CL/VINETIC®-0

Table 17 Absolute Maximum Rating Parameters NOT VALID for VINETIC®-CL/VINETIC®-0

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog input and output pins	–					V_{DD33_x} = 3.3 V,
Pins	–					V_{DD15_i} = V_{DD15P} = 1.5 V,
DCP_x, DCN_x		–0.3	–	3.63	V	V_{GND15_i} = V_{GND15P} =
RING_x, TIP_x, IT_x, VCMIT_x, ITAC_x, ACP_x, ACN_x		–0.3	–	1.65	V	V_{GND33_x} = 0 V

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

5.2 Operating Range VINETIC®-CL/VINETIC®-0

V_{GND} = V_{GND15_i} = V_{GND15P} = V_{GND33_x} = 0 V

Table 18 Operating Range Parameters NOT VALID for VINETIC®-CL/VINETIC®-0

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog input pins RING_x, TIP_x, IT_x referred to the corresp. pin VCMIT_x	–	–0.5	–	0.5	V	V_{DD15_i} = 1.5 V
Analog input pin ITAC_x referred to the corresp. pin VCMIT_x	–	–0.11	–	0.11	V	V_{DD15_i} = 1.5 V
Analog output pins:	–					V_{DD33_x} = 3.3 V,
						V_{DD15_i} = 1.5 V
DCP_x, DCN_x		0.25	–	2.75	V	R_{Load} > 100 kΩ
ACP_x, ACN_x		0.2	–	1.2	V	R_{Load} > 20 kΩ
C1_x, C2_x		0	–	3.3	V	I_{Load} < 220 µA
referred to the corresp. ground pins GND15_x, GND33_x						
Analog pin VCMIT_x referred to the corresp. ground pin GND15_x	–	–	0.7	–	V	V_{DD15_AB} = 1.5 V

Table 18 Operating Range Parameters NOT VALID for VINETIC®-CL/VINETIC®-0 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog input pins (RING_x, TIP_x)						
Input impedance (RING_x, TIP_x): single input measurement (RING_x, TIP_x to GND15_x)	$R_{RTinS,G}$ 1)	600	750	900	kΩ	–
Input impedance (RING_x, TIP_x): differential measurement (RING_x to TIP_x)	R_{RTinD} 1)	1200	1500	1800	kΩ	–
Input impedance (RING_x, TIP_x): differential measurement (RING_x,TIP_x to VCMIT_x)	$R_{RTinD,V}$ 1)	800	1000	1200	kΩ	–

1) Not subject for production test - verified by design/characterization

5.2.1 Power Consumption VINETIC®-CL/VINETIC®-0

The power values in the corresponding chapter in [1] are NOT VALID for the VINETIC®-CL/VINETIC®-0 and must be replaced by the following parameters:

T_A = 0 °C to 85 °C, unless otherwise stated.
$V_{DD15} = V_{DD15\_i} = V_{DD15P}$ = 1.5 V ± 5 %
$V_{DD33} = V_{DD33\_x}$ = 3.3 V ± 5 %
$V_{GND} = V_{GND15\_i} = V_{GND15P} = V_{GND33\_x}$ = 0 V

Table 19 Power Consumption Parameters for VINETIC®-CL/VINETIC®-0

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power consumption in operation modes 1)						
System base load	$P_{DD15,ACT}$ $P_{DD33,ACT}$	– –	125 2) 25 3)	150 2) 30 3)	mW mW	Basic EDSP Load
EDSP module 4)						
Active	$P_{DD15,EDSP}$	–	1.5	1.7	mW/Mcycles	EDSP power consumption, max. EDSP load: 163.8 Mcycles/s

1) To calculate total power consumption, the values for both supply voltages (3.3 V and 1.5 V) have to be summed up.
2) Depends on the EDSP load used.
3) Depends on the load of the external circuitry at the I/O pins.
4) For estimation of power consumption with different EDSP loads.

6 Package Outlines

For a detailed description please refer to [1].

Literature References

[1] VINETIC®-2CPE/-1CPE (PEB/PEF 3332/-3331) Version 2.2 Prel. Data Sheet Rev. 1.0, 2006-07-07

[2] VINETIC®-CPE Prel. User's Manual System Description Rev. 2.0, in preparation

Attention: Please refer to the latest revision of the documents.

Standards References

[3] ETSI Standard ES 202 971 V1.2.1, (2006-01), Access and Terminals (AT); Public Switched Telephone Network (PSTN); Harmonized specification of physical and electrical characteristics of a 2-wire analogue interface for short line interface

[4] ITU-T Recommendation Q.552, (11/2001), Transmission characteristics at 2-wire analogue interfaces of digital exchanges

[5] Telcordia Technologies GR-909-CORE Issue 2 December 2004, Generic Criteria for Fiber in the Loop Systems

Terminology

A	
A/D	Analog to digital
AAL2	ATM Adaption Layer 2
AC	Alternative Current
ADC	Analog Digital Converter
AITDF	Advanced Integrated Test and Diagnostic Functions
ALM	Analog Line Module
ATD	Answering Tone Detector
ATM	Asynchronous Transfer Mode
C	
CAS	Channel Associated Signaling
CNG	Comfort Noise Generation
Codec	Coder Decoder
CPE	Customer Premises Equipment
CRAM	Coefficient RAM
D	
DAA	Data Access Arangement
DAC	Digital Analog Converter
DC	Direct Current
DSP	Digital Signal Processor
DTMF	Dual Tone Multi Frequency
E	
EXP	Expander
F	
FRR	Frequency Response Receive filter
FRX	Frequency Response Transmit filter
FSK	Frequency Shift Keying
FTTH	Fiber to the Home
FXO	Foreign eXchange Office
FXS	Foreign eXchange Subscriber
G	
GPIO	General Purpose Input/Output
H	
HW	Hardware
I	
IAD	Integrated Access Device
ITU	International Telecommunication Union
IP	Internet Protocol
ISDN	Integrated Services Digital Network
J	
JTAG	Joint Test Action Group

L	
LSSGR	Local area transport access Switching System Generic Requirements
N	
NG-DLC	Next Generation Digital Loop Carrier
NT	Network Terminal
P	
PBX	Private Branch eXchange
PCM	Pulse Code Modulation
POTS	Plain Old Telephone Service
R	
RAM	Random Access Memory
RBS	Robbed Bit Signaling
RTCP	Real-time Transport Control Protocol
RTP	Real-time Transport Protocol
S	
SLIC	Subscriber Line Interface Circuit (same for all versions)
SOHO	Small Office/Home Office
T	
TDM	Time Division Multiplexing
TG	Tone Generator
TH	Transhybrid Balancing
TS	Time Slot
TTX	Teletax (Metering)
U	
UTD	Universal Tone Detection
UTG	Universal Tone Generator
V	
VAD	Voice Activity Detection
VINETIC®	Voice and Internet Enhanced Telephony Interface Concept
VINETICOS	Voice and Internet Enhanced Telephony Interface Concept Coefficients Calculation Software
VoATM	Voice over ATM
VoDSL	Voice over DSL
VoIP	Voice over IP
W	
WLL	Wireless Local Loop
X	
xDSL	(all flavors of) Digital Subscriber Line

www.infineon.com

Published by Infineon Technologies AG