Rev. 2.0, 2005-05-18

VINETIC®

Voice and Internet Enhanced Telephony Interface Concept

PEB 3324, -3322, -3314, -3394, -3304, -4262, -4264/-2, -4364, 4265/-2, 4365, 4266

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Overview

This document is an Addendum to the VINETIC® Version 1.4 Prel. User´s Manual – System Reference DS1, 2003-10-15.

The following data have been changed or must be added:

1 Line Current Sensing Restriction in Reverse Polarity

Chapter 2.2.5, page 27: information on line current sensing restriction in reverse polarity added.

Table 3 DC Characteristics

Symbol	Programmable Range	Condition
R_I	1.8 kΩ … 40 kΩ	–
I_0	0 … 32 mA	Only for SLIC-S, SLIC-E, SLIC-P
	0 … 50 mA	Only for SLIC-S2 (see restrictions for reverse polarity as depicted below), SLIC-E2
I_{K1}	0 … 32 mA	Only for SLIC-S, SLIC-E, SLIC-P
	0 … 50 mA	Only for SLIC-S2 (see restrictions for reverse polarity as depicted below), SLIC-E2

Revision History: Previous Version: Rev. 1.0

Major Changes: **Chapter 7** added.

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Table 3 DC Characteristics (cont'd)

Symbol	Programmable Range	Condition
V_{K1}	0 … 50 V	$V_{K1} < V_{LIM} - I_{K1} \times R_{K12}$ when only one edge (V_{K1}, I_{K1}) is necessary
		$V_{K1} < V_{LIM} - I_{K1} \times R_V$ $V_{K1} > V_{LIM} - I_{K1} \times R_{K12}$ when both edges (V_{K1}, I_{K1}) and (V_{K2}, I_{K2}) are necessary
V_{LIM}	0 … 50 V	$V_{LIM} > V_{K1} + I_{K1} \times R_{K12}$ when only one edge (V_{K1}, I_{K1}) is necessary
		$V_{LIM} > V_{K1} + I_{K1} \times R_V$ $V_{LIM} < V_{K1} + I_{K1} \times R_{K12}$ when both edges (V_{K1}, I_{K1}) and (V_{K2}, I_{K2}) are necessary
R_{K12}	R_V … 2000 Ω	–

If the SLIC is operated with a power supply voltage of V_{DD} = 3.3 V, there is a restriction with line current sensing in reverse polarity as the current at the IT pin $I_{IT,\ rev\text{-}pol}$ of the SLIC flows in the direction as shown in **Figure 1**.

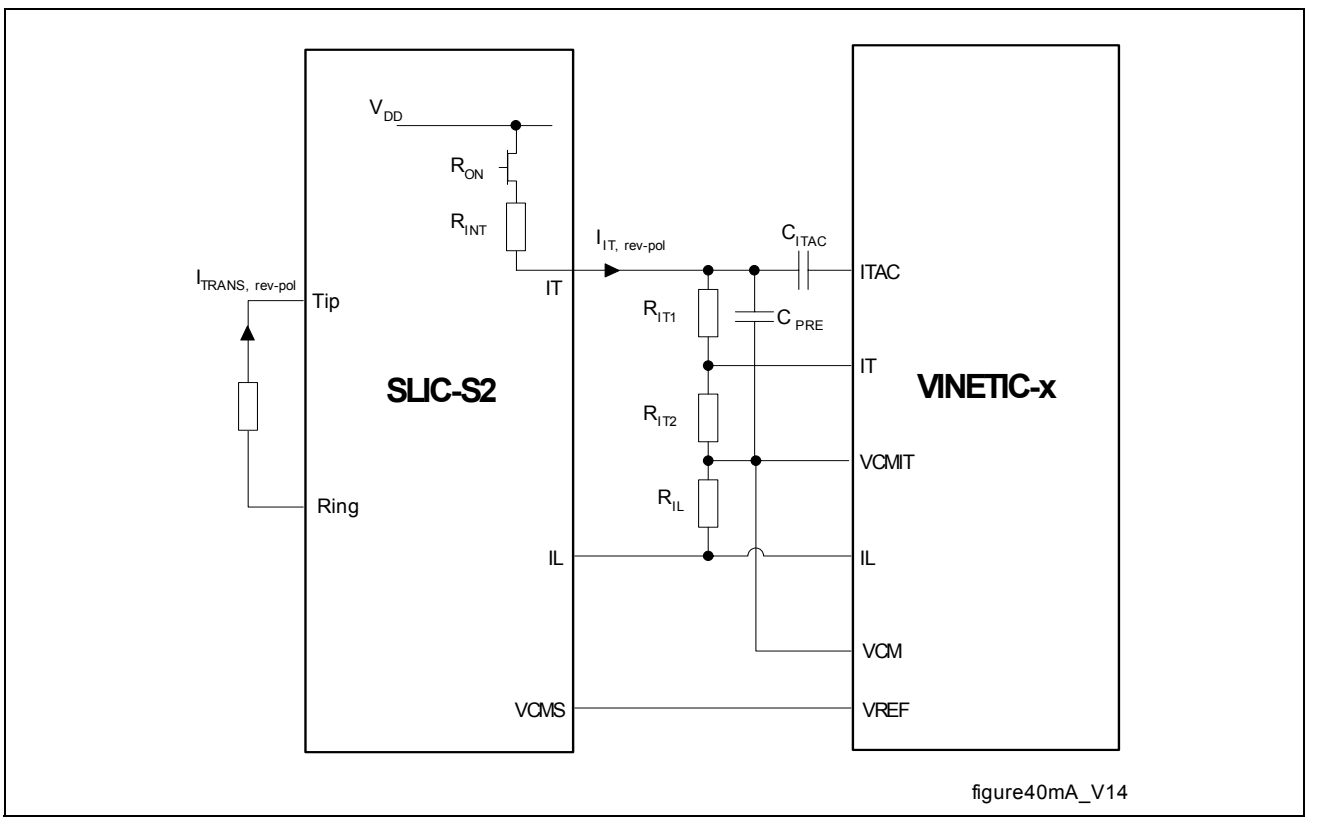

Figure 1 SLIC/CODEC Interface Circuitry

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This means that the voltage at the IT pin is going close to the V_{DD} supply. Because of internal resistors (R_{ON}, R_{INT}) the V_{DD} supply voltage can not be reached. Therefore the correct value of the transversal line current I_{IT} cannot be measured at the Codec which will lead to a false DC regulation behaviour.

The maximum transversal current I_{max_cur} which can be sensed is calculated as follows:

$$I_{max\_cur} = V_{wc\_delta\_v} / R_{total} \times K_{IT}.$$

with

$V_{delta\_v} = V_{DD} - V_{CM}$ = 3.3 V - 1.5 V = 1.8 V

$V_{wc\_delta\_v} = V_{delta\_v}$ - tolerance = 1.6 V (worst case delta voltage)

$R_{total} = R_{IT1} + R_{IT2} + R_{INT} + R_{ON}$ = 680 Ω + 510 Ω + 760 Ω + 200 Ω = 2150 Ω

K_{IT} = 50 (value of the current divider for transversal current)

I_{max_cur} = 37.2 mA

Please make sure that the maximum transversal current which can be sensed (I_{max_cur}) will not be exeeded within your system. The maximum current in the system is the sum of the highest DC current I_0 (see **Table 3**) and the peak value of the AC current (e.g. 2 mA). If teletax signals (TTX) are required during reverse polarity feeding it is also necessary to take the peak teletax current into account.

If the current calculated above does not fit to your system requirements, the following workarounds can be used:

Workaround 1

SLIC supply 5 V

→ $V_{wc\_delta\_v}$ = 3.2 V

→ I_{max_cur} = 74.4 mA

Workaround 2

R_{IT2} = 680 Ω

R_{IT1} = 0 Ω

→ I_{max_cur} = 48.8 mA

Disadvantage of Workaround 2:

- Capacitance of C_{PRE} must be increased from 18 nF to 33 nF.
- Lower gain in the analog impedance matching loop. This may influence the transmission performance in terms of return loss and the stability margin of the output impedance. Please check carefully with VINETICOS.

2 Extended Battery Feeding

Chapter 2.2.9, page 31: description improved, table added.

~~**Figure 17** shows the DC feeding impedances R_{MAX} in Active High mode and $R_{MAX,ActB}$ in Active Boost mode (for more information about the VINETIC® operating modes, see Chapter 3.1).~~

Table 4 shows all possible DC line feeding options:

Table 4 DC Line Feeding Options

DC Line Feeding	DC Line Feeding Impedance	SLIC Mode	*VINETIC®-x* Mode[1)]
Standard line feeding	R_{MAX}	ACTL ACTH	Active Low Active High
Extended battery feeding for long lines	$R_{MAX,ActB}$	ACTR	Active Boost

1) For more information about the *VINETIC®-x* operating modes see Chapter 3.1.

Figure 17 shows the DC line feeding impedances R_{MAX} (standard line feeding) and $R_{MAX,ActB}$ (extended battery feeding).

3 Ring Trip Thresholds used in Ringing Modes with VINETIC®

Chapter 2.4.2, page 36: table on Ring Trip thresholds added.

Table 5 gives an overview about the thresholds used with different Ring Trip methods for internal and external ringing with VINETIC®.

Table 5 Ring Trip Thresholds used in Ringing Modes

Selected Ring Trip Method	RTR: RTR-SEL	RTR: RTR-FAST	Used Threshold in Ringing Mode (Coefficient name)[1)]	Used Threshold in Ring Pause Mode (Coefficient name)[1)]
DC Ring Trip	0	0	DC Ring Trip Current Threshold	DC Ring Trip Current Threshold
AC Ring Trip	1	0	AC Ring Trip Threshold	DC Ring Trip Current Threshold
Fast Ring Trip	X	1	Fast AC Ring Trip Threshold	DC Ring Trip Current Threshold

1) Threshold programmed by the coefficient with VINETICOS. Refer to table 23 in chapter 7.3 in VINETIC® Version 1.4 Prel. User's Manual – Software Description Rev. 2.0, 2004-10-19.

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4 Internal Balanced Ringing

Chapter 2.4.6, page 42: description changes.

In ringing mode, the DC feeding ~~control~~ loop is not active.

5 Deep Sleep Mode

Chapter 3.2.1, page 59: description changes.

Deep Sleep Mode

After a wake up from deep sleep mode, the *VINETIC®-x* enters the Power Down High Impedance ~~PDRH or PDRR~~ mode.

6 Capacitance Measurements

Chapter 3.7.3.11, page 87: several program sequence text changes.

- Set the following parameter values:

Parameter	Symbol & Value	VINETICOS
Voltage slope of ramp generator	dU/dt = 200 V/s	DC specification description page for ringing
Ring frequency	f_{RING} = 100 Hz	DC specification description page for ringing
Ring generator delay	$T_{RING,DELAY}$ = 345 ms	DC specification description page for ringing
Ring offset voltage 1	RO1 = 70 V	DC specification description page for ringing
Ring offset voltage 2	RO2 = –30 V	DC specification description page for ringing
Ring offset voltage 3	arbitrary[1)]	DC specification description page for ringing
DC level meter current 50% full scale	$I_{LM,DC}$ = 2 mA	DC specification description page for levelmetering

1) not relevant for this calculation

- Integration time $T_I = 1/f_{RING}$ = 1/100 Hz = 10 ms.
- Set coefficient Ring Delay.

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- Select the DC level meter for DC Current on IT by setting bits LM-SEL[3:0] in register LMCR to 0101.
- Execute the level meter only once by setting bit LM-ONCE in register LMCR to 1.
- Enable the ramp generator by setting bit RAMP-EN in register LMCR to 1.
- ~~Apply~~Select Ring Offset voltage RO1 to Ring and Tip line by setting bits RNG-OFFSET[1:0] in register LMCR to 01 (the ramp generator will softramp to RO1).
- Wait for RAMP-READY.
- ~~Apply~~Select Ring Offset voltage RO2 to Ring and Tip line by setting bits RNG-OFFSET[1:0] in register LMCR to 10.
- Enable the ramp generator by setting bit LM-EN in register LMCR to 1.
  - Comment: The voltage ramp starts at RO1 and ramps up/down until RO2 is achieved. After the integration time, the result will be stored within the LMRES register.
- Read the result register LMRES.
- Set LM-EN in register LMCR to 0.
- When RO2 is reached the RAMP-READY interrupt (if not masked) will be generated. To start another ramp you simply select the new target voltage (for example RO1) and set LM-EN to 1.
- Set RAMP-EN to 0.

The actual current $I_{CMeasure}$ amounts to:

$$I_{CMeasure} = 2 \times I_{LM,\,DC} \times LM_{Result} \quad (1)$$

The capacitance $C_{Measure}$ calculates as:

$$C_{Measure} = \frac{I_{CMeasure}}{\frac{dU}{dt}} \quad (2)$$

Example:

$LM_{Value} = 3AF2_H = 15090$

$LM_{Result} = LM_{Value}/LM_{Fullscale} = 15090/32768 = 0.4605$

$I_{CMeasure} = 2 \times 2\ mA \times 0.4605 = 1.842\ mA$

$C_{Measure} = 1.842\ mA/200\ V/s = 9.21\ \mu F$

SOP Command Timing Requirements

To ensure the correct function of AITDF test sequences, consecutive and interdependent SOP commands[1)] for the ALM modules must be sent with time gaps of ≥ 2 ms.

1) SOP commands that depend on the setting of registers of an earlier SOP command

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7 Additional Components

7.1 Application Circuits

The following application circuits and bill of materials have been changed:

7.1.1 Application Circuits for Internal Ringing

Chapter 5.1.1, page 114: C_N, R_{DCLP} and C_{DCLP} added.

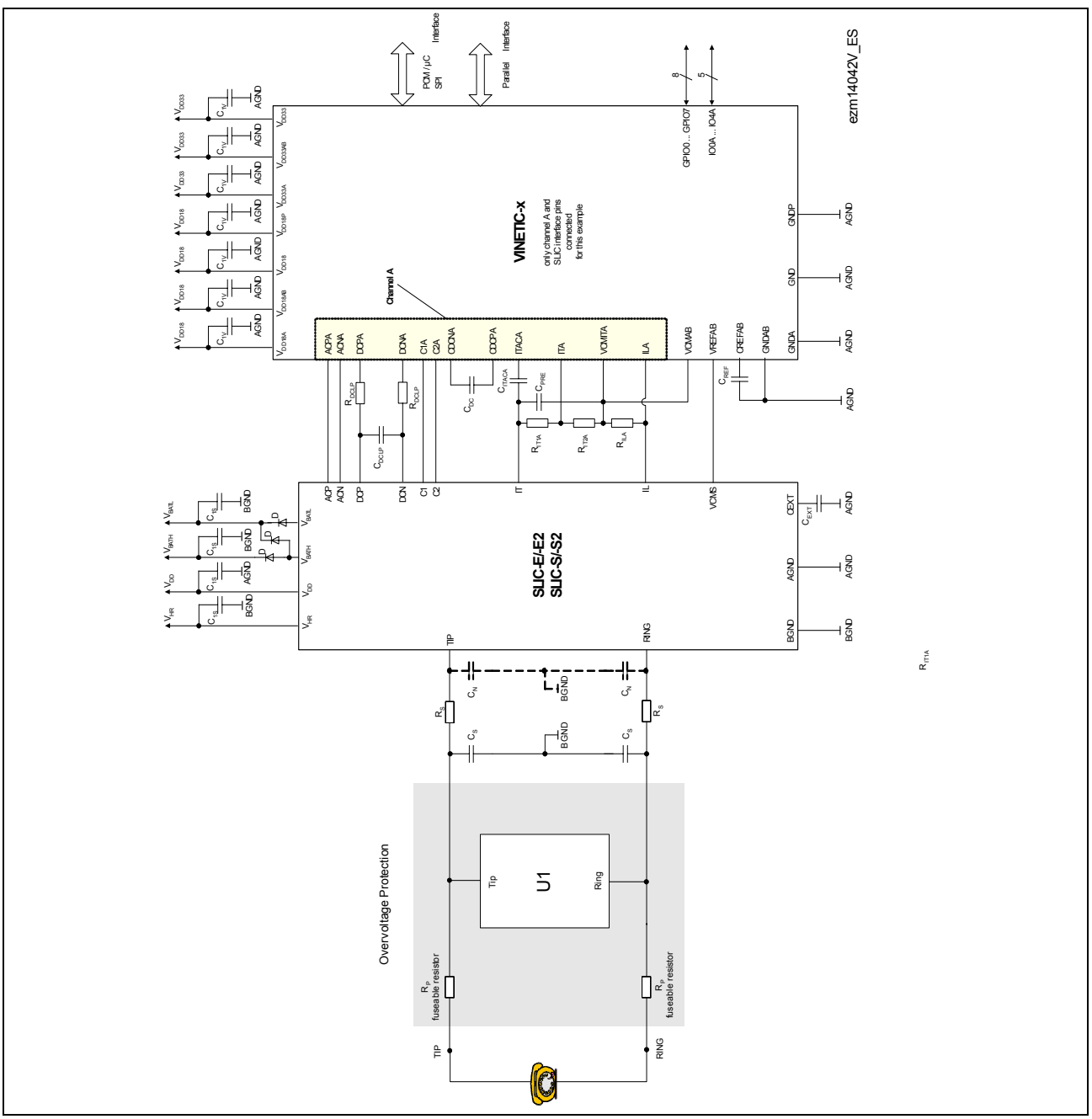

Figure 2 Application Circuit Internal Ringing (balanced) for SLIC-E/-S

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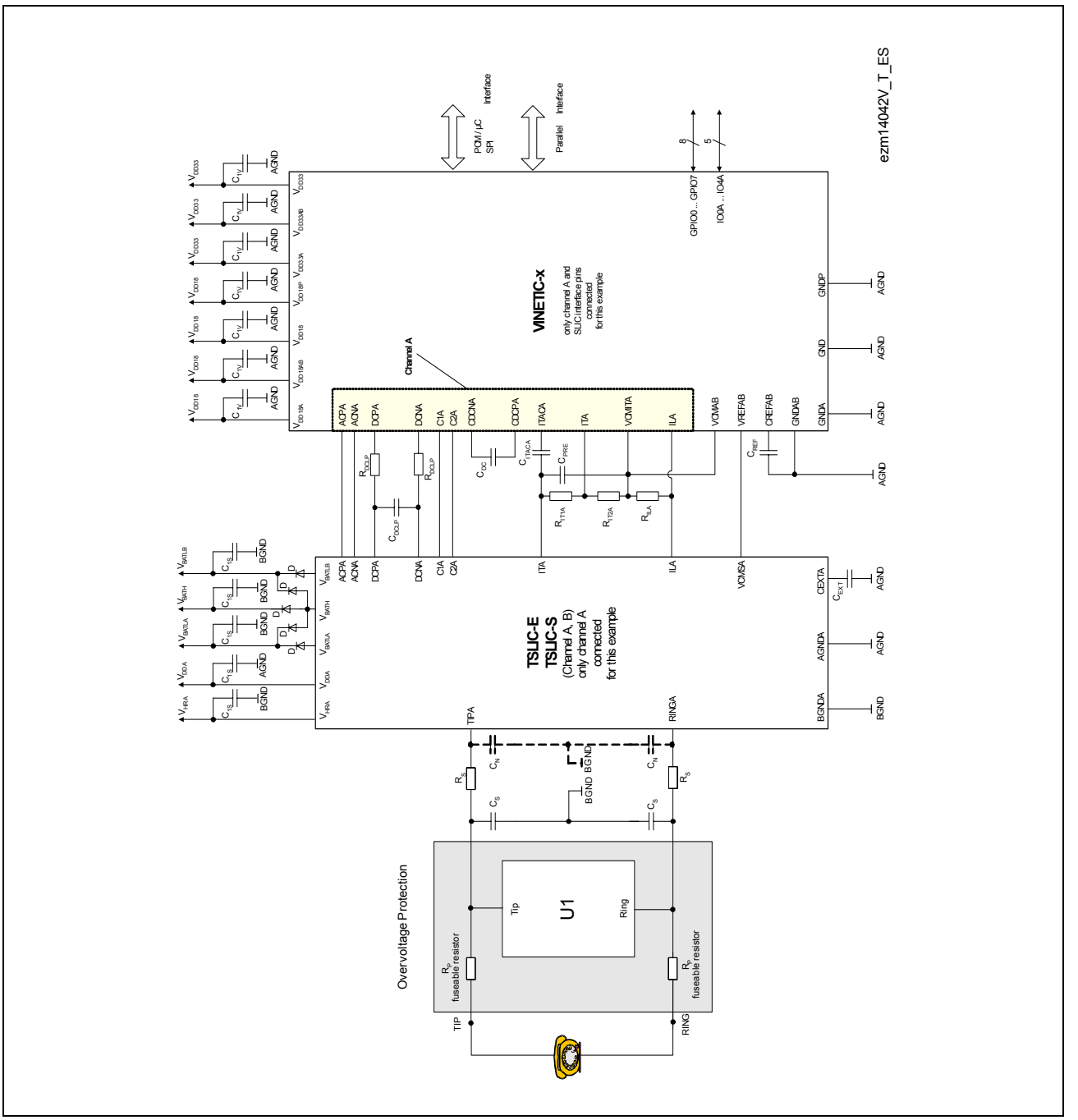

Figure 3 Application Circuit Internal Ringing (balanced) for TSLIC-E/-S

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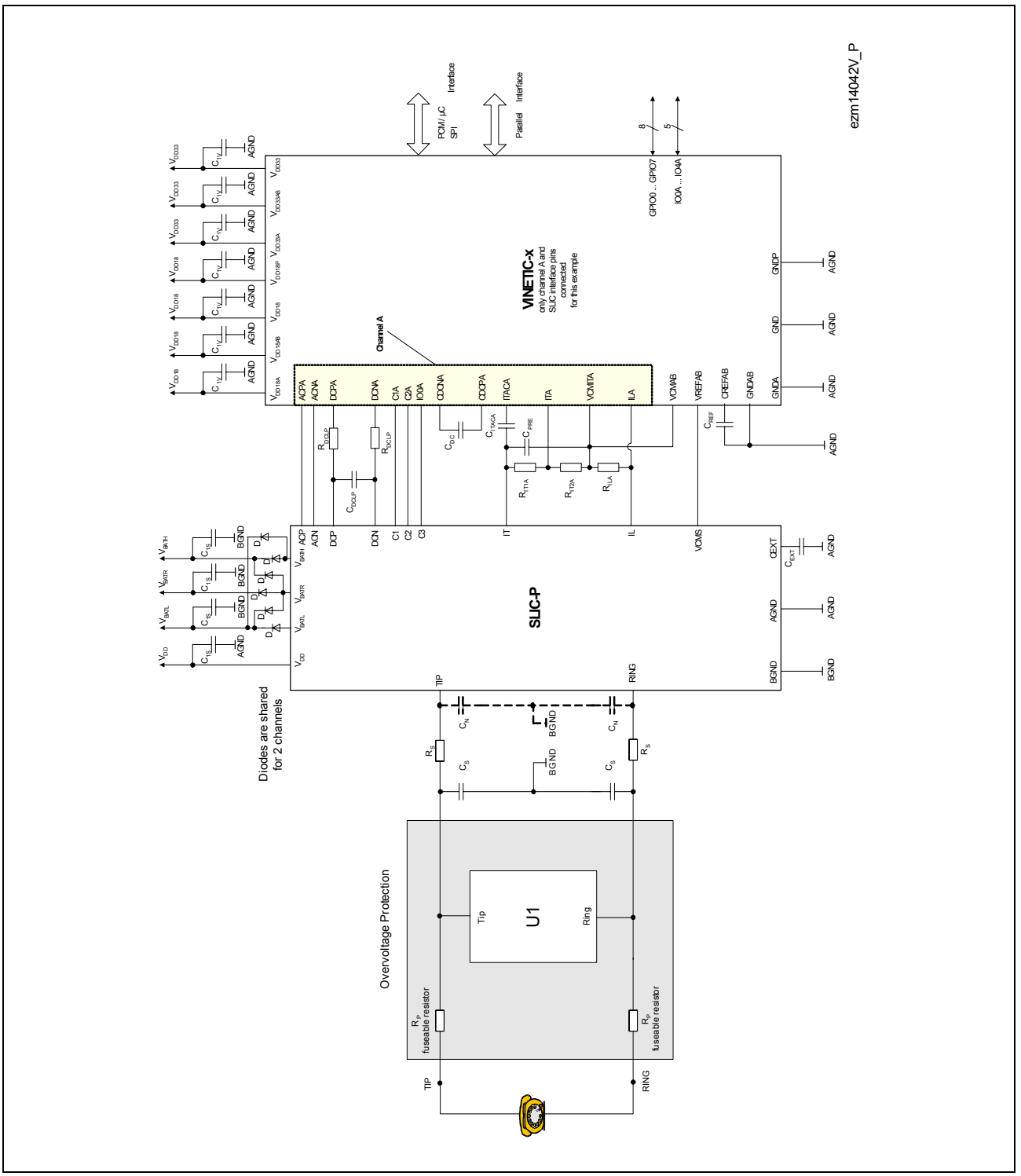

Figure 4 Application Circuit Internal Ringing (bal. & unbal.) for SLIC-P

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7.1.2 Bill of Materials Internal Ringing

Chapter 5.1.2, page 117: C_N, R_{DCLP} and C_{DCLP} added.

Table 6 External Components in Application Circuit Internal Ringing

No.	Symbol	Value	Unit	Tol.	Rating	SLIC-E/-S Systems	TSLIC-E/-S Systems	SLIC-P Systems
8	C_N 1)	100	pF	10%	100 V	x	x	
8	C_N 1)	100	pF	10%	250 V			x
8	R_{DCLP}	33	Ω	1%	–	x	x	x
4	C_{DCLP}	4.7	µF	10%	6.3 V	x	x	x

1) Optional COG type capacitor (e.g. TDK C1608COG2A101J) for applications in noisy environments (such as close WLAN transmitters) to avoid coupling of disturbances from HF radiation into the voice band.

7.1.3 External Ringing with SLIC-LCP

Chapter 5.1.3, page 118: C_{FB}, R_{DCLP} and C_{DCLP} added.

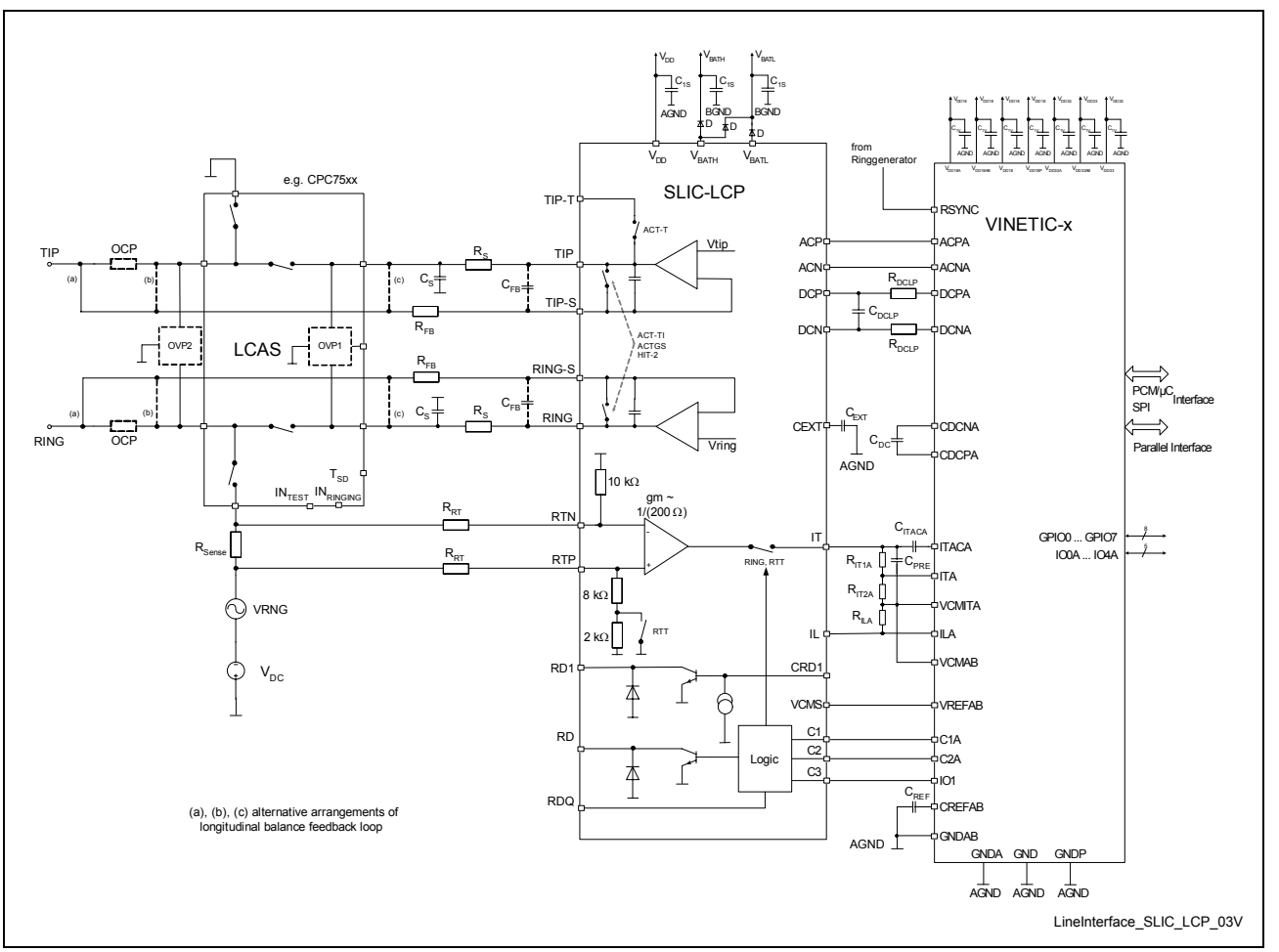

Figure 5 Application Circuit External Ringing for SLIC-LCP (LCAS)

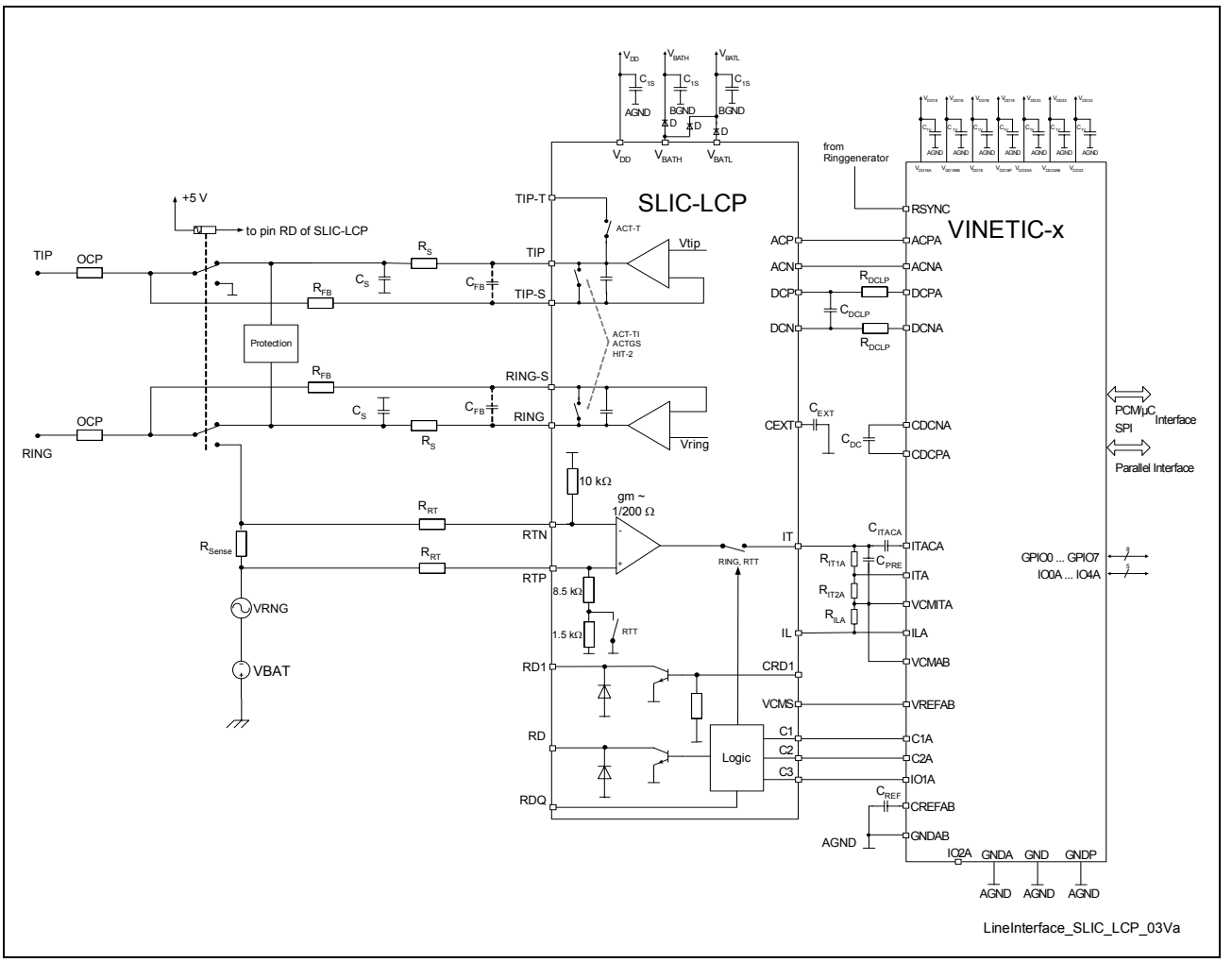

Figure 6 Application Circuit External Ringing for SLIC-LCP with Relays

7.1.4 Bill of Materials External Ringing

Chapter 5.1.4, page 120: C_{FB}, R_{DCLP} and C_{DCLP} added.

Table 7 External Components in Application Circuit External Ringing

No.	Symbol	Value	Unit	Tol.	Rating
8	C_{FB} 1)	22	pF	5%	100 V
8	R_{DCLP}	33	Ω	1%	–
4	C_{DCLP}	4.7	µF	10%	6.3 V

1) Longitudinal balance feedback stabilization

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7.2 Signal Paths - DC Feeding

Chapter 2.2, page 22: R_{DCLP} and C_{DCLP} added.

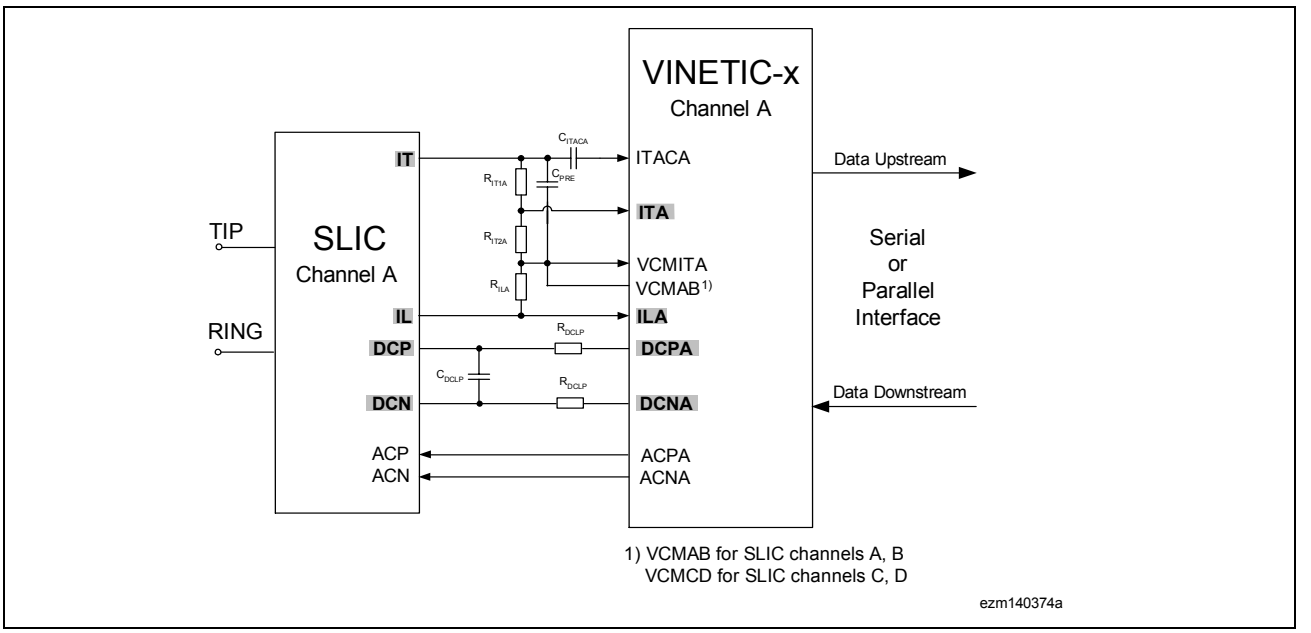

Figure 7 Signal Paths - DC Feeding

7.3 Signal Paths - AC Transmission

Chapter 2.3, page 32: R_{DCLP} and C_{DCLP} added.

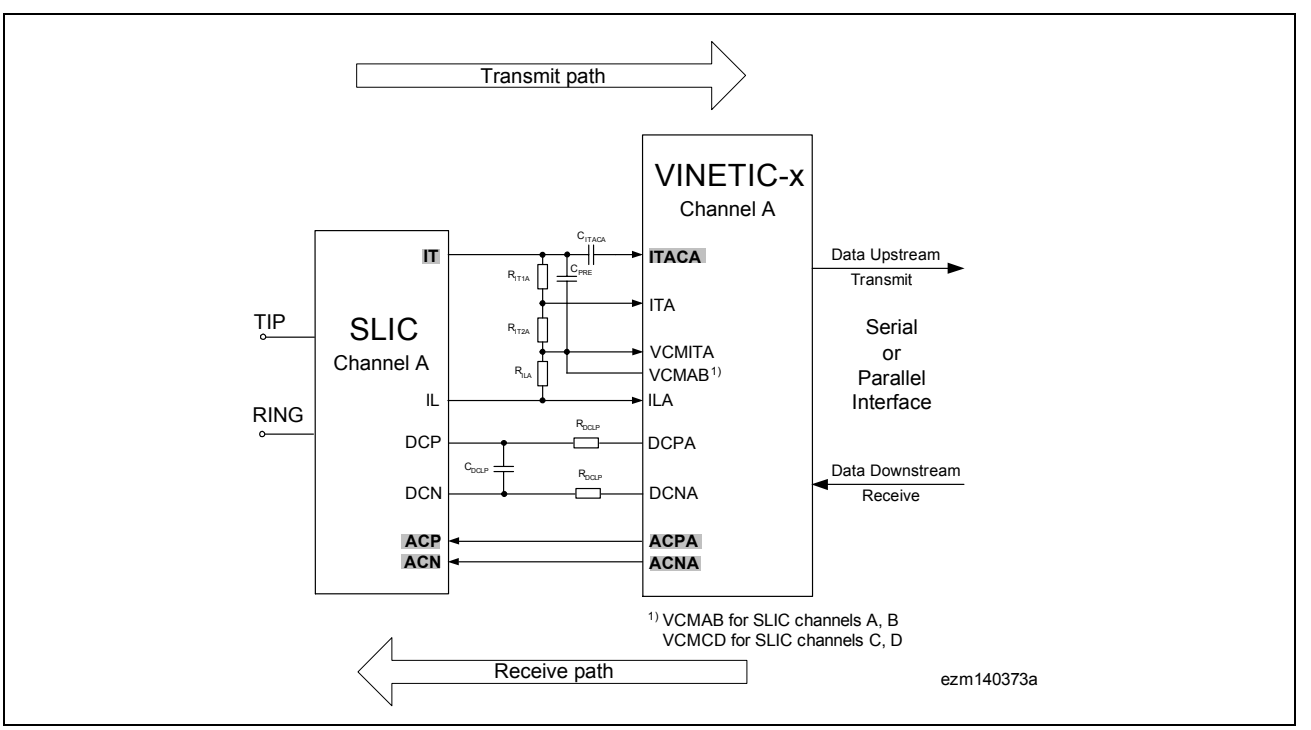

Figure 8 Signal Paths - AC Transmission