SMART 4268

SLIC-DC Evaluation Board

SLIC-DC, PEF 4268, V1.1/V1.2

Hardware Description

Communications

Infineon technologies

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Revision History: **2005-08-29** Rev.1.3

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Page	**Subjects (major changes since last revision)**
all	Change to SMART 4268 V1.2

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1 Introduction

1.1 Overview

The SLIC-DC Evaluation Board SMART 4268 serves as evaluation platform for SLIC-DC PEF 4268 together with the VINETIC and the DuSLIC chip set. It allows to run 2 POTS lines in parallel. Additionally a VINETIC Evaluation Board EASY 334 V1.2 (or later) or DuSLIC Evaluation Board SMART 3265 V2.1 (or later) has to be connected.

The SLIC-DC Evaluation Board SMART 4268 V1.2 operates with SLIC-DC PEF 4268 in P-DSO-24-8 or P-TQFP-48-1 package. Both SLIC-DC devices are placed in a socket (default). Channel B uses SLIC-DC in a P-DSO-24-8package, channel A is equipped with SLIC-DC in P-TQFP-48-1 package.

The power supply voltage can be connected by using banana plugs or a plug-in power supply connector. The SLIC-DC Evaluation Board is not powered by the connected VINETIC or DuSLIC board.

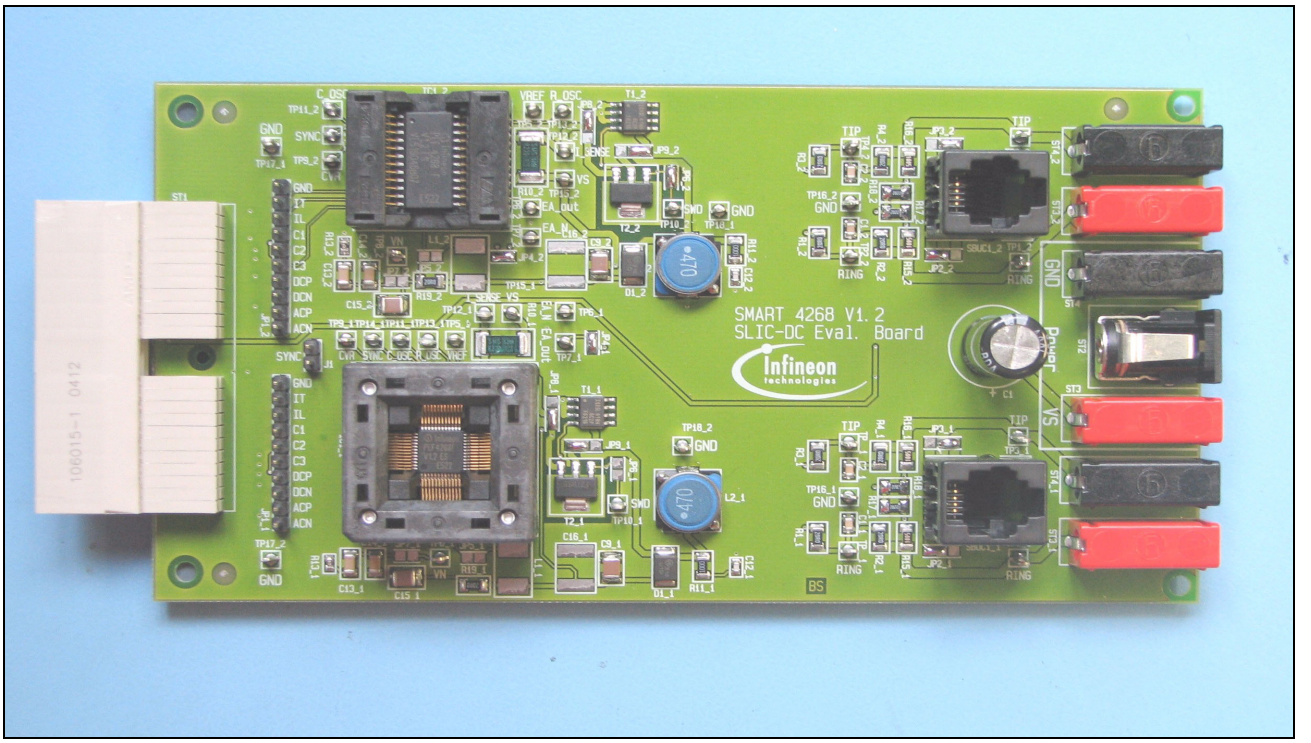

Figure 1 SLIC-DC Evaluation Board SMART 4268

1.2 Features of SLIC-DC Evaluation Board SMART 4268

- Compatible to VINETIC Evaluation Board EASY 334 (V1.2 or later) and DuSLIC Evaluation Board SMART 3265 V2.1 (or later)
- Both package versions of SLIC-DC can be evaluated, P-TQFP-48-1 and P-DSO-24-8 package

- Test pins for all important signal lines
- Banana plugs and western jacks (RJ-11) for each telephone line
- Banana plugs for external laboratory power supply
- Power supply connector to connect a +12 V plug-in power supply (included in the package)
- Two mounting options for the DC/DC converter possible

2 Operational Information

2.1 SMART 4268 with EASY 334 V1.2 (or later)

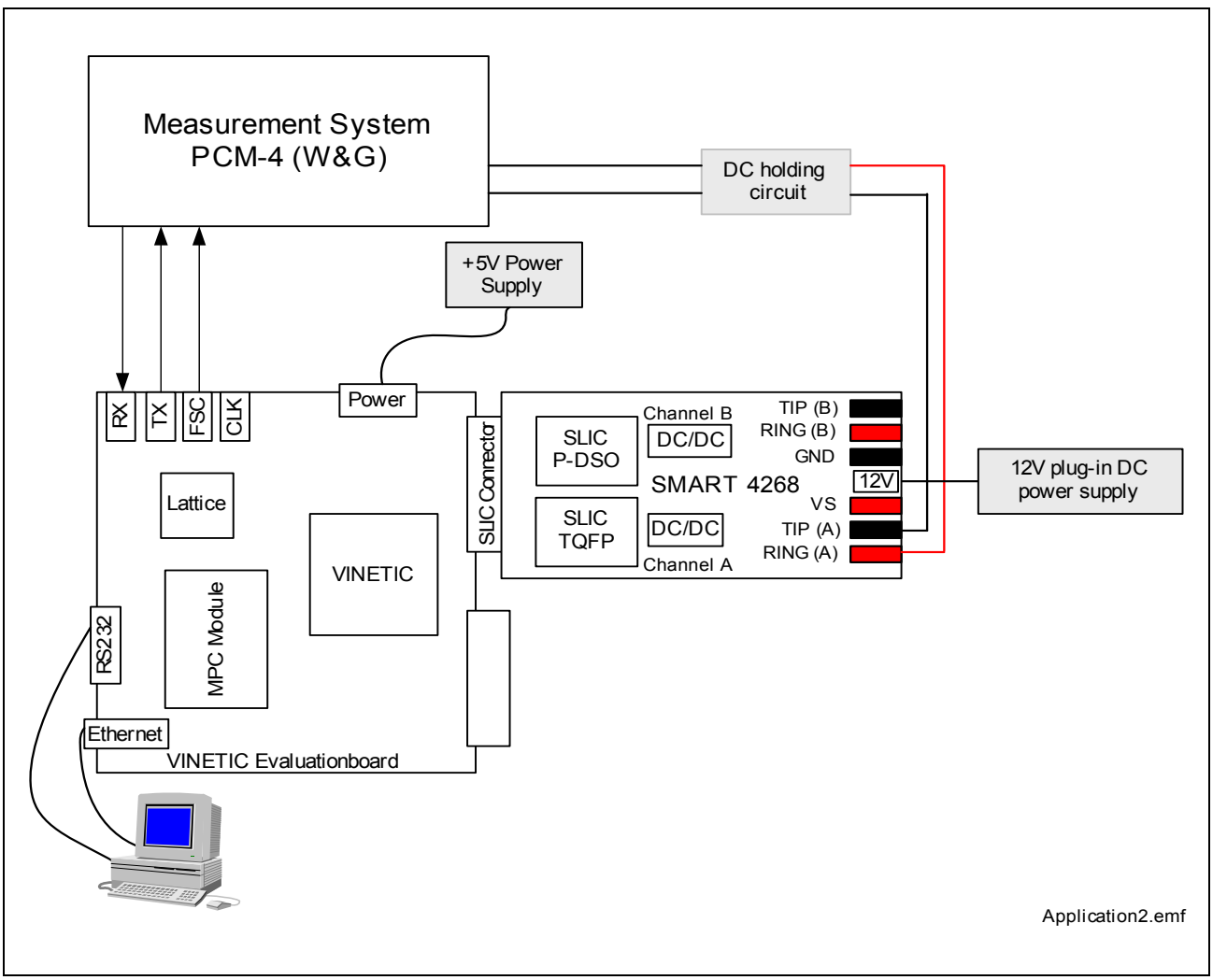

Figure 2 Connection with EASY 334 V1.2 (VINETIC) for PCM-4 Measurements

The connection of SMART 4268 with EASY 334 is shown in **Figure 2**. PCM-4 measurements can be performed in this configuration. The VINETIC chip set supports up to four SLICs. Therefore, two SLIC-DC Evaluation Boards can be connected to one VINETIC Evaluation Board. EASY 334 is configured and controlled by the MPC Module. The PC controls the system via an Ethernet interface. The voltage for the SLIC-DC Evaluation Board is connected using a +12 V plug-in DC power supply (included with the SLIC-DC Evaluation package).

2.2 SMART 4268 with SMART 3265 V2.1

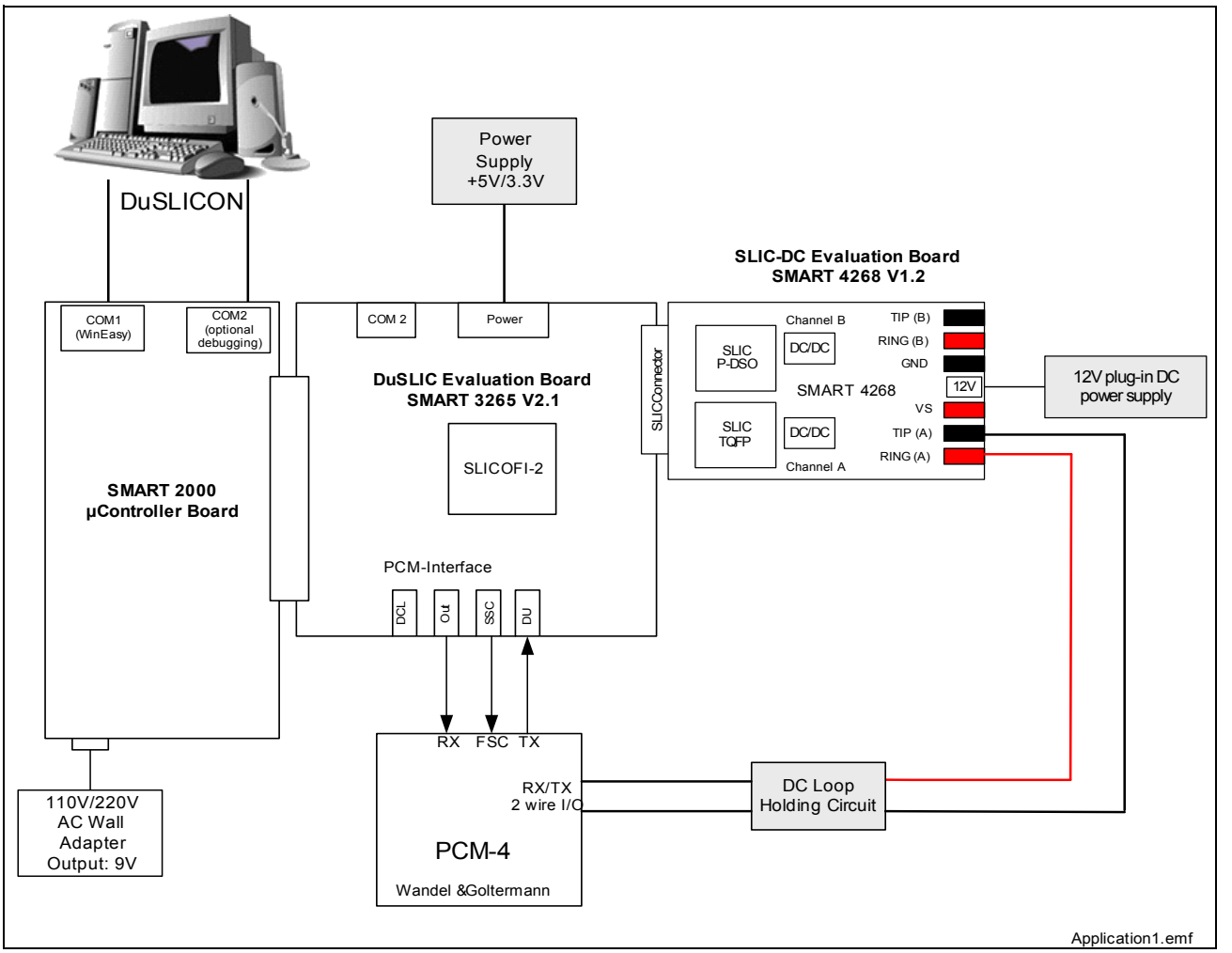

Figure 3 Connection with SMART 3265 V2.1 for PCM-4 Measurements

The connection of DuSLIC Evaluation Board SMART3265 V2.1 and SLIC-DC Evaluation Board is shown in **Figure 3**. The DuSLIC chip set supports two SLIC devices. The DuSLIC Evaluation Board is configured and controlled by the SMART2000 Mainboard. The Mainboard is controlled by the PC via the RS232-interface. All necessary power supply voltages for the DuSLIC are connected to the DuSLIC Evaluation Board, the voltage for the SLIC-DC Evaluation Board is connected using a +12V plug-in DC power supply (part of the SLIC-DC Evaluation package). The Mainboard is powered separately using an AC/DC plug-in power supply.

3 Circuitry

3.1 Block Diagram

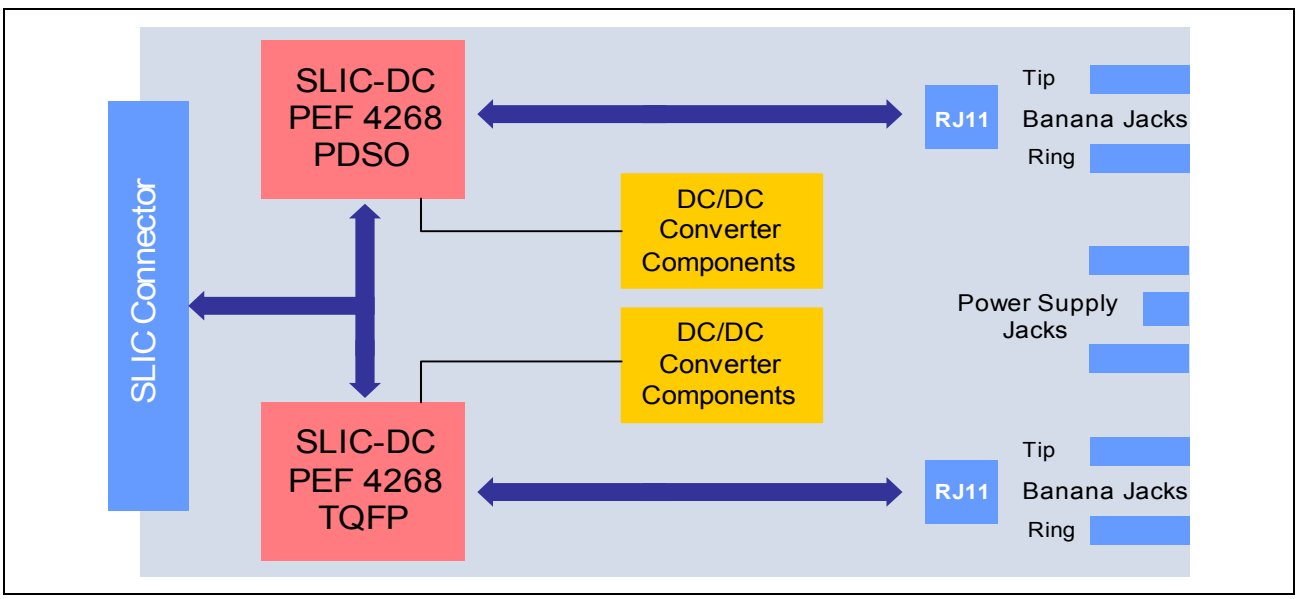

Figure 4 Block Diagram of the SLIC-DC Evaluation Board V1.1/V1.2

The SLIC-DC Evaluation Board SMART 4268 consists of 5 main blocks:

- SLIC connector
- SLICs (sockets for both packages)
- Line connectors
- 2 different DC/DC converter circuitries (usage with PMOS or bipolar transistor)
- Power Supply connectors

3.2 SLIC-DC Circuit

The board is populated with two SLIC-DC PEF 4268 devices for serving two channels. Channel B is equipped with P-DSO-24-8package; channel A is equipped with P-TQFP-48-1 package. The SLIC devices can either be placed in the socket (default) or can be directly soldered onto the board, if the sockets are removed.

3.3 SLIC Connector

The SLIC-DC Evaluation Board SMART 4268 is connected to the VINETIC Evaluation Board EASY 334 or the DuSLIC Evaluation Board SMART 3265 V2.1 via an 110 pin connector.

3.4 Line Connectors

The board has two different POTS line connections, a 6/4 western plug (RJ11) or banana plugs (for using test equipment) . As default, the inner wires of the 6/4 western plug (RJ11) are used.

3.5 Power Supply Connectors

The power supply voltage for the SLIC-DC Evaluation Board SMART 4268 needs to be provided by the plug-in power supply connector or via the two banana plugs. The default power supply voltage is +12 V. A plug-in switching power supply is part of the SLIC-DC Evaluation package. The recommended voltage range depends on the switching transistor used (bipolar or PMOS) according to the SLIC-DC PEF 4268 data sheet.

Table 1 Power Supply and Voltage Ranges

Supply	PEF 4268
VS	+12 V default (+9 V..+20 V), if ZX5T955G used; (+9 V....+40 V), if IRF 6216 used

When applying supply voltages to the SLIC, refer to the absolute maximum ratings of the SLIC data sheet.

3.6 DC/DC Circuitries

The two channels on SMART 4268 differ in SLIC package and switch transistor type. By setting soldering bridges the transistor type can be changed.

Default settings:
Channel A: SLIC-DC in TQFP package and bipolar transistor ZX5T955G used
Channel B: SLIC-DC in PDSO package and PMOS transistor IRF 6216 used

3.7 Measurement Points

The on-board measurement points are listed in **Table 2**.

Table 2 Measurement Points Description

Pin	Function		Pin	Function
TP1_1	RING Channel A		TP2_1	RING at C1_1
TP3_1	TIP Channel A		TP4_1	TIP at C2_1
TP5_1	VREF		TP6_1	EAO
TP7_1	EAN		TP8_1	VN
TP9_1	CVR		TP10_1	SWD
TP11_1	COS		TP12_1	SENSE
TP13_1	ROS		TP14_1	SYNC
TP15_1	VS		TP16_1	GND
TP17_1	GND		TP18_1	GND
TP1_2	RING Channel B		TP2_2	RING at C1_2
TP3_2	TIP Channel B		TP4_2	TIP at C2_2
TP5_2	VREF		TP6_2	EAO
TP7_2	EAN		TP8_2	VN
TP9_2	CVR		TP10_2	SWD
TP11_2	COS		TP12_2	SENSE
TP13_2	ROS		TP14_2	SYNC
TP15_2	VS		TP16_2	GND
TP17_2	GND		TP18_2	GND

3.8 Measurement Header JP1_1, JP1_2

Each channel has a measurement header to have access to the signals between SLIC-DC and VINETIC/DuSLIC.

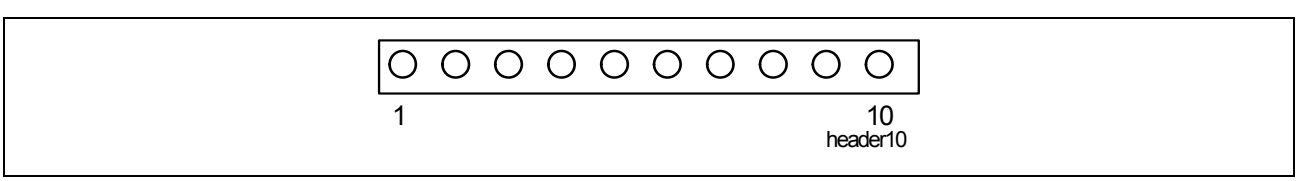

Figure 5 Measurement Header

Table 3 Measurement Header JP1_1, JP1_2

Pin	Signal
1	ACN
2	ACP
3	DCN
4	DCP
5	C3 of the SLIC is connected to IO0 of VINETIC and IO2 of DuSLIC
6	C2
7	C1
8	IL
9	IT
10	GND

3.9 SLIC ID Module Recognition

Every SLIC module has a resistor coded identification at four pins of the SLIC Connector. With no SLIC- DC Evaluation Board connected to the VINETIC Board, the ID is '1111_b'. The SLIC-DC Evaluation Board SMART 4268 has the ID '0101_b'. Therefore, the resistors R1, R2, are connected to the SLIC Connector to set the bits to '0'.

4 Connector and Header Pin-outs

4.1 SLIC Connector (ST1)

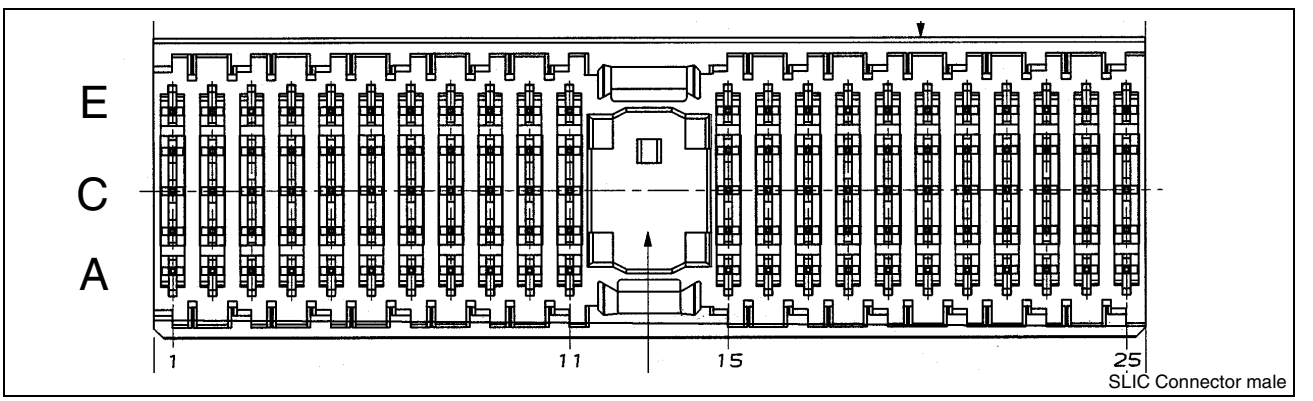

Figure 6 SLIC Connector Front View

Table 4 SLIC-Connector (ST1)

Pin No.	Symbol	I/O	Function
A1	TEST1		**Channel B** Sensing Ring line between resistors (not used)
A2	RINGCHB		**Channel B** Line testing signal at voltage divider at the TIP side
A3	ANALOG2B	O	**Channel B** Line testing signal at voltage divider at the RING side
A4	TEST2	O	**Channel B** Sensing Tip line between resistors (not used)
A5	IO3B	I/O	**Channel B** User programmable IO with analog functionality (not used)
A6	VCM		**Reference voltage for SLICs (IL, IT, ITAC, VCMIT)** VCMAB or VCMCD of VINETIC
A7	IO4B	I/O	**Channel B** User programmable IO with analog functionality (not used)
A8			**not used**
A9	VCC	I	**Power Supply** +5 V (not used)

Table 4 SLIC-Connector (ST1) (cont'd)

Pin No.	Symbol	I/O	Function
A10	VCC	I	**Power Supply** +5 V (not used)
A11	VCC	I	**Power Supply** +5 V (not used)
A12	V1V8	I	**Power Supply** +1.8 V (not used)
A13	V1V8	I	**Power Supply** +1.8 V (not used)
A14	GPIO0	I/O	**General Purpose IO GPIO0[1] (not used)**
A15	-		**not used**
A16	-		**not used**
A17	ANALOG1A	O	**Channel A** Line testing signal at voltage divider at the RING side
A18	ANALOG2A	O	**Channel A** Line testing signal at voltage divider at the TIP side
A19	-		**not used**
A20	IO3A	I/O	**Channel B** User programmable IO with analog functionality (not used)
A21	-		**not used**
A22	IO4A	I/O	**Channel A** User programmable IO with analog functionality (not used)
B1	GND	I	**Power Supply** Ground
B2	IO0B	I/O	**Channel B** User programmable IO, C3 signal of the SLIC must be connected (not used)
B3	IO1B	I/O	**Channel B** User programmable IO with relay driver functionality (not used)
B4	GND	I	**Power Supply** Ground

Table 4 SLIC-Connector (ST1) (cont'd)

Pin No.	Symbol	I/O	Function
B5	GND	I	**Power Supply** Ground
B6	GND	I	**Power Supply** Ground
B7	VCMITB	O	**Channel B** Reference signal for transversal/longitudinal current sensing (not used)
B8			**not used**
B9	V3V3	I	**Power Supply** +3.3 V (not used)
B10	V3V3	I	**Power Supply** +3.3 V (not used)
B11	V3V3	I	**Power Supply** +3.3 V (not used)
B12	V1V8	I	**Power Supply** +1.8 V (not used)
B13	ID0	O	**SLIC Module ID signal ID0 of ID[3:0]**
B14	GPIO1	I/O	**General Purpose IO GPIO1[2] (not used)**
B15	-		
B16	GND	I	**Power Supply** Ground
B17	IO0A	I/O	**Channel A** User programmable IO, C3 signal of the SLIC must be connected (not used)
B18	IO1A	I/O	**Channel A** User programmable IO with relay driver functionality (not used)
B19	GND	I	**Power Supply** Ground
B20	GND	I	**Power Supply** Ground
B21	GND	I	**Power Supply** Ground

Table 4 SLIC-Connector (ST1) (cont'd)

Pin No.	Symbol	I/O	Function
B22	VCMITA	O	**Channel A** Reference signal for transversal/longitudinal current sensing (not used)
			not used
C1	ITACB	O	**Channel B** Transversal current AC
C2	GND	I	**Power Supply** Ground
C3	ITB	O	**Channel B** Transversal Current (AC + DC) (not used)
C4	GND	I	**Power Supply** Ground
C5	DCPB	O	**Channel B** two wire output voltage
C6	ACNB	O	**Channel B** voltage controlling Tip wire
C7	GND	I	**Power Supply** Ground
C8			**not used**
C9	VHR	I	**Power Supply** VHR (not used)
C10	VBATH	I	**Power Supply** VBATH (not used)
C11	VBATL	I	**Power Supply** VBATL (not used)
C12	VBATR	I	**Power Supply** VBATR (not used)
C13	ID1	O	**SLIC Module ID signal ID1 of ID[3:0]**
C14	GPIO2	I/O	**General Purpose IO GPIO2[3] (not used)**
C15	-		**not used**
C16	ITACA	O	**Channel A** Transversal current AC

Table 4 SLIC-Connector (ST1) (cont'd)

Pin No.	Symbol	I/O	Function
C17	GND	I	**Power Supply** Ground
C18	ITA	O	**Channel A** Transversal Current (AC + DC)
C19	GND	I	**Power Supply** Ground
C20	DCPA	O	**Channel A** two wire output voltage
C21	ACNA	O	**Channel A** voltage controlling Tip wire
C22	GND	I	**Power Supply** Ground
			not used
D1	GND	I	**Power Supply** Ground
D2	GND	I	**Power Supply** Ground
D3	GND	I	**Power Supply** Ground
D4	IO2B	I/O	**Channel B** User programmable IO with analog functionality (not used)
D5	GND	I	**Power Supply** Ground
D6	GND	I	**Power Supply** Ground
D7	VCMSB	I	**Channel B** Reference voltage, VREF of VINETIC (+1.5 V) (not used)
D8			**not used**
D9	VHR	I	**Power Supply** VHR (not used)
D10	VBATH	I	**Power Supply** VBATH (not used)

Table 4 SLIC-Connector (ST1) (cont'd)

Pin No.	Symbol	I/O	Function
D11	VBATL	I	**Power Supply** VBATL (not used)
D12	VBATR	I	**Power Supply** VBATR (not used)
D13	ID2	O	**SLIC Module ID signal ID2 of ID[3:0]**
D14	GPIO3	I/O	**General Purpose IO GPIO3[4] (not used)**
D15	-		
D16	GND	I	**Power Supply** Ground
D17	GND	I	**Power Supply** Ground
D18	GND	I	**Power Supply** Ground
D19	IO2A	I/O	**Channel A** User programmable IO with analog functionality (not used)
D20	GND	I	**Power Supply** Ground
D21	GND	I	**Power Supply** Ground
D22	VCMSA	I	**Channel A** Reference voltage, VREF of VINETIC (+1.5 V) (not used)
E1	GND	I	**Power Supply** Ground
E2	ILB	O	**Channel B** Longitudinal current input
E3	C1B	O	**Slic operation mode channel B** Ternary logic output, indication thermal input
E4	C2B	O	**Slic operation mode channel B** Ternary logic output

Table 4 SLIC-Connector (ST1) (cont'd)

Pin No.	Symbol	I/O	Function
E5	DCNB	O	**Channel B** two wire output voltage
E6	ACPB	O	**Channel B** voltage controlling Ring wire
E7	GND	I	**Power Supply** Ground
E8			**not used**
E9	VHR	I	**Power Supply** VHR (not used)
E10	VBATH	I	**Power Supply** VBATH (not used)
E11	VBATL	I	**Power Supply** VBATL (not used)
E12	VBATR	I	**Power Supply** VBATR (not used)
E13	ID3	O	**SLIC Module ID signal ID3 of ID[3:0]**
E14	RSYNC		**Ring signal synchronization pulse**
E15	-		**not used**
E16	GND	I	**Power Supply** Ground
E17	ILA	O	**Channel A** Longitudinal current input
E18	C1A	I/O	**Slic operation mode channel A** Ternary logic output, indication thermal input
E19	C2A	O	**Slic operation mode channel A** Ternary logic output
E20	DCNA	O	**Channel A** two wire output voltage
E21	ACPA	O	**Channel A** voltage controlling Ring wire
E22	GND	I	**Power Supply** Ground

1) On VINETIC Evaluation Board channel A and B, connector for channel C and D use GPIO4

2) On VINETIC Evaluation Board channel A and B, connector for channel C and D use GPIO5

3) On VINETIC Evaluation Board channel A and B, connector for channel C and D use GPIO6

4) On VINETIC Evaluation Board channel A and B, connector for channel C and D use GPIO7

4.2 Tip/Ring Interface Connector

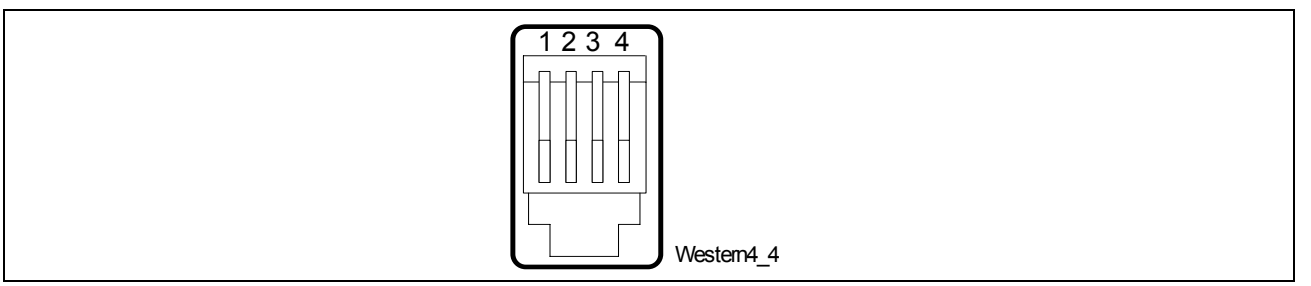

Figure 7 Tip/Ring Interface Connector (SBUC1_1, SBUC1_2)

Table 5 Pin-out of the Western Plug (SBUC1_1, SBUC1_2)

Pin No.	Symbol	I/O	Function
1	RING	I/O	**Ring line** J2_1 /J2_2: connection of Pin 1 and Pin 2
2	RING	I/O	**Ring line** J2_1 /J2_2: connection of Pin 2 and Pin 3 **(default)**
3	TIP	I/O	**Tip line** J3_1 /J3_2: connection of Pin 1 and Pin 2 **(default)**
4	TIP	I/O	**Tip line** J3_1 /J3_2: connection of Pin 2 and Pin 3

4.3 Power Supply Connector

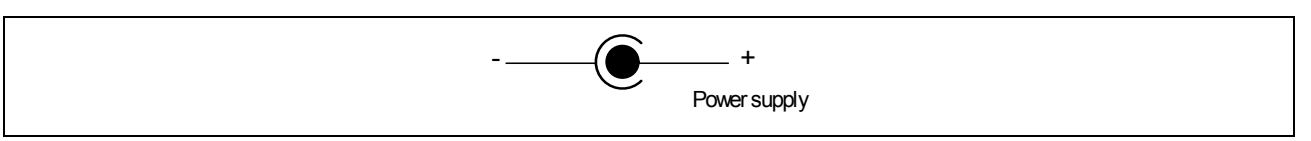

Figure 8 Plug-in Power Supply Connector

The board can be powered by 2 the included AC/DC +12 V plug-in power supply or any other +9 V..+20 V supply with the polarity shown in **Figure 8**. This voltage can be increased, if on both channels PMOS transistors are used.

5 Components

5.1 Floor Plan of the Board

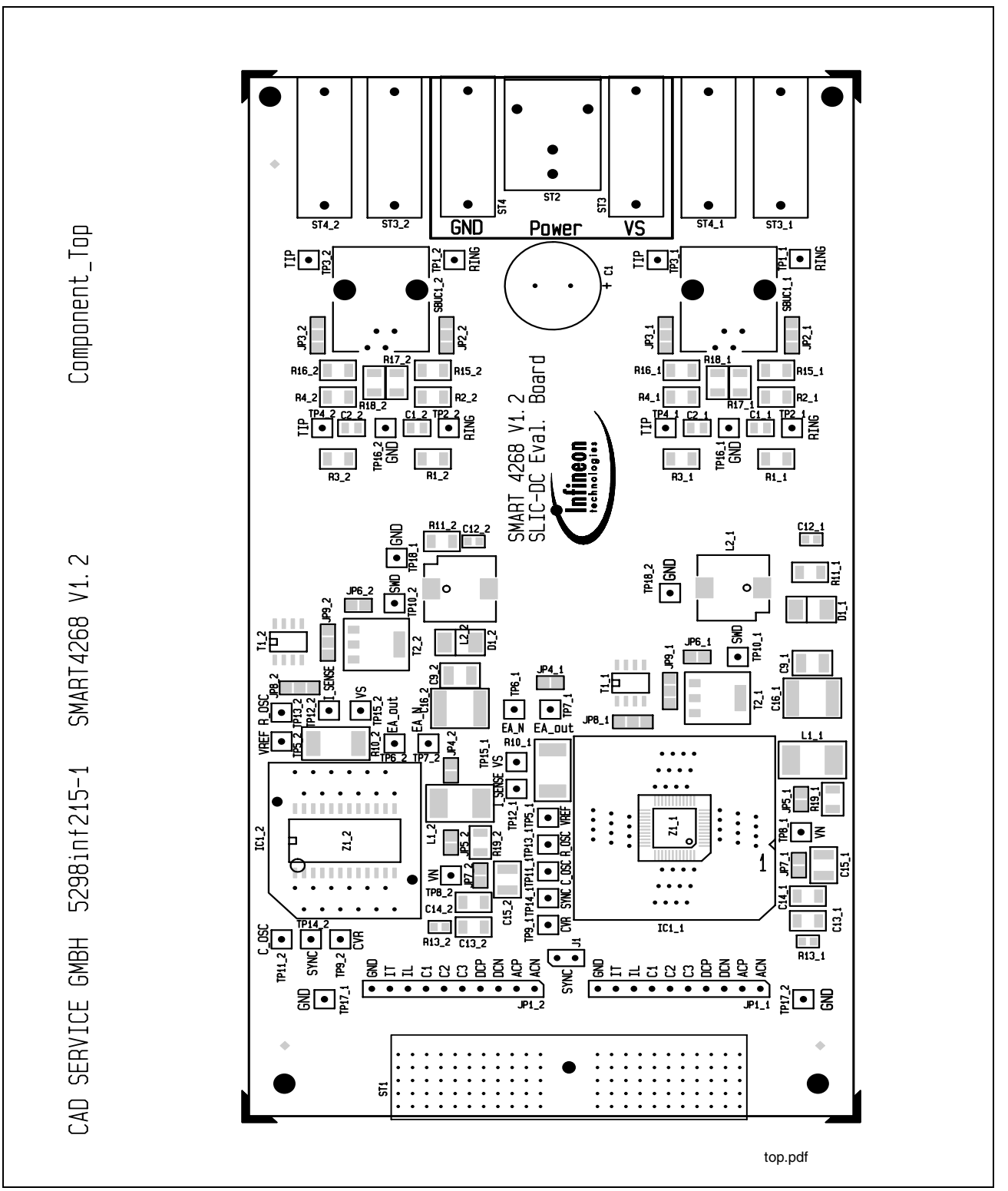

Figure 9 Floor Plan of SLIC-DC Evaluation Board V1.2 (Top View)

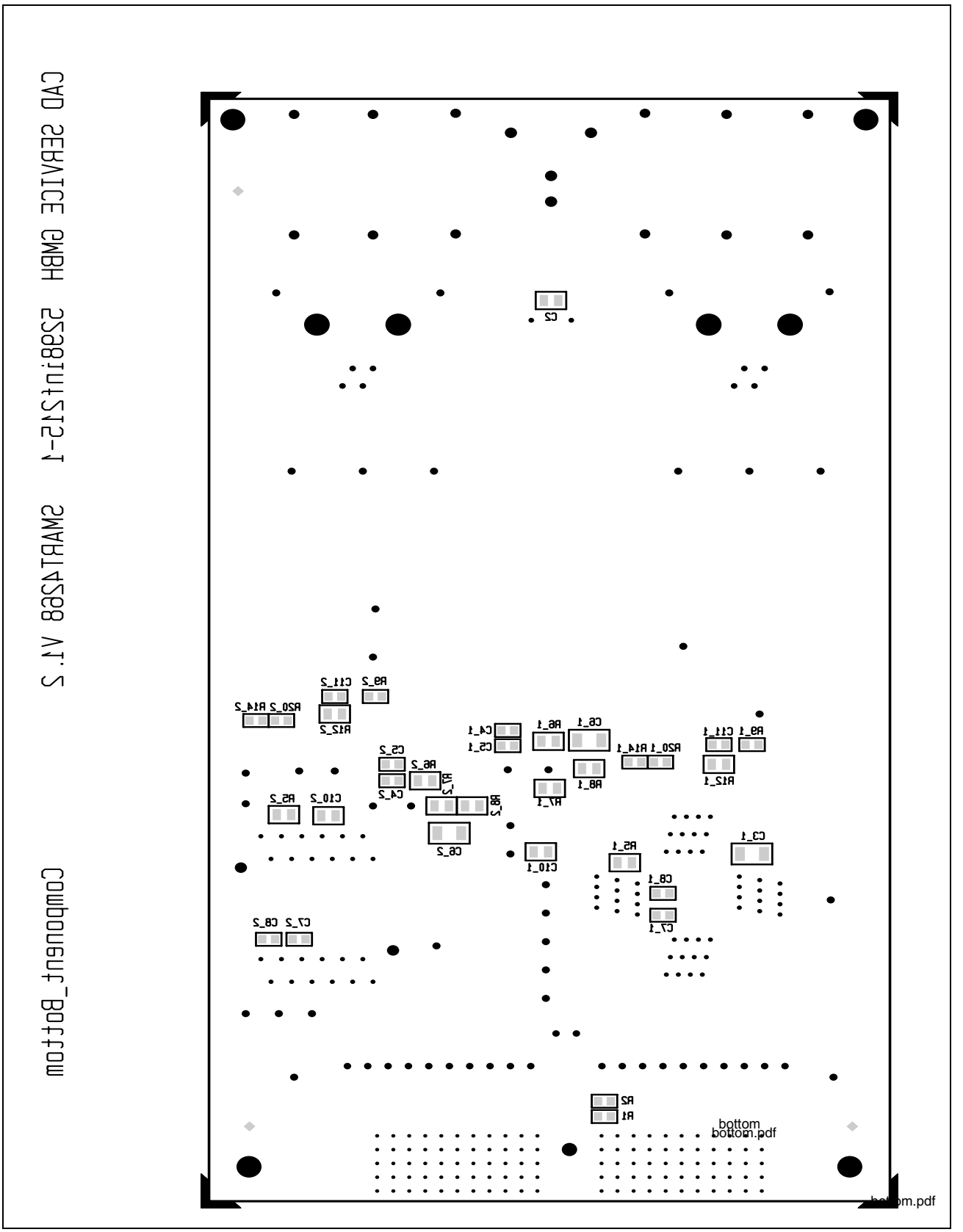

Figure 10 Floor Plan of SLIC-DC Evaluation Board V1.2 (Bottom View)

6 Configurations

This chapter describes all configurations of the SLIC-DC Evaluation Board SMART 4268. All jumpers, solder bridges, their functions and the possible power supply solutions are described here.

6.1 Selecting the Power Supply Voltage on the Board

The board is fed by the banana plugs or by the plug-in DC power supply. At the banana jacks the applied power supply may vary between +9 V..+40 V, if PMOS-FET is used on both channels. **If the bipolar transistors ZX5T955G are connected, a supply range of VS = +9 V..+20 V is allowed**. The external +12 V DC plug-in power supply (included with the package) is connected at jack ST2.

6.2 Setting Transistor Type

The switching transistors on SMART 4268 are SMD-types. When changing such devices, pads can easily be destroyed. Therefore, both transistor types are mounted. The devices are connected to the circuitry via soldering bridges. The default mounting of the SLIC-DC Evaluation Board SMART 4268 V1.2 is shown in **Table 6**.

Default settings:

Channel A: PNP transistor ZX5T955G used
Channel B: PMOS IRF 6216 used

Table 6 Setup the PMOS-Transistor or PNP Transistor

Solder bridge	Connection	Component	Transistor
JP8_1,JP8_2	1-2		PMOS-FET
JP9_1,JP9_2	1-2		
JP6_1,JP6_2	closed		
JP8_1,JP8_2	2-3		PNP Transistor
JP9_1,JP9_2	2-3		
JP6_1,JP6_2	open		

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