User's Manual, DS1, July 2002

EASY 334

VINETIC Evaluation Board

EASY 334 V1.2

PEB 3324 V1.x

Hardware Description

Wired Communications

Infineon technologies

Never stop thinking.

User's Manual

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Preface

Organization of this Document

The *EASY 334 User's Manual* consists of six chapters:

- Chapter 1, Introduction
  Gives an introduction of the VINETIC Evaluation Board .
- Chapter 2, Overview
  Shows the concept and the Block Diagram.
- Chapter 3, System Structure
  Deals with the system structure and the functionality.
- Chapter 4, Interfaces
  Describes the interface components of the EASY 334 VINETIC Evaluation Board.
- Chapter 5, Board Control
  Deals with all blocks and Register Settings of the Board.
- Chapter 6, Pinout Descriptions
  Describes all interfaces of the EASY 334 VINETIC Evaluation Board.

Related Documentation

The *EASY 334 User's Manual* does not include technical details of the chip set itself. Recommended documentation for the chip includes:

- Voice and Internet Enhanced Telephony Interface Circuit, VINETIC, PEB 3324
- User's Manual-Software Description, VINETIC, PEB 3324
- SLICs SLIC-S/-S2
  SLIC-E/-E2
  SLIC-P
  TSLIC-S
  TSLICE

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1 Introduction

The EASY 334 is used to evaluate the VINETIC device.

The VINETIC is a device for accessing the analog telephone line, including a powerful DSP for voice processing as well as for data compression.

Although the telephone net by itself is almost digital and also more and more access lines have been replaced by digital or xDSL lines, the requirement for analog telephone access is increasing. Most of xDSL indeed, e.g. Integrated Access Devices (IAD), Voice Gateways (VG) or Cable Modems integrate also Voice over IP (VoIP), Voice over ATM (VoATM) Voice over DSL (VoDSL).

To access these features the users are still using analog telephone sets. Therefore the new evolving technologies require all the standard features that analog access cards provide, like feeding, ringing, touch tone / DTMF detection, Caller-ID generation and many more. Additionally most of the new technologies also use a different way of network, based on packetized voice. The most widely known networks are the Internet Protocol (IP) and the Asynchronous Transfer Mode (ATM) network.

These packetized networks share their flow typically with all kinds of media like data and video. In order to keep the voice bandwith minimal, voice compression is used. At the same time echo originating from the analog termination has to be cancelled, both at the user side, and on the media gateway side.

The VINETIC family comprises voice processor and SLIC devices that work seamless together. The VINETIC is able to use the same SLICs as in the well known DuSLIC family, easing migration from DuSLIC to VINETIC by using the same analog interface.

1.1 Features of VINETIC

- Fully programmable 4-channel codec with enhanced signal processing capabilities
- Glueless interface to Infineon SLIC family: SLIC-S/-S2, TSLIC-S, SLIC-E/-E2, TSLIC-E and SLIC-P

1.1.1 Integrated DSP Features

- Integrated VoIP/VoDSL DSP with SRAM and software download capability
- Integrated DTMF generator
- Integrated DTMF decoder
- Integrated Caller ID (FSK) generator
- Integrated fax/modem detection by Universal Tone Detection unit (UTD), In-band tone detection

- Optimized filter structure for modem transmission, enhanced modem performance for improvement of V.90 transmission
- Multi-party conferencing
- G.711, G.711 Annex I (BFM), G.711 Annex II (VAD + CNG)
- Voice compression: G.723.1, G.726, G.728, G.728 Annex I (BFM), G.729 A, B,
- G.729 E
- Voice Activity Detection (VAD)
- Comfort Noise Generation (CNG)
- Algorithms for Line Echo Cancellation G.165/G.168
  (exceeding 16 - 128 ms tail lenght)
- T.38 Fax Relay Support
- CAS/RBS signaling filter to enhance modem performance
- Support for packet encapsulation: AAL2 (ATM/DSL) and RTP (TCP/IP)
- Packet preprocessing
- Codec/SLIC Features
- Specification in accordance with ITU-T Recommendation G.712,
- ITU-T Recommendation Q.552 for interface Z and applicable LSSGR
- Internal balanced/unbalanced ringing capability up to 85 Vrms
- Sinusoidal and trapezoidal ringing
- External ringing support
- Programmable teletax (TTX) generation (metering)
- Programmable battery feeding with capability for driving longer loops
- Ground/loop start signaling, Ground key detection
- Polarity reversal
- Message Waiting
- Automatic modes for POTS signaling and Power Management
- Advanced Integrated Test and Diagnosis Functions (AITDF) for local loop monitoring and production test
- On-hook transmission
- Power optimized architecture with power management capability (integrated battery switches)
- With SLIC-P additionally:
- Extreme low power
- Unbalanced Ringing

1.1.2 Interface Features

- 8 kHz PCM Transmission
- IOM-2 or PCM/µC interface selectable
- PCM interface with 2 PCM highways
- Serial control interface, SCI (Infineon) compatible, SPI compatible
- Parallel Host interface: Intel/Motorola and HPI compatible
- SLIC interface compatible with DuSLIC SLICs
- JTAG interface for boundary scan

2 Overview

2.1 Concept for the Final Evaluation System

The system consists of the EASY 334 VINETIC Evaluation Board and two SLIC modules which carry the SLIC devices.

The EASY 334 VINETIC Evaluation Board is controlled via a PC connected to the ethernet port (10Base-T). The Evaluation Board carries a CPU module from TQ Components with the MPC, the VINETIC, an IOM-2 controller and a CPLD for logic adaptions. Via two identical interface connectors the front end modules (2 analog channels each) can be connected. **Figure 1** shows the system setup:

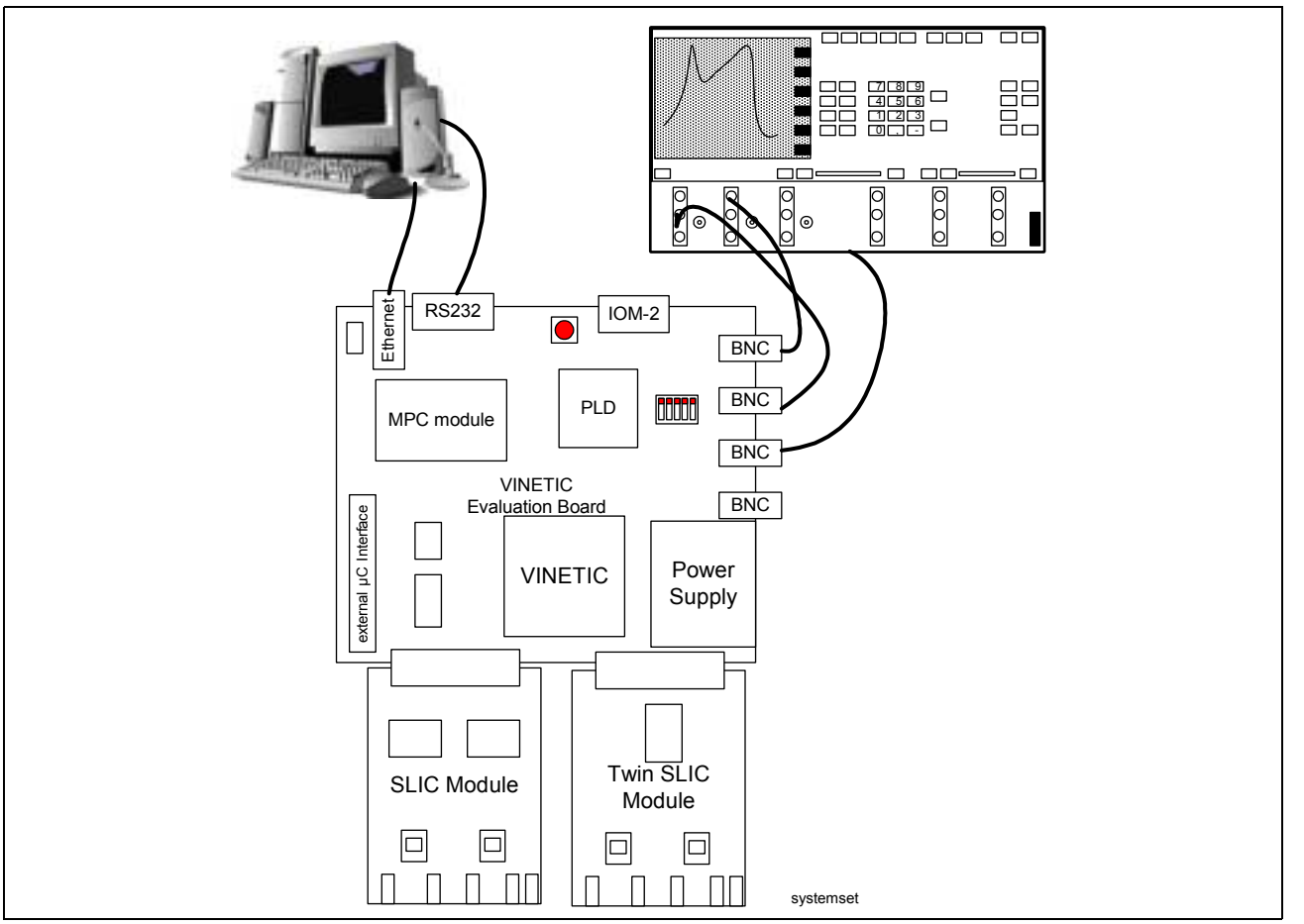


Figure 1 System Setup of the VINETIC Evaluation Board

The PC will run a control program to operate the VINETIC in different modes and will allow to evaluate and demonstrate all features. The software is described in a software specification.

The SLIC modules are not covered within this document. Please refer to separate documentations about the SLIC modules.

2.2 Block Diagram

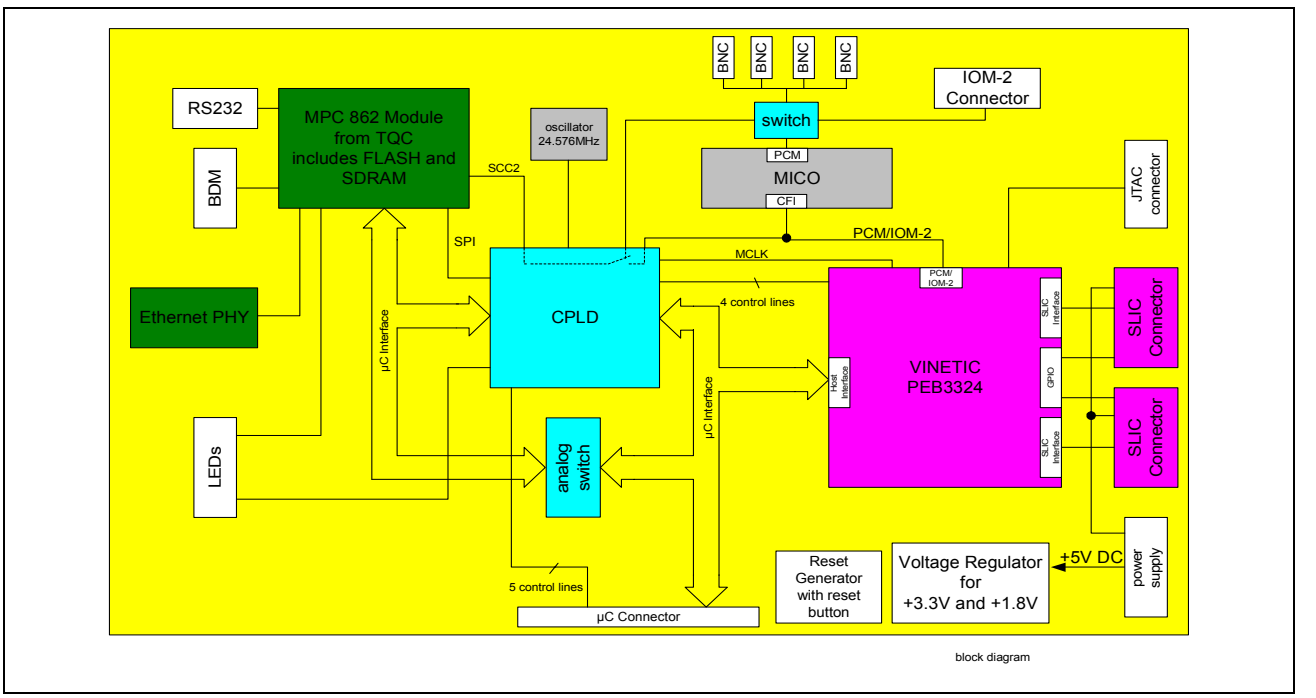


Figure 2 Block Diagram of the EASY 334 VINETIC Evaluation Board

The board consists of following functional blocks:

- VINETIC on socket (P-LQFP-176 or P-LBGA-176)
- µController add on module (Power QUICC) with, RAM, FLASH
- Clock generation
- Power supply (+3.3 V and +1.8 V) and reset generation
- Ethernet interface
- RS232 interface
- PCM interface
- IOM-2 host controller (in order to operate the board together with standard PCM test equipment when IOM mode is selected)
- Mode configuration (controlled via programmable CPLD)
- MICO (PEB 2015) Mini IOM-2 COntroller
- Interface connectors to SLIC modules
- LEDs to indicate operating mode
- JTAG Interface Connector

2.3 General Hardware Implementations

Issues concerning the above mentioned basic building blocks of the board are described in the next chapters.

The microcontroller interface of the VINETIC is not +5 V tolerant (VINETIC pads are for only +3.3 V operation tolerant). The used CPLD device connected to the microcontroller bus is a +3.3 V type with +5 V tolerant I/Os.

The µC interface of the microcontroller is buffered by a CPLD which is +5 V tolerant.

The MICO is a +5 V device. The databus of the MICO is separated from the VINETIC databus, because the VINETIC is **not** +5 V tolerant.

The standard bus mode is the Motorola Mode by default. All components of the VINETIC Evaluation Board V1.2 are accessed in Motorola Mode.

The HPI interface has to be tested by conneting an external board. In this case the parallel µC interface of the microcontroller is tristated. This µC tristate mode can also be used to connect a device that runs with one of the not on board supported bus modes like INFINEON/INTEL mux/ demux mode.

The VINETIC is able to run in both interface modes, IOM-2 or µC mode. In case of IOM2 mode, both, programming of the VINETIC, signalling and voice data are transferred via the serial IOM-2 interface. The parallel µC interface of the VINETIC is not available in IOM-2 mode.

If the VINETIC chipset is put into µC mode, programming and signalling is done via the parallel µC interface, while the voice data is handled via standard PCM-interface. In µC mode all IOM-2 related devices (MICO) are deactivated (reset is active). The clocks for the IOM-2 devices are switched off during µC mode.

2.4 General Power Supply Requirements

All required power supply voltages are provided by one single connector. The frontend module is also supplied via the VINETIC Evaluation Board V1.2.

To make the EASY 334 VINETIC Evaluation Board compatible to the former DuSLIC system, the power connector will be the same. By this way, the required +1.8 V supply voltage has to be created on the evaluation board.

The following power supply requirements exist on the EASY 334 VINETIC Evaluation Board

Table 1 Power Supply of the EASY 334 VINETIC Evaluation Board

Voltage Level	Max Current	Use
+5 V DC laboratory supply	1.5 A	Supply for MPC module and MICO. The 1.5 A max. current value results from adding the supply currents of the +1.8 V and +3.3 V supply when created on board.
+3.3 V DC on board / laboratory supply	1 A	EASY 334 supply voltage
+1.8 V DC on board / laboratory supply	0.8 A	EASY 334 supply voltage
VBATL laboratory supply	see SLIC datasheet	Battery voltage
VBATH labatory supply	see SLIC datasheet	Battery voltage
VBATR laboratory supply	see SLIC datasheet	Battery voltage
VHR laboratory supply	see SLIC datasheet	Auxiliary supply voltage

The given values are calculated for the operation with four active channels.

The +3.3 V and +1.8 V supply voltages are generated on board and only the +3.3 V supply voltage can be fed externally! For special tests the +1.8 V supply voltage can be fed externally by a jumper. A 0R resistor has to be removed before.

The voltages +5 V, V_{BATL}, V_{BATH}, V_{BATR} and V_{HR} have always to be supplied by external power supplies.

The supply voltages are connected to the VINETIC by a 0R resistor in parallel to a jumper to measure the current. The following 14 power supply lines can be measured:

- VDD33
- VDD33A
- VDD33B
- VDD33AB
- VDD33C
- VDD33D
- VDD33CD
- VDD18
- VDD18A
- VDD18B
- VDD18AB

- VDD18C
- VDD18D
- VDD18CD

2.5 General Clocking Concept

By default the whole system clocks are generated on board via a crystal oscillator (24.576 MHz) and a CPLD. This provides a full synchronous operation of the EASY 334 VINETIC Evaluation Board.

The range of the generated PCM clock signal is 512 kHz[1)] to 8192 kHz. The clocks are selectable by software. These clock rates are derived from the 24.576 MHz clock signal generated on board by an external crystal oscillator. The stability of the clock signal is +- 30 ppm.

The 4.096 MHz MCLK signal for the VINETIC is also derived from this oscillator. Also the IOM-2 DCL (4.096 MHz) is generated from the 24.576 MHz clock oscillator. All PCM clocks are generated from one clock source (CPLD and oscillator). Thus the PCM devices (VINETIC and the MICO) are synchronous.

The PCM clock values can be selected by programming registers in the CPLD via software. If a clock value is selected the FSC will be generated automatically.

The master clock MCLK towards the VINETIC will be selectable between 256 kHz, 512 kHz and 8.192 MHz in 512 kHz steps.

A possibility is provided to connect a PCM-4 system to the evaluation board. This measurement system can be used in both slave and master mode. If the PCM-4 generates the clocks, the on board generated PCM clocks can be disabled.

1) Device is capable of 256 kHz minimum.

3 System Structure

3.1 Block and Placing Diagram

The following figure shows which components are used on the EASY 334 VINETIC Evaluation Board and gives an idea of how these parts will be placed on the evaluation board.

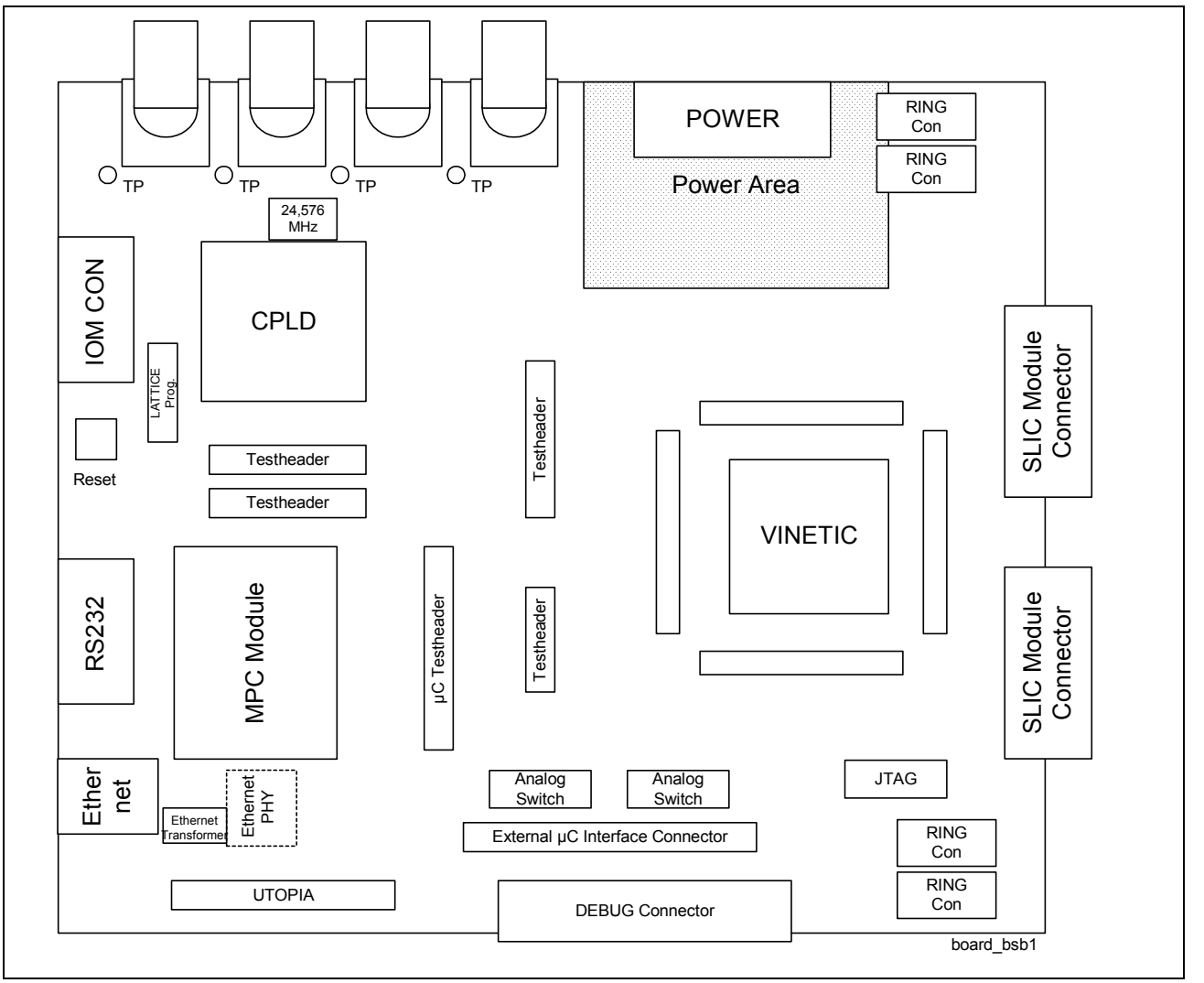


Figure 3 The Placement on the EASY 334 VINETIC Evaluation Board

3.2 Power Concept on the EASY 334 VINETIC Evaluation Board

The VINETIC Evaluation Board has several possibilities to connect the different ground planes. The feature is implemented to find out the best ground concept for the EASY 334. Several jumpers are placed on the board to connect the different grounds. In parallel a short circuit is placed of the jumper to realize a very good connection. The short

circuits are placed on the solder side of the board. The jumpers are placed on the component side of the board. **Figure 4** shows the jumpers and their function.

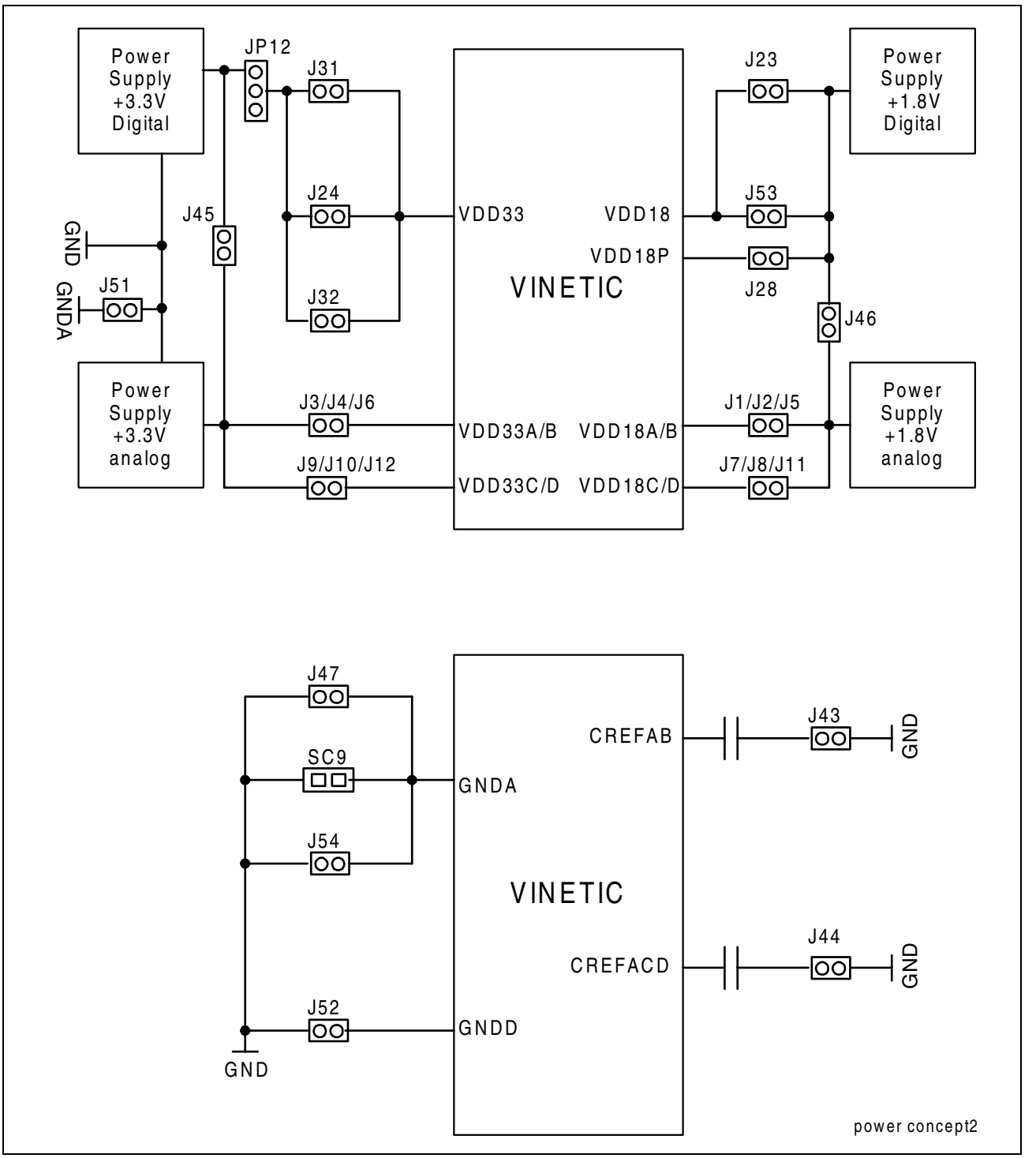


Figure 4 Power Concept and the Jumpers

Table 2 Jumpers and their Grounding Function

Jumper	Short circuit	Potential	Function
JP12	-	+3.3 V	selects the power (internal or external)
J45	SC3	+3.3 V	connect the digital and analog supply
J51	SC8	GND	connect the digital and analog GND
J31	-	+3.3 V	connect the digital supply
J24	-	+3.3 V	connect the digital supply
J53	-	+3.3 V	connect the digital supply
J47	SC5	GND	connect the digital and analog GND
J54	-	GND	connect the digital and analog GND
J52	-	GND	connect the digital and analog GND
-	SC9	GND	connect the digital and analog GND
J43	SC1	GND	CREFAB ground to digital ground
J44	SC5	GND	CREFCD ground to digital ground
J46		+1.8 V	selects the power (internal or external)
J23	-	+1.8 V	connect the digital supply
J3	-	+3.3 V	current measurement jumper of VDD33A
J4	-	+3.3 V	current measurement jumper of VDD33B
J6	-	+3.3 V	current measurement jumper of VDD33AB
J9	-	+3.3 V	current measurement jumper of VDD33C
J10	-	+3.3 V	current measurement jumper of VDD33D
J12	-	+3.3 V	current measurement jumper of VDD33CD
J1	-	+1.8 V	current measurement jumper of VDD18A
J2		+1.8 V	current measurement jumper of VDD18B
J5		+1.8 V	current measurement jumper of VDD18AB
J7		+1.8 V	current measurement jumper of VDD18C
J8		+1.8 V	current measurement jumper of VDD18D
J11		+1.8 V	current measurement jumper of VDD18CD

The default jumper setting is:

J45, J47, J43, J44, J46

J45 and J46 only closed, when 2 voltage regulators are soldered on the board

4 Interfaces

The EASY 334 VINETIC Evaluation Board allows to run the VINETIC in the following interface modes.

- 8bit INTEL demultiplexed + PCM
- 8bit INTEL multiplexed + PCM
- 16bit INTEL demultiplexed + PCM
- 16bit INTEL multiplexed + PCM
- 8bit MOTOROLA + PCM
- 16bit MOTOROLA + PCM
- 8bit HPI + PCM
- 16bit HPI + PCM
- IOM-2 (2.048MHz)
- IOM-2 (1.536MHz)
- IOM-2 (4.096MHz)
- SPI + PCM
- SCI +PCM

As the CPU module carries a MOTOROLA processor, the default µC mode on the EASY 334 VINETIC Evaluation Board is the Motorola Mode. All devices will be accessed in this mode. Only the VINETIC will be accessed in the different µC modes, that are listed above. The bus mode is selected by setting the corresponding bit in the CPLD registers.

To configure the VINETIC to one of the modes above, pin strapping options are used, These pin strapping options are realized by user programmable registers located in the CPLD. For further information about the registers see **Chapter 5.2**. No jumper is provided to configure the EASY 334 and it's interfaces to the different modes.

To implement a different µC access to the VINETIC, the external µC interface connector will be used, while, on the other side, the MPC will be connected only to the CPLD. These two possible configurations shows **Figure 5**.

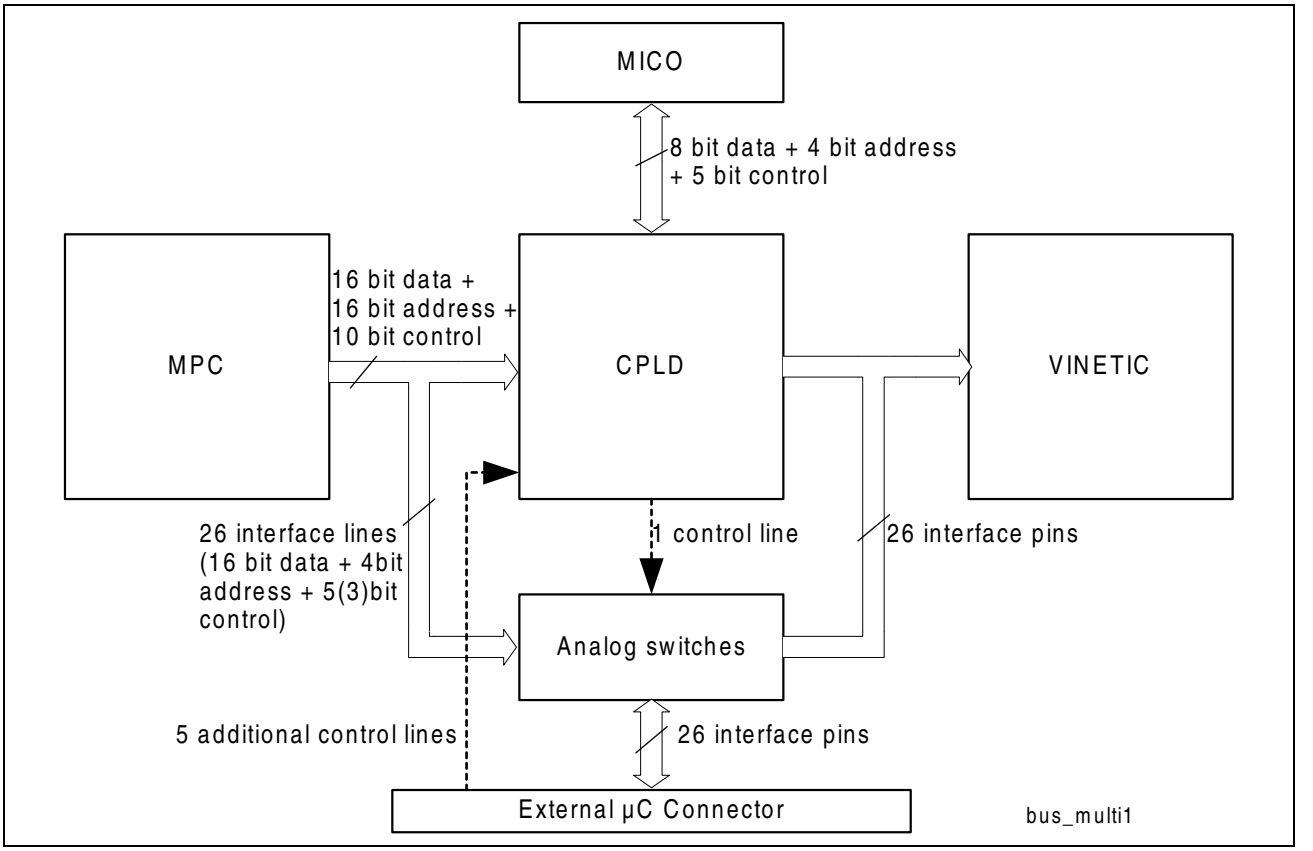


Figure 5 µC Interface Structure on the EASY 334 VINETIC Evaluation Board

If the µC bus is connected to the CPLD then it is possible to emulate an Infineon/INTEL multiplexed or demultiplexed bus mode in the CPLD. The bus size towards the VINETIC device (if 8bit or 16bit are used) depends on the chosen bus size from the MPC. The HPI interface will not be emulated in the CPLD.

To operate the VINETIC with an HPI interface mode, the µC interface has to be connected to the external bus connector. In this case it is possible to use a special configured test equipment in which the HPI interface can be directly used over a special interface connector.

All interfaces that are connected to port pins of the MPC have to be initialized as described in the following subchapters. On the VINETIC Evaluation Board no UTOPIA interface is provided. But if the interface settings are done like described in the following chapters the use of an UTOPIA interface in the future is possible.

4.1 INFINEON/INTEL Bus Mode

The Infineon/INTEL multiplexed and demultiplexed bus mode will be emulated by the CPLD.

If a bus mode is emulated by the CLPD, this feature will not be provided in the principle code versions to put the board into operation. The dedicated code version will be delivered when the default operations (default bus mode is Motorola Mode) are verified.

The VINETIC runs by default in the Motorola mode after board reset.

If a real INFINEON/INTEL bus timing shall be tested, it's possible to disconnect the VINETIC from the MPC µC interface and connect it to the external µC connector. In this way an additional board carrying an INFINEON/INTEL microcontroller can be used to control the VINETIC. It is then not possible to control the whole EASY 334 VINETIC Evaluation Board by the external microcontroller.

The used bus size depends on which width is selected by an access using the MPC to the VINETIC and set in the VMODE register of the CPLD. The CPLD is always running in Motorola 8 Bit Mode.

4.2 MOTOROLA Bus Mode

The Motorola bus mode is the standard µC mode in the EASY 334 VINETIC Evaluation Board. After every reset, the VINETIC operates in the Motorola mode by default.

The default bus size that is used after reset is the 16bit mode.

If the 8bit mode should be used, the CPLD has to provide a bit shift on the address lines towards the EASY 334. By operating the EASY 334 in that bus mode, all control and address signals have to be buffered in the CPLD.

Only the 16bit mode can be run without buffering any µC interface relevant signals.

4.3 External µC Interface

The µC interface of the VINETIC is connected to a external µC connector to support all µC interfaces without the MPC Module or these modes, which are not testable by the MPC and the CPLD logic.

4.4 IOM-2 Mode

In IOM-2 mode the parallel µC interface is not available.

When the EASY 334 VINETIC Evaluation Board is used in IOM-2 mode two different configurations for IOM-2 mode are available.

For handling IOM-2 on the EASY 334 VINETIC Evaluation Board, the MICO is placed on the Evaluation Board.

It is also possible to connect an external IOM2 master to the EASY 334 VINETIC Evaluation Board.

The IOM-2 interface is not connected to the MPC module.

The external master has to be connected to the BNC-jacks located on the board or to the IOM-2 connector (DSUB-9) located on the board.

By default the MICO is the IOM-2 master. The IOM-2 signals are connected from the IOM-2 master to the VINETIC. This includes the FSC, DCL, DU and DD signal. The clock signals have to be provided. All actions regarding the IOM-2 interface (master selection) require that the IOM-2 mode for the VINETIC is selected.

When the MICO is selected for IOM-2 programming of the VINETIC, the IOM-2 DCL is generated on the EASY 334 VINETIC Evaluation Board. When an external IOM-2 master is connected to the board, the DCL and the FSC clock signal have to be provided external. In this case the MICO has to be held in reset state.

No AC termination is provided on the IOM-2 connector.

The PEF2015 (MICO) can be accessed only in Motorola bus mode. To enable the clocks for the MICO, the bit MRES in CMDREG1 has to be set to ’1’. When the MICO is activated (IOM-2 mode of VINETIC CMDREG2:VMODE="1111"), the clock relations are set as defined in CMDREG3:CLOCK. If the MICO is used, the PCM clock and the CFI clocks (IOM-2 of VINETIC) are identical.

All MICO clocks are synchronous and are derived from the same clock (24.576 MHz). The PFS and the FSC signals of the MICO are connected together and are also connected to the FSC signal of the EASY 334. The timing relations for PCM clocking and IOM-2 clocking are fixed and cannot be changed. The MICO can be clocked from the crystal oscillator located on board.

4.5 PCM Mode

PCM Mode for the VINETIC is set with the CMDREG2:VMODE during the reset signal is hold active (bit CMDREG1:VRES=’0’).

When the EASY 334 is used in PCM mode two different configurations for PCM mode (regarding to the PCM master) are available.

When the EASY 334 is used with PCM mode the MICO has to be set into reset state.

The default board setup for the VINETIC is the PCM master mode. The clocks (FSC and PCLK) are generated on board. Both clocks are derived from the 24.576 MHz clock and are synchronous to the MCLK clock signal of the VINETIC.

It is also possible to connect an external PCM source (PCM4) to the EASY 334 VINETIC Evaluation Board. The external PCM source has to be connected to the BNC-jacks located on the board or to the IOM-2 connector (DSUB-9) located on the board. The selection of the PCM source is done by the register bits CMDREG3:IOMen and S/Mn. The FSC and the PCLK are synchronous to the MCLK of the EASY 334. The FSC/DCL

and MCLK is generated on the Evaluation Board by the clock generator or the FSC/DCL is delivered in the Slave Mode. In the Slave mode the MCLK is identically to the DCL. The same modes are possible with the PCM interface. In these cases the MCLK is identically to the PCLK. Following clock mode settings are selectable via register:

- PCLK=8.192 MHz
- PCLK=4.096 MHz
- PCLK=3.072 MHz
- PCLK=2.048 MHz
- PCLK=1.536 MHz
- PCLK=1.024 MHz
- PCLK=512 kHz

4.6 PCM Interface Connector

The PCM interface is connected to 4 BNC jacks on the PCM side of the board.

The PCM signals are buffered with a LS type buffer to be able to drive 50 Ohm loads. The PCM4 interface can be used in two different modes regarding the clock generation and driving capability.

- Master mode: All PCM clocks are generated on the EASY 334 VINETIC Evaluation Board, PCLK, FSC and MCLK of VINETIC are synchronous. All clocks are derived from the same crystal oscillator (24.576 MHz). The clocks and the upstream signal is buffered by the LS buffer.
- Slave mode 1: All clocks for the VINETIC are delivered from external. The IOM-2 or PCM clock DCL/PCLK and FSC/PFS are delivered to the board. In these modes the MCLK is used by the IOM-2 or PCM clock PCLK (or DCL).

4.7 SLIC Module Interface

The EASY 334 VINETIC Evaluation Board has two identical module interfaces to connect to the SLIC modules.

Besides the analog signals all necessary supply voltages are provided on both connectors.

4.8 JTAG Emulation Port

The VINETIC has an implemented JTAG port for debug purposes. The JTAG interface can be accessed by a PC parallel port connection via adapter cable. All signals from the parallel port connection will be buffered by logic at the adapter cable to provide a +3.3 V signal level towards the EASY 334. For other tests the VINETIC pins TEST and TRSTQ are connected to a separate header.

4.9 Ethernet Link

The Ethernet port on the Main Board is compatible to the TQC Starter Kit. The pinout of the connector is shown in **Chapter 6.6**. The SCC1 of the MPC has to be initialized for Ethernet access.

4.10 RS232 Debug Link

This RS232 port is used to output messages. It is compatible to the TQC Starter Kit. The reset line is not supported. The pinout of the connector is shown in **Chapter 6.5**.

4.11 BDM Interface

The BDM port interfaces to a Lauterbach MPC-debugger. It is compatible to the TQC Starter Kit. The pinout of the BDM connector is shown in **Chapter 6.8**.

4.12 SCC2 and UTOPIA Interface of MPC

The both interfaces SCC2 and UTOPIA of the MPC Module are reserved for future use. These signals are not used at this Evaluation Board. Therefore, it is possible to redesign the board without to change the signal and to modifiy the software later on. E.g. the SCC2 is used to connect the PCM interface of the VINETIC with the PCM interface of the MPC.

4.13 CPLD Programming interface

The connector for programming the Lattice CPLD is provided on the EASY 334 VINETIC Evaluation Board.

4.14 Test Pins

Following test pins will be provided:

- GND pins;
- PCM-Highway (Highway A and B), direct on the VINETIC (8tp);
- MICO clock and control signals (14pin header);
- 8 unused output pins from the CPLD, for debugging purposes;
- Test header of all VINETIC pins arranged in the same pinning as the chip (same number as pins);
- MPC data, address, control signals (54pin header)

5 Board Control

5.1 Reset Logic

The software reset for the EASY 334 and the MICO are realized by register bits on board. The registers are placed in the CPLD and accessed via software.

Following reset sources are logically "ored" into the resulting reset provided to the EASY 334 VINETIC Evaluation Board components:

- onboard power on reset (active low, MAX708RCSA used)

The reset-controller MAX708RCSA checks the supply voltages (+5 V, +3.3 V). The +3.3 V supply voltage can be optionally generated from the +5 V supply.

- reset button (active low), the reset button is debounced

On-board power-on reset and the reset button appear on the same reset signal. The reset signal will be set active for a time duration of approx. 200ms when the reset button is pressed or the board is connected to power first time. Also when the monitored supply voltages (+3.3 V and +5 V) are below the threshold voltage of the reset controller device, the reset will be set active until the voltages are above threshold level.

- reset set by on-board software register

- CMDREG1:VRES: (active high) controls the reset signal (low active) for VINETIC
- CMDREG1:MRES: (active high) reset signal for MICO
- CMDREG1:IOMRES: (active high) reset signal for IOM2-Connector

5.2 CPLD Logic

The logic supports the on board configuration registers and the clock generator. Also the mode settings of the MICO and VINETIC are set. Additional function is the emulation of the Intel demultiplexed and/or multiplexed mode for the VINETIC. The emulation is automatically started, when these modes are selected for the VINETIC. The default mode is the Motorola demultiplexed mode. The MICO and the CMDREGs are always running in the Motorola mode.

The logic is placed into a CPLD from Lattice. The type is the ispLSI5128.

Attention: The address bus between MPC and Vinetic is always shifted by 1, because the MPC can not read or write in 16 bit mode at A0 = '1'.

MPC A1 = > VINETIC A0

5.2.1 Clocking Concept

All clocks are delivered from external or are generated on-board by the clock generator. The clock generator has a clock input frequency of 24.576 MHz. The clock frequency is

set to the frequency selected in CMDREG3 and fed to the MICO PCM- and CFI-interface. In the IOM-2 interface mode the MICO is enabled (reset disabled) and initialized. In all other modes of the VINETIC the MICO is disabled and the MICO inputs are tristate. In addition and for future use the PCM clocks and CFI-clocks are delivered at different IOs of the CPLD. If the internal clock generator is not used, the clock outputs for the PCM- and IOM-2 interface is in the tristate mode. The clocks can be fed via the BNC plugs or via the IOM-2 Service Access Connector (D-Sub 9 pole).

5.2.2 Signals on the CPLD

The CPLD generates the necessary signals for the onboard devices. The VHDL code for this logic is provided in the Appendix.

The nomenclature for signal names in the following tables is as follows:

iXXXsignal is an input

oXXXsignal is an output

bXXXsignal is an bidirectional In and output

The following table gives an overview of the signals connected to this chip.

Table 3 Signals on the CPLD

Logic Block	Signal Name	Function
MPC Block	iMA[7..0]	Address lines of the MPC
	bMD[15..0]	Data lines of the MPC
	iDSn	Data strobe of the MPC
	iRWn	Read-write not Signal
	iWE0n	write signal lower byte
	iWE1n	write signal upper byte
	iALE	Address latch enable
	iCS1n	chip select signal
	iCS5n	chip select signal
	iCS6n	chip select signal
	bSCC2	Serial Comunication Controller Interface 2
External µC interface	iVMODE[3..0]	VINETIC Mode selection by ext. µC connector
	iSTANDA	Standalone mode activation

Table 3 Signals on the CPLD (cont'd)

Logic Block	Signal Name	Function
MICO	oMIA[3..0]	address lines to MICO
	bMID[7..0]	data lines to MICO
	oMIWRn	write signal to MICO
	oMIRDQ	read signal to MICO
	oMCSn	chip select signal to MICO
VINETIC µC interface	oVA[3..0]	Address lines to VINETIC
	bVD[15..0]	data lines to VINETIC
	oVALE	Address latch for VINETIC
	oVWRn	Write signal to VINETIC
	oVRDn	Read Signal to VINETIC
	oVCSn	chip select signal to VINETIC
	oFSEL[3..0]	Mode Selection of the VINETIC
Reset Block	iRESn	Board and power-on RESET
	oMRES	MICO Reset
	oVRES	VINETIC Reset
	oICRES	IOM-2 Connector Reset
Clock Generator	iCLK	Oscillator Clock of 24.576 MHz
	oPFS	8 kHz PCM Frame for MICO
	oPCLK	PCM data clock for MICO
	oFSC	8 kHz frame for IOM-2 or PCM-interface of VINETEC
	oDCL	data clock for IOM-2 or PCM-interface of VINETEC
Status	oLED[7..0]	Status LEDs output
SLIC ID	SLAID[3..0]	SLIC Module A Identification input
	SLBID[3..0}	SLIC Module B Identifcation input

5.2.3 CPLD Registers Setup

This section describes the registers located in the CPLD. For the register descriptions of the other on-board devices (VINETIC and MICO) please refer to the specific data sheets and User's Manual for these devices.

5.2.4 Version Controlling

Located at Address 0xFA (hex) a version register is provided. After reset the version of the CPLD can be read from this address. The version for the CPLD on the EASY 334 VINETIC Evaluation Board will start with the number 0x64(hex) = 100 (dezimal). This is equal to the version number of the board. When a redesign of the board appears and the version changes to e.g. V1.2 then the version numbers of the CPLD will start at 0x78(hex) = 120(dezimal.). Thus 10 different released CPLD versions are possible for each board version.

5.2.5 Command Register 1 (CMDREG1)

Base Address: FE_H

Command Register 1

CMDREG1
Command Register 1 **($XXFE_H$)** **Reset Value: 00_H**

7	6	5	4	3	2	1	0
MUX			0	0	IOMRES	MRES	VRES
rw	rw		rw			rw	rw

Field	Bits	Type	Description
MUX	[7:5]	rw	**Control Bits for analog multiplexer (Linetest support)** 000 Voltage on RING Channel B is measured 001 VBATH is measured 010 VBATL is measured 011 VBATR is measured 100 VHR is measured 101 GND is measured 110 TIP-RING potential difference is measured 111 VCMS is measured
IOMRES	2	rw	**IOM Connector Reset** 0 Reset is active 1 Reset is disabled
MRES	1	rw	**MICO Reset** 0 Reset is active 1 Reset is not active

Field	Bits	Type	Description
VRES	0	rw	**VINETIC Reset** 0 VINETIC Reset is active 1 VINETIC Reset is not active

5.2.6 Command Register 2 (CMDREG2)

Base Address: FD_H

Command Register 2

CMDREG2
Command Register 2 **($XXFD_H$)** **Reset Value: $0C_H$**

7	6	5	4	3	2	1	0
PCMBK	**PCMHW**	**MPCBYP**	**MCSW**	**VMODE**			
rw	rw			rw		rw	rw

Field	Bits	Type	Description
PCMBK	7	rw	**PCM Loop Activation** 0 No loop activated 1 DRA connected to DXB and DRB connected to DXA
PCMHW	6	rw	**Selection on PCM highways for measurement** 0 PCM highway A selected for measurement PCM highway B connected to MPC 1 PCM highway B selected for measurement PCM highway Aconnected to MPC
MPCBYP	5	rw	**Microcontroller Interface Bypass** 0 Microcontroller interface of VINETIC is connected via CPLD 1 Microcontroller interface is connected directly between MPC and VINETIC
MCSW	4	rw	**µC Interface Switch Selection** 0 VINETIC is connected to the Motorola Bus (via CPLD) 1 VINETIC is connected to the µC Interface connector

Field	Bits	Type	Description
VMODE	[3:0]	rw	**VINETIC Interface Mode Selection** 1100 16 Bit Motorola Mode + PCM 0100 8 Bit Motorola Mode + PCM 1011 16 Bit Intel Demultiplexed Mode + PCM 0011 8 Bit Intel Demultiplexed Mode + PCM 1010 16 Bit Intel Multiplexed Mode + PCM 0010 8 Bit Intel Multiplexed Mode + PCM 1101 16 Bit HPI + PCM 0101 8 Bit HPI + PCM 0000 SPI + PCM 0001 SCI + PCM 1111 IOM-2

5.2.7 Command Register 3 (CMDREG3)

Base Address: FC_H

Command Register 3

CMDREG3
Command Register 3 **($XXFC_H$)** **Reset Value: 00_H**

7	6	5	4	3	2	1	0
MCLKen	**0**	**IOMen**	**S/Mn**	**CLOCK**			
rw	rw			rw		rw	rw

Field	Bits	Type	Description
MCLKen	7	rw	**Master Clock Selection enable** 0 MCLK = DCL 1 MCLK is selected in CMDREG5
IOMen	5	rw	**IOM-2 Connector is clock output** 0 IOM-2 Connector is clock input 1 IOM-2 Connector is clock output
S/Mn	4	rw	**Clock Slave / Master Selection** 0 Board is in slave mode (all clocks have to be delivered) 1 Board is in master mode (all clocks are generated on board)

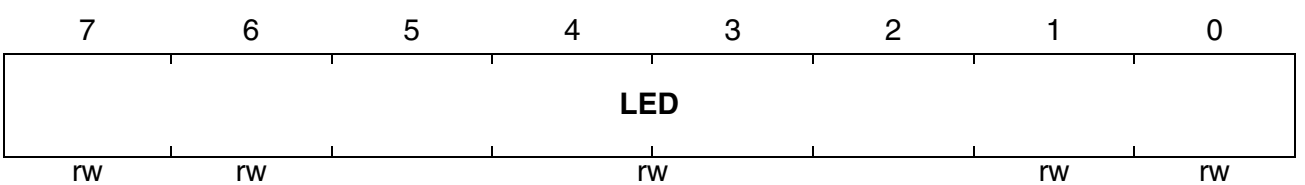
Field	Bits	Type	Description
CLOCK	[3:0]	rw	**Clock Generator Selection for VINETIC and MICO (when enabled)** PCLK = DCL = PDC PFS = FSC 0000 4.096 MHz 8 kHz 0001 2.048 MHz 8 kHz 0010 1.536 MHz 8 kHz 0011 8.192 MHz 8 kHz 0100 3.072 MHz 8 kHz 0101 1.024 MHz 8 kHz 0110 512 kHz 8 kHz 0111 reserved reserved 1xxx reserved reserved

5.2.8 Command Register 4 (CMDREG4)

Base Address: FB_H

Command Register 4

CMDREG4
Command Register 4 ($XXFB_H$) Reset Value: 00_H



Field	Bits	Type	Description
LED	[7:0]	rw	**LED** 0 LED is off 1 LED is on

5.2.9 Command Register 5 (CMDREG5)

Base Address: $F8_H$

Command Register 5

CMDREG5
Command Register 5 ($XXF8_H$) Reset Value: 00_H

7	6	5	4	3	2	1	0
MCLK			0	0	0	0	0
rw	rw		rw			rw	rw

Field	Bits	Type	Description
MCLK	[7:5]	rw	**Master Clock Selection** 000 MCLK = 4.096 MHz 001 MCLK = 2.048 MHz 010 MCLK = 1.536 MHz 011 MCLK = 8.192 MHz 100 MCLK = 3.072 MHz 101 MCLK = 1.024 MHz 110 MCLK = 512 kHz 111 MCLK = 256 kHz

5.2.10 Version Register (VersionREG)

Base Address: FA_H

Version Register

VersionREG
Version Register ($XXFA_H$) Reset Value: 26_H

7	6	5	4	3	2	1	0
0	0	1	0	0	1	1	0
rw	rw		rw			rw	rw

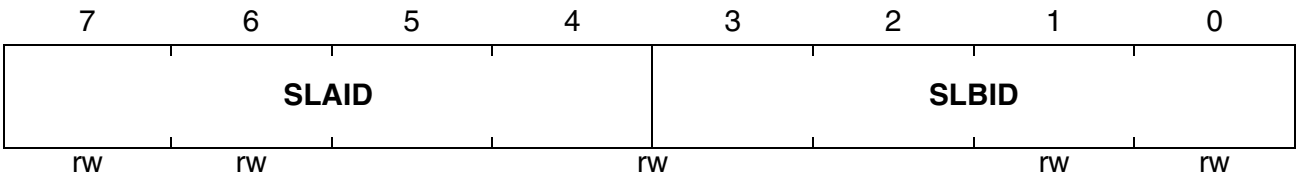
The version register contains the value 0x26h for the first version.

5.2.11 SLIC Identification Register (SLIDREG)

Base Address: $F9_H$

SLIC Identification Register

SLIDREG
SLIC Identification Register ($XXF9_H$) Reset Value: $FF^{1)}_H$



1) Reset value only correct when no SLIC Board is connected

Field	Bits	Type	Description
SLAID	[7:4]	r	**SLIC Module A Identification Byte** 0000 SMART4265 V1.1 Board is connected (SLIC E/S/P) 0001 SMART4365 V1.1 Board is connected (T-SLIC) 1000 GEMINAX-VINETIC Board is connected rest reserved
SLBID	[3:0]	r	**SLIC Module B Identification Byte** 0000 SMART4265 V1.1 Board is connected (SLIC E/S/P) 0001 SMART4365 V1.1 Board is connected (T-SLIC) 1000 GEMINAX-VINETIC Board is connected rest reserved

5.3 Memory Addressing the On-Board Devices

5.3.1 CPLD Addressing

The CPLD is addressed via memory mapping by the MPC. The chipselect line MCS6n is used to access the CPLD. The setup of the MPC register is as follows.

Base Address: 0xC0010000

Base Register: 0x0801

Option Register:0xFF4F8784

5.3.2 VINETIC Addressing

The VINETIC is addressed via memory mapping by the MPC. The chipselect line MCS7n is used to access the VINETIC. The setup of the MPC register is as follows.

Base Address: 0xC0020000

Base Register: 0x0801

Option Register: 0xFF4F8F34

5.3.3 MICO Addressing

The MICO is addressed via memory mapping by the MPC. The chipselect line MCS5n is used to access the MICO. The setup of the MPC register is as follows.

Base Address: 0xC0030000

Base Register: 0x0801

Option Register: 0xFFFF8F34

5.3.4 Register Addressing

The registers for board configuration are also addressed via memory mapping

Table 4 Register Offset and Address Range

Register	Offset	Range	Function
CMDREG1	FEh	FEh	Read/Write
CMDREG2	FDh	FDh	Read/Write
CMDREG3	FCh	FCh	Read/Write
CMDREG4	FBh	FBh	Read/Write
CMDREG5	F8h	F8h	Read/Write
VersionREG	FAh	FAh	Read
SLIDREG	F9h	F9h	Read

5.3.5 Interrupts

Up to 2 on-board devices are able to generate interrupt requests to the micro controller. The following table shows the sources and how they can be handled by the MPC module.

Table 5 Interrupt Table

Interrupt Signal	Function
MIRQ7n	MICO
MIRQ6n	VINETIC
MIRQ5n	VINETIC READY signal
MIRQ4n	not used
MIRQ3n	not used
MIRQ2n	not used
MIRQ1n	not used
MIRQ0n	Pulled up, NMI (not used)

6 Pinout Descriptions

6.1 DC-Power Supply Connector (ST12)

The power supply connector provides all voltages to the board. The +3.3 V supply can be selected from the supply connector or from the on-board voltage regulator. The selection is done by jumper JP12. The +3.3 V is generated on-board from +5 V using a voltage regulator CT1086. The maximum current is 1.0 A from this device.

The +5 V power supply can be used only from the external power supply. The maximum current is 1.5 A.

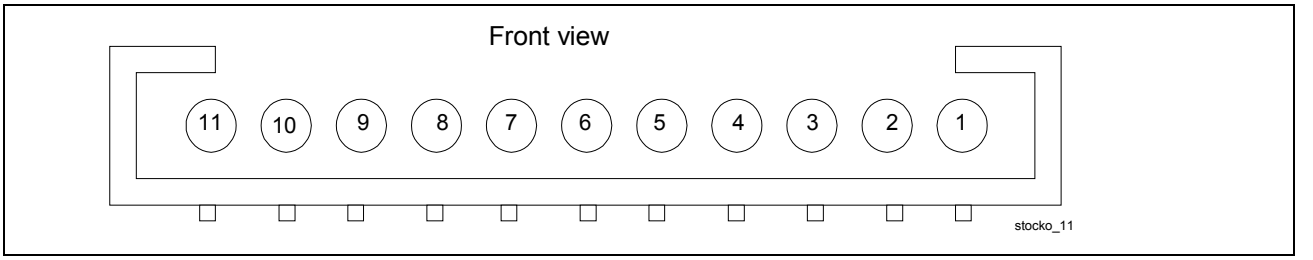


Figure 6 Power Supply Connector ST12

Table 6 Pin Description ST12

Pin	Voltage
1	+5 V (VCC)
2	GND
3	+3.3 V (V3V3)
4	GND
5	VHR
6	GND
7	VBATL
8	GND
9	VBATH
10	GND
11	VBATR

6.2 SLIC Connector (ST6 and ST7)

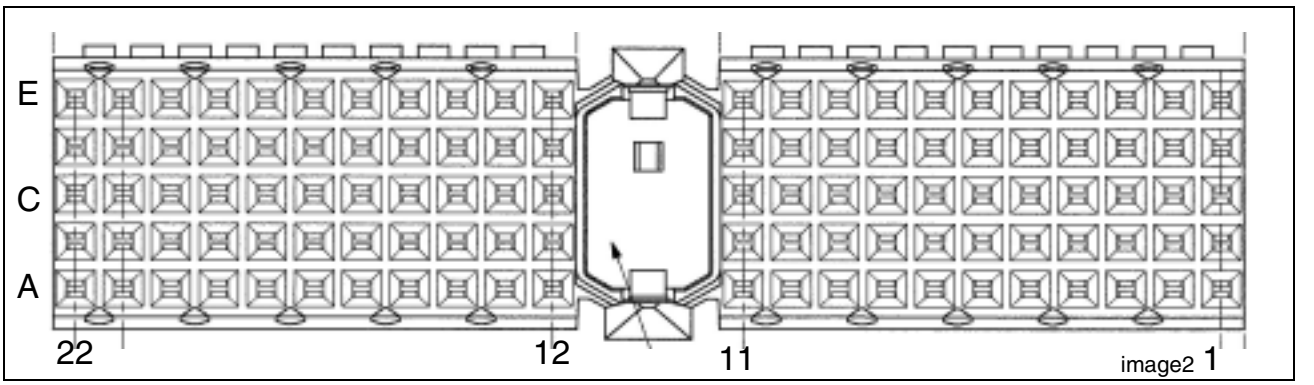


Figure 7 SLIC Connector ST6 and ST7 (Front View)

Table 7 SLIC Connector ST6 and ST7

Pin	Row A	Row B	Row C	Row D	Row E
1	TEST1	GND	ITACB	GND	GND
2	RINGCHB	IO2B	GND	GND	ILB
3	ANALOG2B	IO1B	ITB	GND	C1B
4	TEST2	GND	GND	C3B	C2B
5	IO3B	GND	DCPB	GND	DCNB
6	VCM	GND	ACNB	GND	ACPB
7	IO4B	VCMITB	GND	VCMSB	GND
8	n.c.	n.c.	n.c.	n.c.	n.c.
9	VCC	V3V3	VHR	VHR	VHR
10	VCC	V3V3	VBATH	VBATH	VBATH
11	VCC	V3V3	VBATL	VBATL	VBATL
12	+1.8 V	+1.8 V	VBATR	VBATR	VBATR
13	+1.8 V	ID0	ID1	ID2	ID3
14	GPIO0[1)]	GPIO1[1)]	GPIO2[1)]	GPIO3[1)]	n.c.
15	n.c.	n.c.	n.c.	n.c.	n.c.
16	n.c.	GND	ITACA	GND	GND
17	ANALOG1A	IO2A	GND	GND	ILA
18	ANALOG2A	IO1A	ITA	GND	C1A
19	n.c.	GND	GND	C3A	C2A
20	IO3A	GND	DCPA	GND	DCNA

Table 7 SLIC Connector ST6 and ST7 (cont'd)

21	n.c.	GND	ACNA	GND	ACPA
22	IO4A	VCMITA	GND	VCMSA	GND

[1] GPIO0..GPIO3 at5 SLIC Connector 1 for channel A and B. GPIO4..GPIO7 at SLIC Connector 2 for channel C and D. Additional GPIO0..GPIO7 connected to LEDs (D26..D33) in parallel.

n.c. not connected

6.3 External Ring Connector ST8, ST9, ST10 and ST11

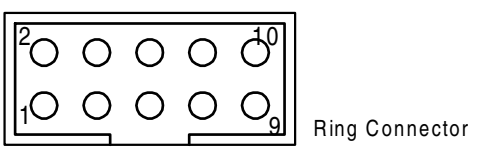


Figure 8 External Ring Connector ST8, ST9, ST10 and ST11

Table 8 Pin-out of the External Ring Connector

Pin	Use	Signal	Description
1	I	IO2A/C/D	Ring Voltage (RINGTRIP for channel B)
2	O	RECON1/2/3/4	relay driver output
3	O	VCC	+5 V
4	I	RSYNC	RSYNC pin of VINETIC
5	O	V3V3	+3.3 V
6	-	n.c.	-
7	O	VCMAB/CD	signal VCM of VINETIC
8	-	n.c.	
9	-	n.c.	
10	O	GND	

6.4 Lattice Programming Interface Connector ST5

The Programming Interface Connector is only used to program the Lattice device by Infineon Technologies.

6.5 External µC Interface Connector (JP7)

The external µC Interface connector is a male type with a grid of 2.54 mm.

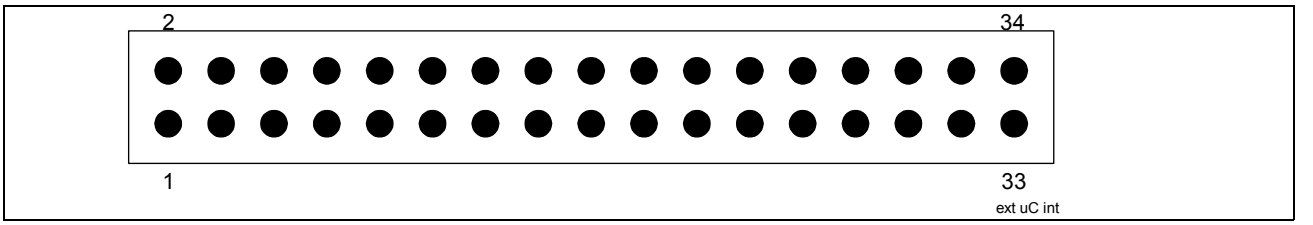


Figure 9 External µC Interface Connector JP7 (Top View)

Table 9 Pin-out of the External µC Interface Connector (JP7)

Pin	Use	Function		Pin	Use	Function
1	I/O	GND		2	I/O	GND
3	I	IFC0 (VINFC0)		4	I/O	IFAD0 (VINAD0)
5	I	IFC1 (VINFC1)		6	I/O	IFAD1 (VINAD1)
7	I	IFC2 (VINFC2)		8	I/O	IFAD2 (VINAD2)
9	I	IFC3 (VINFC3)		10	I/O	IFAD3 (VINAD3)
11	I	IFC4 (VINFC4)		12	I/O	IFAD4 (VINAD4)
13	I	IFC5 (VINFC5)		14	I/O	IFAD5 (VINAD5)
15	I	IFC6 (VINFC6)		16	I/O	IFAD6 (VINAD6)
17	I	IFC7 (VINFC7)		18	I/O	IFAD7 (VINAD7)
19	O	IFC8 (VINFC8)		20	I/O	IFAD8 (VINAD8)
21	O	+3.3 V		22	I/O	IFAD9 (VINAD9)
23	O	+3.3V		24	I/O	IFAD10 (VINAD10)
25	I	VMODE0		26	I/O	IFAD11 (VINAD11)
27	I	VMODE1		28	I/O	IFAD12 (VINAD12)
29	I	VMODE2		30	I/O	IFAD13 (VINAD13)
31		VMODE3		32	I/O	IFAD14 (VINAD14)
33		Interrupt VINETIC (VININTn)[1)]		34	I/O	IFAD15 (VINAD15)

1) Label error: The label on the board is GND.

The Mode of the VINETIC interface is latched at VMODE[3..0], when the VINETIC reset is inactive.

6.6 Debug Interface Connector ST14

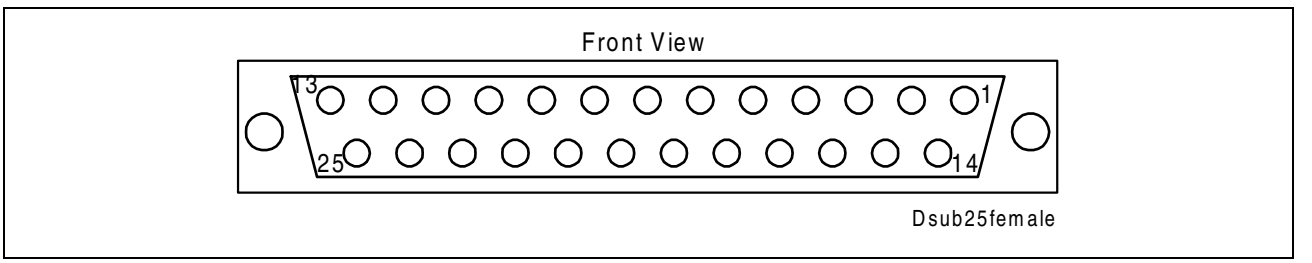


Figure 10 Debug Interface Connector ST14

Table 10 Pin-out of the Debug Connector ST14

Pin	Use	Signal	VINETIC Pin	Description
1	-	n.c.	-	-
2	I	TDI	TDI/TM0	JTAG data input
3	I	TMS	TMS/TM1	JTAG Testmode select input
4	I	TCK	TCK/TM2	JTAG Testmode clock input
5	I	TDRS	TDRS	JTAG Reset input
6	O	Pull-down	-	-
7	O	Pull-up	-	-
8	-	n.c.		
9	-	n.c.		
10	O	Pull-down		
11	-	n.c.		
12	O	TDO	TDO/TM3	JTAG Testmode output
13	-	n.c.	-	-
14	-	n.c.	-	-
15	-	n.c.	-	-
16	-	n.c.	-	-
17	-	n.c.	-	-
18	I/O	GND	-	-
19	I/O	GND	-	-
20	I/O	GND	-	-
21	I/O	GND	-	-
22	I/O	GND	-	-

Table 10 Pin-out of the Debug Connector ST14 (cont'd)

Pin	Use	Signal	VINETIC Pin	Description
23	I/O	GND	-	-
24	I/O	GND	-	-
25	I/O	GND	-	-

The debug interface is connected to the JTAG interface of the EASY 334. A driver SN74LVT245B is placed between chip and connector to shift the levels of the JTAG signals. The driver is enabled by J50 (position 2-3).The jumper J42 has to be set in position 1-2 to enable the test modes of the EASY 334.

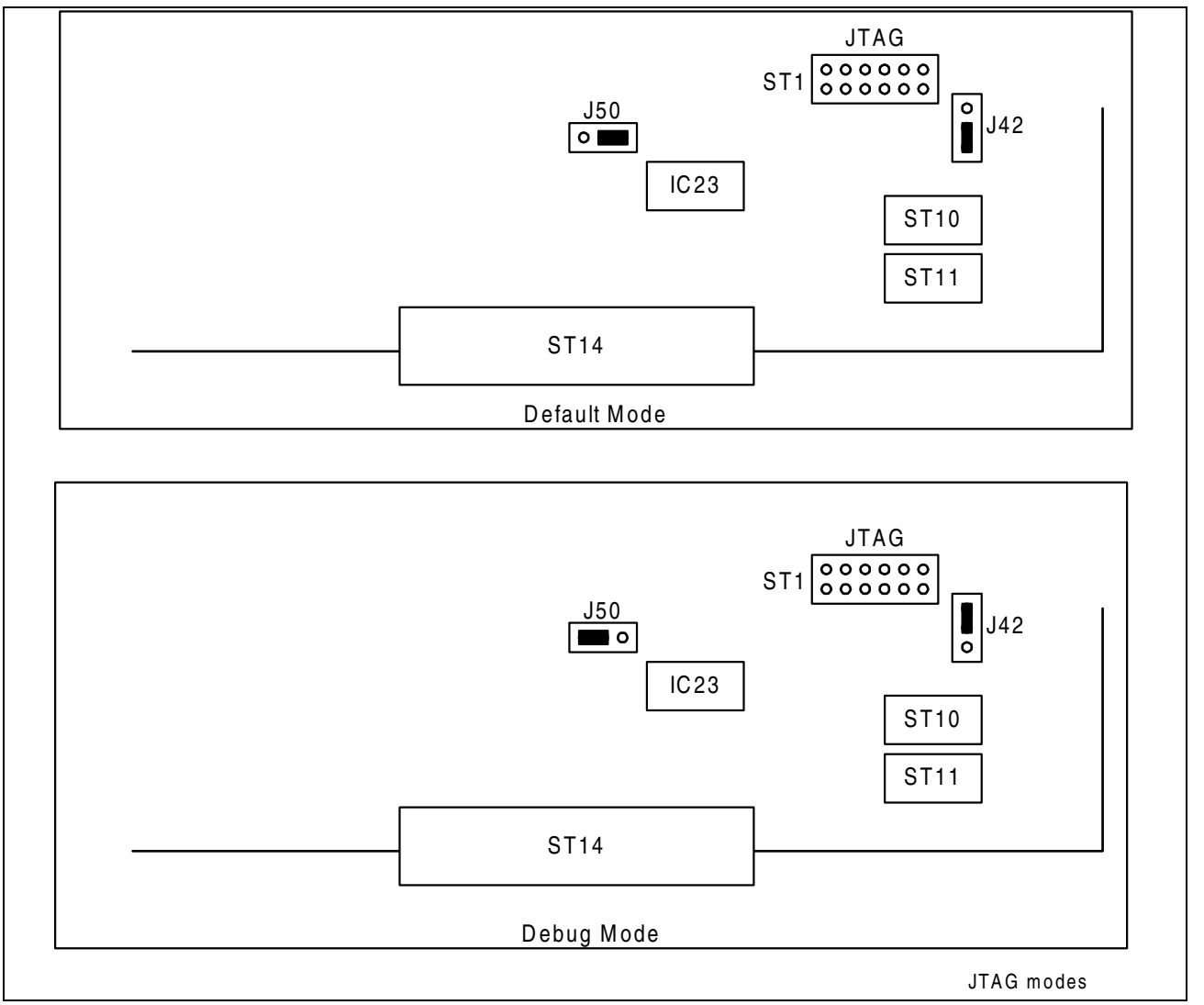


Figure 11 Jumper Setting for JTAG Modes

6.7 MPC Module Connectors

The MPC Module is delivered by TQ Components.

The dimensions are described in the next figure. The pin-out is described in the next two tables.

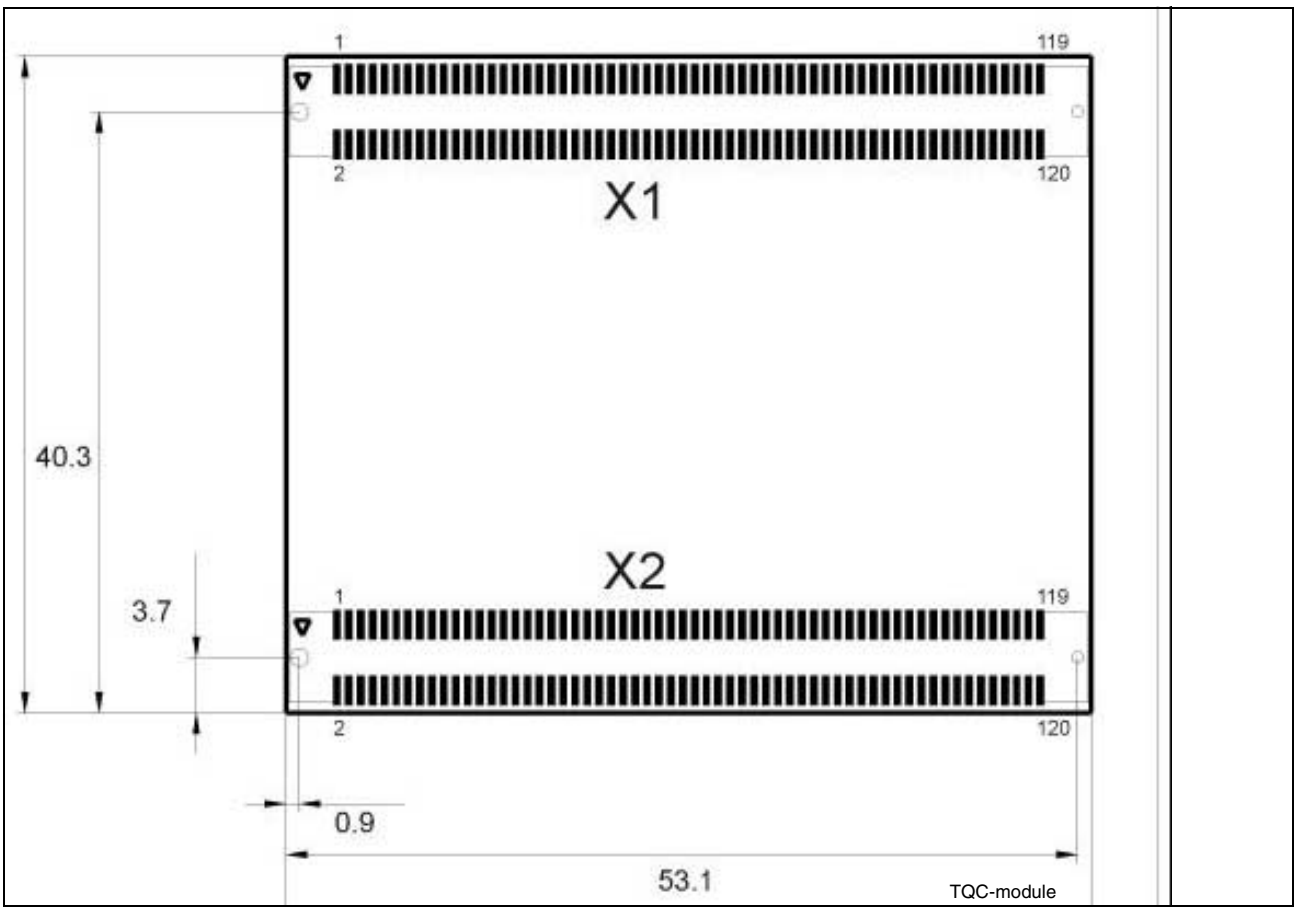


Figure 12 Dimensions of the MPC Module (Top View)

Table 11 Pin-out of the Connector X1 of the MPC Module

Pin	Use	Function		Pin	Use	Function
1	I/O	GND		2	I	IRQ0n (ext. Pull-up)
3	I	IRQ1n (ext. Pull-up)		4	I	res. (IRQ2n) (ext. Pull-up)
5	I	IRQ3n (ext. Pull-up)		6	I	IRQ4n (ext. Pull-up)
7	I	IRQ5n		8	I	IRQ6n
9	I	IRQ7n		10	I	RXSOC
11	O	ALE_A (not used)		12	I	RxDATA0
13	I	RxDATA1		14	I	RxDATA2
15	I	RxDATA3		16	I	RxDATA4
17	I	RxDATA5		18	I	RxDATA6

Table 11 Pin-out of the Connector X1 of the MPC Module (cont'd)

Pin	Use	Function		Pin	Use	Function
19	I	RxDATA7		20	-	n.c.
21	O	RxCLK		22	-	n.c.
23	-	n.c.		24	-	n.c.
25	O	ALE_B (not used)		26	I/O	IP_B7 (ext. Pull-down)
27	I/O	IP_B6 (ext. Pull-down)		28	I/O	IP_B5 (ext. Pull-down)
29	I/O	IP_B4 (ext. Pull-down)		30	I/O	IP_B3 (ext. Pull-down)
31	I/O	IP_B2 (ext. Pull-down)		32	-	n.c.
33	-	n.c.		34	I	RESINn
35	I/O	PORESETn		36	-	n.c.
37	I/O	HRESETn		38	-	n.c.
39	-	n.c.		40	O	n.c.
41	I/O	ENMONn		42	I/O	SRESETn
43	I	JTAG/BDMn (GND)		44	-	n.c.
45	-	n.c.		46	-	n.c.
47	-	n.c.		48	-	n.c.
49	-	n.c.		50	-	n.c.
51	-	n.c.		52	I	RxD3
53	O	TxD3		54	-	n.c.
55	-	n.c.		56	-	n.c.
57	-	n.c.		58	-	n.c.
59	-	n.c.		60	-	n.c.
61	-	n.c.		62	-	n.c.
63	-	n.c.		64	O	CS7n (VINETIC)
65	O	CS6n (CPLD)		66	O	CS5n (MICO)
67	-	n.c.		68	-	n.c.
69	-	n.c.		70	-	n.c.
71	-	n.c.		72	-	n.c.
73	O	OEn		74	-	n.c.
75	-	n.c.		76	O	WE0n
77	O	WE1n		78	-	n.c.
79	-	n.c.		80		Address Bus A31 (LSB)
81		Address Bus A30		82		Address Bus A29
83		Address Bus A28		84		Address Bus A27
85		Address Bus A26		86		Address Bus A25
87		Address Bus A24		88		Address Bus A23

Table 11 Pin-out of the Connector X1 of the MPC Module (cont'd)

Pin	Use	Function		Pin	Use	Function
89		Address Bus A22		90		Address Bus A21
91		Address Bus A20		92		Address Bus A19
93		Address Bus A18		94		Address Bus A17
95		Address Bus A16		96		Address Bus A15
97		Address Bus A14		98		Address Bus A13
99		Address Bus A12		100		Address Bus A11
101		Address Bus A10		102		Address Bus A9
103		Address Bus A8		104		Address Bus A7
105		Address Bus A6		106		Address Bus A5
107		Address Bus A4		108		Address Bus A3
109		Address Bus A2		110		Address Bus A1
111	O	Address Bus A0 (MSB)		112	O	+3.3 V
113	O	+3.3 V (n.c.)		114	O	+3.3 V (n.c.)
115	I/O	GND		116	I	+5 V
117	I/O	GND		118	I	+5 V
119	I/O	GND		120	I	+5 V

Table 12 Pin-out of the Connector X2 of the MPC Module

Pin	Use	Function		Pin	Use	Function
1	-	n.c.		2	I/O	GND
3	I	TxSOC		4	O	TXDATA7
5	O	TxDATA6		6	O	TxDATA5
7	O	TxDATA4		8	-	n.c.
9	O	TxCLK		10	O	TxENB
11	O	RxENB		12	O	TxDATA3
13	O	TxDATA2		14	O	TxDATA1
15	O	TxDATA0		16	O	PC4 used as LED for status
17	O	PC5 used as LED for status		18	I	L1RSYNCB (MPC FSC)
19	-	n.c.		20	I	PC8 used as $\overline{CD2}$ for SCC2
21	I	PC9 used as $\overline{CTS2}$ for SCC2		22	I	PC10 used as CD (Ethernet)
23	I	PC10 used as COL (Ethernet)		24	O	PC12 used as LBK (Ethernet)
25	-	n.c.		26	O	PC14 used as $\overline{RTS2}$ for SCC2
27	I	RxCLAV0		28	-	n.c.
29	O	PA1 used as SPICSn		30	I	L1RCLKb (MPC DCL)

Table 12 Pin-out of the Connector X2 of the MPC Module (cont'd)

Pin	Use	Function		Pin	Use	Function
31	-	n.c.		32	-	n.c.
33	I	PA5 used as TCLK (Ethernet)		34	I	PA6 used as SCC2CLK
35	I	PA7 used as RCLK (Ethernet)		36	O	PA 8 used as LED for status
37	O	PA9 used asLED for status		38	I	L1RxDb (MPC RxD)
39	O	L1TxDb (MPC TxD)		40	I/O	PA12/TXD2 (SCC2)
41	I/O	PA13/RXD2 (SCC2)		42	O	PA14 used as TxD (Ethernet)
43	I	PA15 used as RXD (Ethernet)		44	I	TDI (BDM interface)
45	O	TDO (BDM interface)		46	I	TCK (BDM interface)
47	I	n.c.		48	O	RxADDR2
49	O	TxCLAV0 (n.c.)		50	O	RxADDR0
51	O	RxADDR1		52	O	RxADDR4
53	O	PB19 used as TEN (Ethernet)		54	O	TxADDR0
55	O	TxADDR1		56	O	TxADDR0
57	O	TxADDR3		58	O	TxADDR2
59	O	RxADDR3		60	-	n.c.
61	-	n.c.		62	I	PB28 used as SPIMISO
63	O	PB29 used as SPIMOSI		64	O	PB30 used as SPICLK
65	I	PB31 used as SPISEL (Pullup)		66	-	n.c.
67	-	n.c.		68	-	n.c.
69	-	n.c.		70	I/O	CRn/IRQ3n (ext. Pull-up)
71	I/O	FRZ (BDM Interface)		72	-	n.c.
73	O	RD/WRn		74	I	BGn (Pullup)
75	I	BBn (Pullup)		76	I	BRn (Pullup)
77	I	TAn (Pullup)		78	-	n.c.
79	-	n.c.		80	-	n.c.
81	-	n.c.		82	-	n.c.
83	-	n.c.		84	-	n.c.
85	-	n.c.		86	-	n.c.
87	-	n.c.		88	I/O	Data Bus D0 (MSB) (MD0)
89	I/O	Data Bus D1 (MD1)		90	I/O	Data Bus D2 (MD2)
91	I/O	Data Bus D3 (MD3)		92	I/O	Data Bus D4 (MD4)
93	I/O	Data Bus D5 (MD5)		94	I/O	Data Bus D6 (MD6)
95	I/O	Data Bus D7 (MD7)		96	I/O	Data Bus D8 (MD8)
97	I/O	Data Bus D9 (MD9)		98	I/O	Data Bus D10 (MD10)
99	I/O	Data Bus D11 (MD11)		100	I/O	Data Bus D12 (MD12)

Table 12 Pin-out of the Connector X2 of the MPC Module (cont'd)

Pin	Use	Function		Pin	Use	Function
101	I/O	Data Bus D13 (MD13)		102	I/O	Data Bus D14 (MD14)
103	I/O	Data Bus D15 (MD15)		104	I/O	Data Bus D16
105	I/O	Data Bus D17		106	I/O	Data Bus D18
107	I/O	Data Bus D19		108	I/O	Data Bus D20
109	I/O	Data Bus D21		110	I/O	Data Bus D22
111	I/O	Data Bus D23		112	I/O	Data Bus D24
113	I/O	Data Bus D25		114	I/O	Data Bus D26
115	I/O	Data Bus D27		116	I/O	Data Bus D28
117	I/O	Data Bus D29		118	I/O	Data Bus D30
119	I/O	Data Bus D31 (LSB)		120	I/O	GND

6.8 RS232 Connector (ST3)

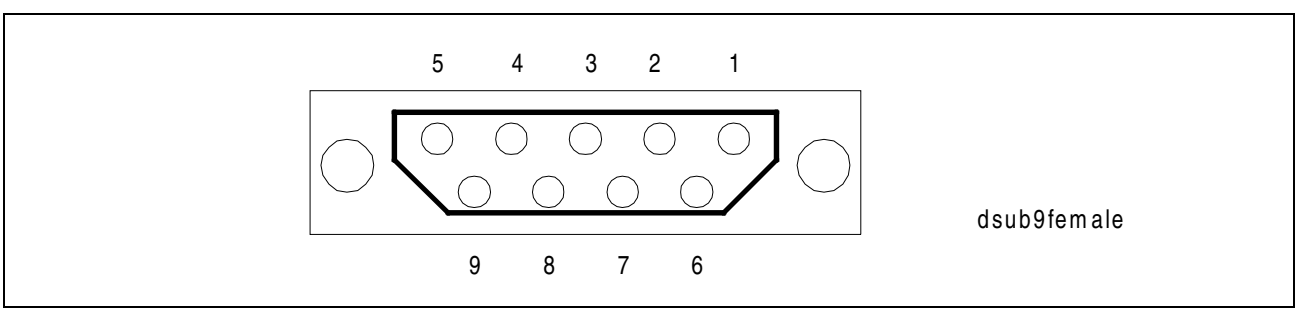


Figure 13 D-SUB9 Connector Pinout ST3 (Front View)

Table 13 Pinout of the D-SUB9 Connector ST3

Pin	MPC pin	Property	Connected Signal	Description
1	RESINn	I	RES232	Reset over RS232 interface
2	TxD3	O	TxD3	Transmit Debud Interface
3	RxD3	I	RxD3	Receive Debug Interface
4	ENMONn	I	ENMON	
5	GND	I/O	DGND	Power Supply
6	ENMONn		ENMON	
7	n.c.			
8	n.c.			
9	n.c.			

The signal RES232 is not supported by the VINETIC Evaluation Board.

6.9 Ethernet Connector ST2

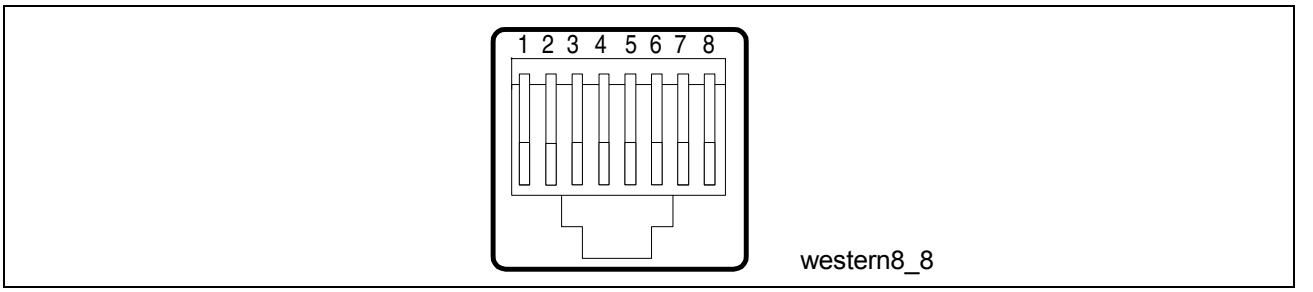


Figure 14 Ethernet Connector ST2 (Front View)

Table 14 Ethernet Connector ST2

Pin	Use	Function
1	I	Rx+
2	I	Rx-
3	O	Tx+
4	-	n.c.
5	-	n.c.
6	O	Tx-
7	-	n.c.
8	-	n.c.

6.10 IOM-2 Connector ST4

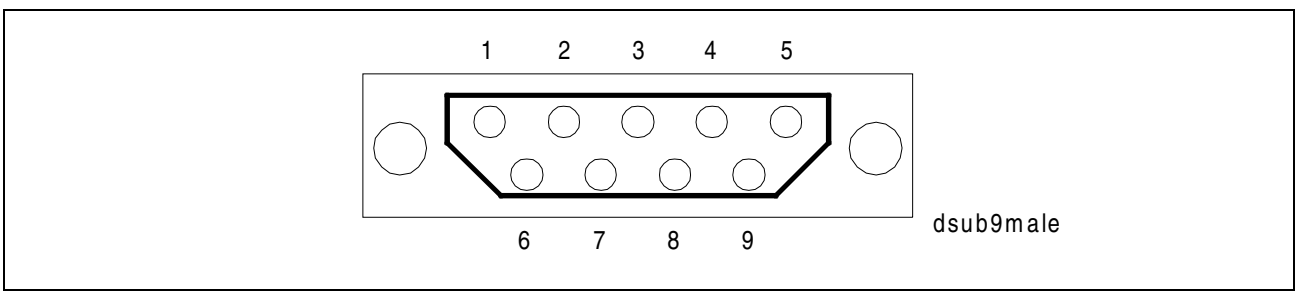


Figure 15 Pinout IOM-2 DSUB-9 Connector ST4 (Front View)

Table 15 Pin Locations IOM-2 Connector ST4

Pin	Use	Function
1	n.c.	
2	O (OD)	IRESn
3	n.c.	
4	O	Data upstream (DU) (iTXD)
5	I	Data Downstream (DD) (iRXD)
6	I	Frame Sync (FSC) (IFSC)
7	I	Data Clock (DCL) (IDCL)
8	n.c.	
9	I/O	Power Ground

6.11 BDM Interface Connector (JP1)

The BDM port has to interface to a Lauterbach MPC-debugger and be compatible to the TQC Starter Kit.

On the EASY 334 VINETIC Evaluation Board a 1 row connector is placed. The Lauterbach MPC-debugger has a two row female connector. Therefore, a adaptor cable has to be configured to connect both connectors (pin-to-pin). **Figure 16** shows both connectors.

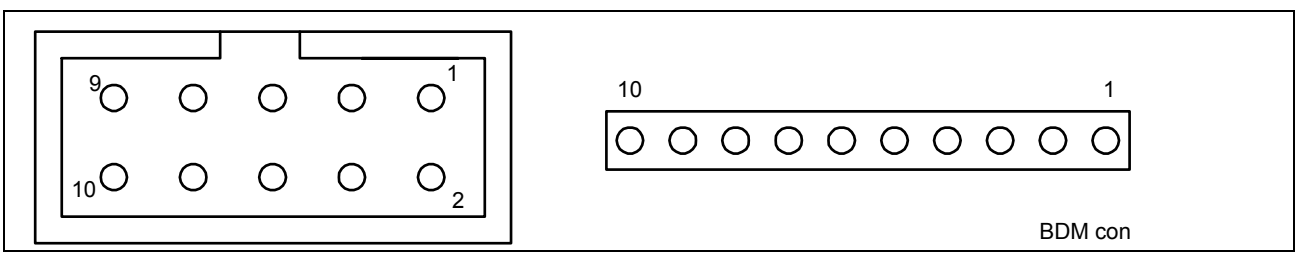


Figure 16 BDM Connector (Top View)

Table 16 Pinout of BDM Connector

Pin	Name	Description
1	FRZ	MPC Connector X2 pin 10
2	SRESETn	MPC Connector X1 pin 42
3	DGND	Power supply GND
4	DSCK/TCK	MPC Connector X2 pin 46
5	DGND	Power supply GND

Table 16 Pinout of BDM Connector

Pin	Name	Description
6	FRZ	MPC Connector X2 pin 10
7	HRESETQ	MPC Connector X1 pin 37
8	DSDI/TDI	MPC Connector X2 pin 44
9	VCC3V3	Power supply +3.3 V
10	DSDO/TDO	MPC Connector X2 pin 45

6.12 JTAG Connector ST1

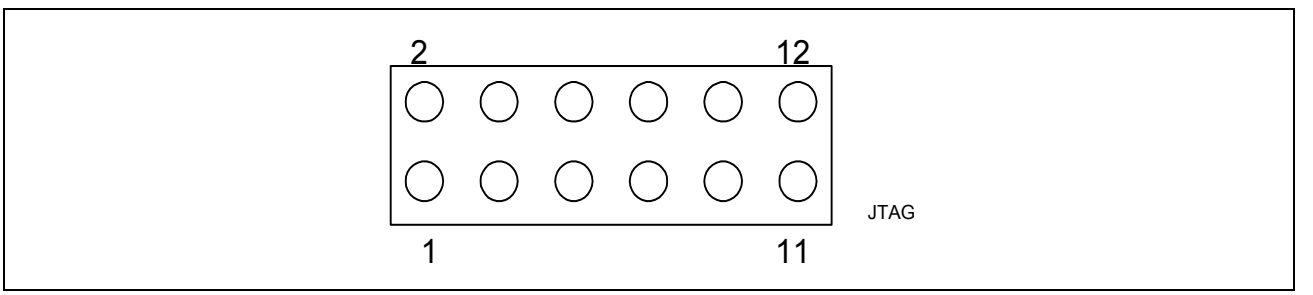


Figure 17 JTAG Connector ST1 (Top View)

Table 17 JTAG Connector ST1

Pin	Use	Function		Pin	Use	Function
1	I	TCK		2	I/O	GND
3	I	TMS		4	I/O	GND
5	O	TDO		6	I/O	GND
7	I	TDI		8	I/O	GND
9	I	TRST# (TDRS)		10	I/O	+3.3 V
11	I	TEST		12	I/O	+3.3 V

Please note, that the JTAG can not be connected directly to a parallel port of a PC. A level shifter has to be placed between the JTAG interface connector and the PC, because the VINETIC pads are not +5V resistant.

6.13 Header Pin-outs

6.13.1 Measurement Header JP2

The Header JP2 is for voltage measurements.

- JP2 pin 1 is connected to +3.3 V.
- JP2 pin 2 is connected to GND.

6.13.2 MPC Measurement Header JP3

The header JP3 carries the control signals of the MPC862 µC-interface.

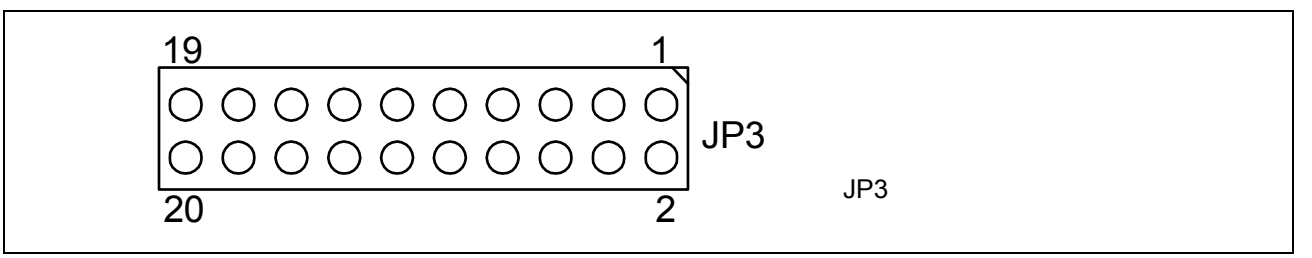


Figure 18 MPC Measurement Header JP3 (Top View)

Table 18 MPC Measurement Header JP3

Pin	Use		Pin	Use
1	nc		2	PORESETn
3	nc		4	MPCRESn
5	CS5 (MICO)		6	HRESETn
7	CS6 (CPLD)		8	SRESETn
9	CS7 (VINETIC)		10	ENMONn
11	MIRQ7 (MICO)		12	OEn
13	MIRQ6 (VINETIC)		14	WE1n
15	MIRQ5 (VINETIC READYn)		16	WE0n
17	nc		18	R/WRn
19	GND		20	GND

6.13.3 Header JP8, JP9, JP10 and JP11and Power Supply Jumper

All pins of the VINETIC are connected to test pins for better access for measurements.The power supply of the VINETIC is connected by jumper in parallel to a 0R-resistor. To measure the current of the VINETIC the 0R-resistor can be removed and via the jumper the current can be measured or a 0.1R is soldered instead of the 0R and

the voltage is measured above the resistor. In this case the voltage corresponds to the current. In **Figure 19** the current jumpers and the measurement headers are shown.

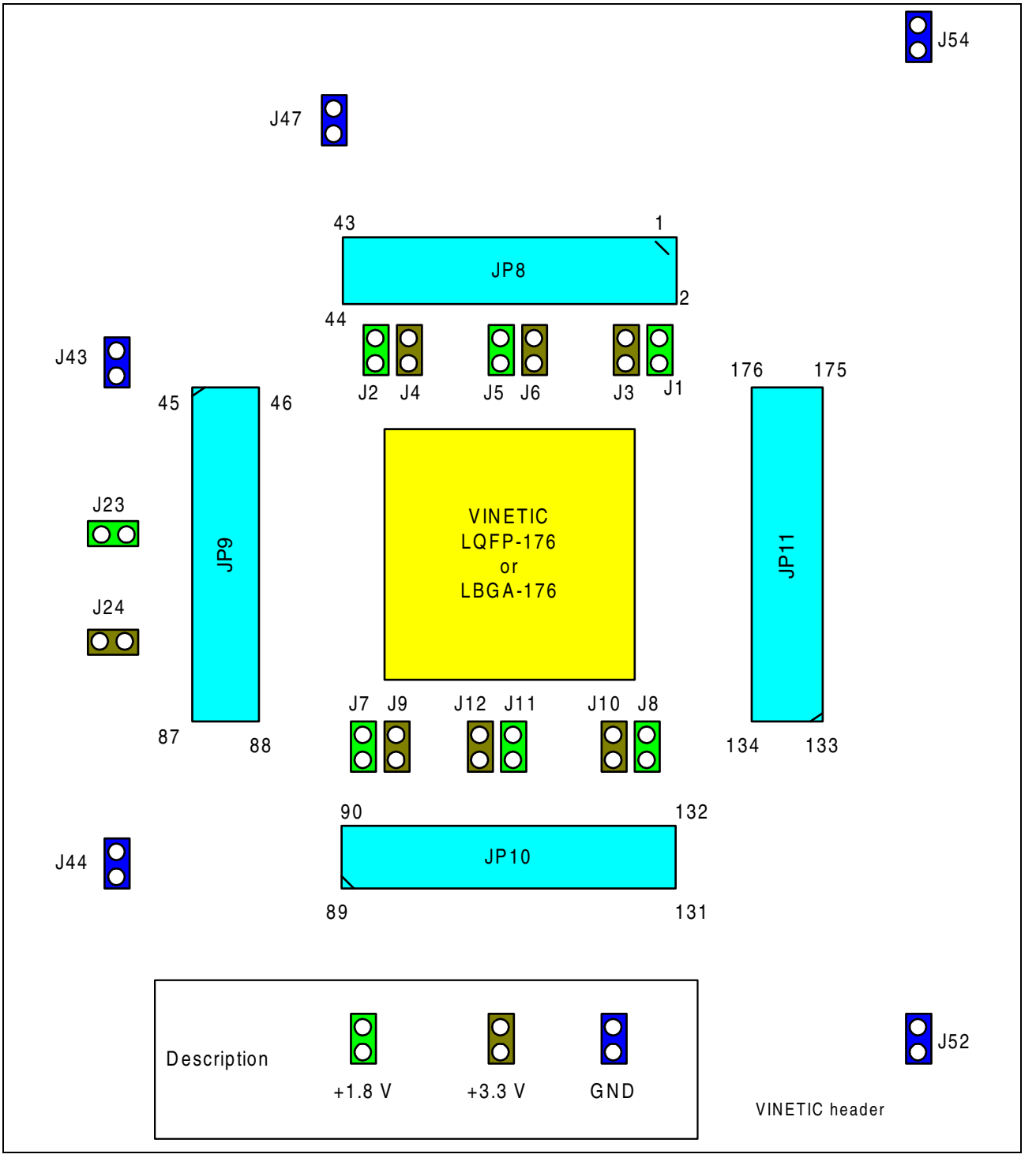


Figure 19 Testheader JP8, JP9, JP10 and JP11 and Power Supply Jumper

6.13.4 MPC Measurement Header JP4

The asynchronous and synchronous serial interfaces are connected to header JP4 for measurements.

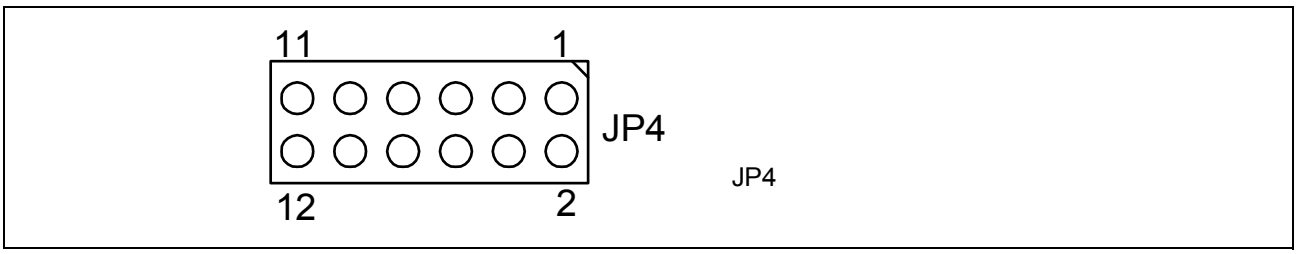


Figure 20 MPC Measurement Header JP4 (Top View)

Table 19 Header JP4

Pin	Use		Pin	Use
1	RxD2		2	SPIMISO
3	TxD2		4	SPIMOSI
5	RTS2n		6	SPICLK
7	CTS2n		8	SPICSn
9	CD2n		10	GND
11	SCC2CLK		12	GND

6.13.5 MPC µC-interface and PCM inteface Header JP5

The µC-interface is connected for measurements at this header JP5.

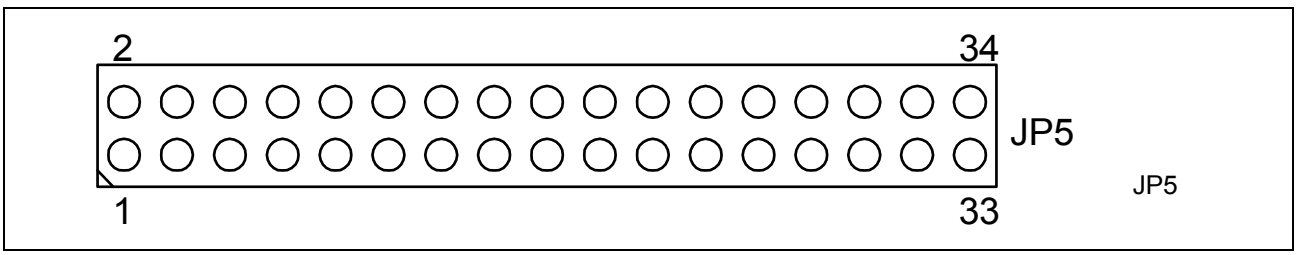


Figure 21 MPC µC-Interface and PCM Interface Header JP5 (Top View)

Table 20 Header JP5

Pin	Use		Pin	Use
1	A0 (MPC A31)		2	A1 (MPC A30)
3	A2 (MPC A29)		4	A3 (MPC A28)

Table 20 Header JP5 (cont'd)

Pin	Use		Pin	Use
5	A4 (MPC A27)		6	A5 (MPC A26)
7	A6 (MPC A25)		8	A7 (MPC A24)
8	A8 (MPC A23)		10	MPC FSC (MPC L1RSYNCb)
11	nc		12	MPC DCL (MPC L1RCLKb)
13	nc		14	MPC RxD (MPC L1RxDb)
15	nc		16	MPC TxD (MPC L1TxDb)
17	D0 (MPC D0)		18	D1 (MPC D1)
19	D2 (MPC D2)		20	D3 (MPC D3)
21	D4 (MPC D4)		22	D5 (MPC D5)
23	D6 (MPC D6)		24	D7 (MPC D7)
25	D8 (MPC D8)		26	D9 (MPC D9)
27	D10 (MPC D10)		28	D11 (MPC D11)
29	D12 (MPC D12)		30	D13 (MPC D13)
31	D14 MPC (D14)		32	D15 (MPC D15)
33	GND		34	GND

6.13.6 Monitor Setting with JP6

The jumper JP6 should be only closed, when the firmware has to be donloaded by Infineon Technologies.

6.13.7 VINETIC HPI Interface Header JP13

The header JP13 supports the measurement for the IFC signals of the VINETIC and the address data lines IFAD0 and IFAD1. At this header the HPI interface can be connected to a external HPI controller.

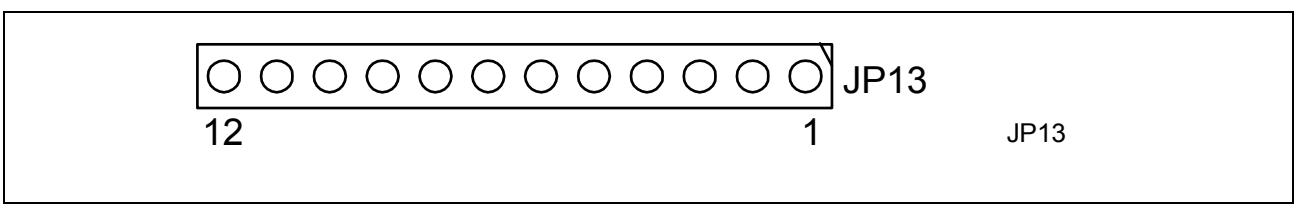


Figure 22 VINETIC IFCx signals at header JP13 (Top View)

Table 21 Header JP13

Pin	Use
1	IFC0
2	IFC1
3	IFC2
4	IFC3
5	IFC4
6	IFC5
7	IFC6
8	IFC7
9	IFC8
10	IFAD0
11	IFAD1
12	GND

6.13.8 PCM Measurement Header JP14

JP14 is connected to the PCM interface of the VINETIC.

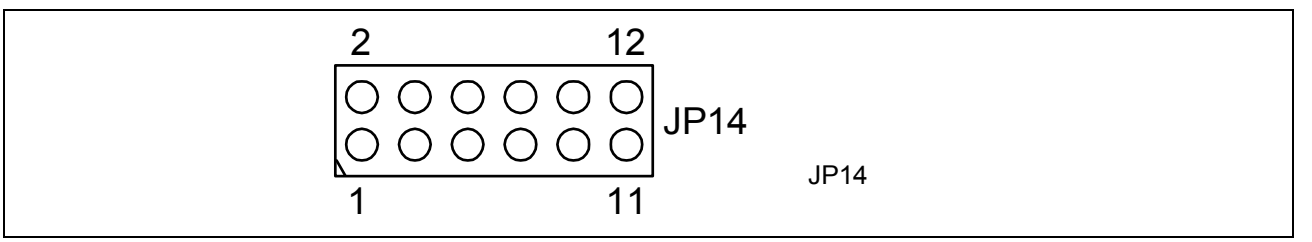


Figure 23 PCM Measurement Header JP14 (Top View)

Table 22 Header JP14

Pin	Use		Pin	Use
1	FSC		2	FSC
3	PCL/DCL		4	PCL/DCL
5	TCQ		6	TC2n
7	DX1 (Label DX)		8	DX2

Table 22 Header JP14 (cont'd)

Pin	Use		Pin	Use
9	DR1 (Label RD)		10	DR2
11	GND		12	GND

6.13.9 Status Header JP19

The register LEDs LED0..LED7 are connected in parallel to the header JP19 to connect a measurement device.

Table 23 Header JP19

Pin	Use
1	GND
2	LED0 (CMDREG4:Bit 0)
3	LED1 (CMDREG4:Bit1)
4	LED2 (CMDREG4:Bit 2)
5	LED3 (CMDREG4:Bit 3)
6	LED4 (CMDREG4:Bit 4)
7	LED5 (CMDREG4:Bit 5)
8	LED6 (CMDREG4:Bit 6)
9	LED7 (CMDREG4:Bit 7)
10	GND

6.13.10 GPIO Measurement Header JP20

The header is connected to the GPIO interface pins of the VINETIC. In parallel the LEDs D26..D33 shows the status of the signals.

6.14 Jumper Settings

No jumper (for setting mode) is placed at the EASY 334 VINETIC Evaluation Board. Jumpers are only used to measure power supply currents of the VINETIC and to select the internal or external +3.3 V power supply.

6.15 Switch Setting

6.15.1 Reset Switch S1

The reset switch resets the board. The reset signal is identical to the power-on reset signal. The complete board is resetted and the MPC gets a reset signal. After reset the software starts the program. All registers of the CPLD are set in reset state, the MICO and the VINETIC are in active reset state.

6.15.2 DIP-Switch S2

The DIP-switch S2 is to set the VINETIC host interface mode, when the EASY 334 VINETIC Evaluation Board is set in the external µC-Interface mode CMDREG2:MCSW.

6.16 Indication LEDs

Table 24 Indication LEDs

LED	Signal
D1	MPC Port PA_8
D2	MPC Port PA_9
D3	MPC Port PC4
D4	Power MPC MPC Connector X1 Pin 112
D5	MPC Port PC5
D6	Ethernet interface (Collision)
D7	Ethernet interface (Tx)
D8	Ethernet interface (Rx)
D9	Ethernet interface (Link)
D12	LED0 from Command Register 5
D13	LED1 from Command Register 5
D14	LED2 from Command Register 5
D15	LED3 from Command Register 5
D16	LED4 from Command Register 5
D17	LED5 from Command Register 5
D18	LED6 from Command Register 5
D19	LED7 from Command Register 5
D20	parallel µC interface of the VINETIC is active

Table 24 Indication LEDs (cont'd)

LED	Signal
D21	IOM-2 connector is input
D22	BNC interface connector is input
D23	Evaluation Board is clock master
D24	PCM Bypass, PCM HW A is connected to PCM HW B of VINETIC
D25	PCM HW A is selected for measurements, HW B is connected to MPC
D26	GPIO0
D27	GPIO1
D28	GPIO2
D29	GPIO3
D30	GPIO4
D31	GPIO5
D32	GPIO6
D33	GPIO7
D46	Interrupt Vinetic is active
D47	Reset line of Vinetic is active
D48	Vinetic is in IOM-2 mode
D53	power good +5 V
D54	power good +3.3 V

6.17 List of Replaceable Parts of the EASY 334 VINETIC Evaluation Board

Table 25 Components mounted on the Board

	Part Number	Description	Source
BU1, BU2, BU3, BU4	BNC	BNC plugs	
T1, T2	BSS123	P-channel FET	Infineon Technologies
Q2, Q3, Q4, Q5	BC848A	NPN transistor	Infineon Technologies
IC1	SN74LVC245ADW	octal Bus transceiver	TI
IC2	LXT905LC	Ethernet PHY	Level One
IC3	SN74ABT125	quadruple tristate driver	TI
IC4, IC5, IC6, IC8	PI5C3244	2 x quadruple analog switches	PERICOM
IC7	PEF 2015	MICO	Infineon Technologies
IC9	SN74LS125	quadruple tristate driver	TI
IC10i	ispLSI5256VA-70LQ208	CPLD	Lattice
IC11, IC12	MAX6305	Reset generator	MAXIM
IC13	PEB 3324	VINETIC LBGA-176	Infineopn Technologies
IC14	PEB 3324	VINETIC LQFP-176	Infineopn Technologies
IC15	SN74HC4051	Multiplexer	TI
IC21	LT1086CT	adjustable voltage regulator 3A	Linear Technologies
IC22	LT1086CM	adjustable voltage regulator 1A	Linear Technologies
IC23	SN74LVT245B-DW	Octal bus driver, low voltage without bus hold	Linear Technologies
D1, D2, D3, D4, D5, D7, D8, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D46, D47, D48	LED red	LED red low current	Infineopn Technologies
D9, D26, D27, D28, D29, D30, D31, D32, D33, D53, D54	LED green	LED green low current	Infineopn Technologies
D6	LED yellow	LED yellow low current	Infineopn Technologies
D10, D11	BZV55C3V3	zener diode, 3.3V	ITT

Table 25 Components mounted on the Board (cont'd)

	Part Number	Description	Source
D35, D36, D38, D40, D42, D44	SMBYW02-200	supressor diode 200V	
D34, D37	1.5KE6.8CA	transient suppressor diode, 6.8V	ST-Microelectronics
D39, D41, D43	1.5KE82CA	transient suppressor diode, 82V	ST-Microelectronics
D45	1.5KE160CA	transient suppressor diode, 160V	ST-Microelectronics
C2, C3, C6, C11, C12, 13, C14, C15, C16, C17, C36, C38, C40, C42, C53, C57, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83	100n	Ceramic Chip Capacitor, X7R, 100nF/50V 10%, SMD 0805	EPCOS
C21, C22, C29, C30	1µ	Ceramic Chip Capacitor, X7R, 1000nF/10V 10%, SMD 0805	EPCOS
C35, C107	4.7µF	Tantalum Chip Capacitor 4.7µF,16V SMD B	EPCOS
C37	100µF	Electrolytic Capacitor, 100µF/10V, 20%, 2.5mm grid	EPCOS
C43, C58, C102, C103, C104	100µF	Tantalum Chip Capacitor 100µF,16V SMD D	EPCOS
C45, C47, C49, C51	10µF	Electrolytic Capacitor, 10µF/160V, 20%, 5mm grid	EPCOS
C46, C48, C50, C52	100nF	Ceramic Chip Capacitor, X7R, 100nF/100V 10%, SMD 1812	EPCOS
C4, C5	100pF	Ceramic Chip Capacitor, NPO, 100pF/63V 5%, SMD 0603	EPCOS
C55	47nF	Ceramic Chip Capacitor, X7R, 47nF/63V 10%, SMD 0603	EPCOS
C7, C8	15pF	Ceramic Chip Capacitor, NP0, 15pF/50V 5%, SMD 0603	EPCOS
C86, C87, C88, C89	18nF	Ceramic Chip Capacitor, X7R, 18nF/63V 10%, SMD 0805	EPCOS
C9, C10	220pF	Ceramic Chip Capacitor, X7R, 220pF/63V 10%, SMD 0603	EPCOS
C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100, C101, C105, C108, C112	100nF	Ceramic Chip Capacitor, X7R, 100nF/50V 10%, SMD 0603	EPCOS
C19, C20, C27, C28	220nF	Ceramic Chip Capacitor, X7R, 220nF/50V 10%, SMD 0805	EPCOS

Table 25 Components mounted on the Board (cont'd)

	Part Number	Description	Source
C18, C54, C56	10nF	Ceramic Chip Capacitor, X7R, 10nF/50V 10%, SMD 0603	EPCOS
C1, C39, C41, C109, C110, C111, C113	100µF	Tantalum Chip Capacitor 100µF,16V SMD D	EPCOS
R1, R2, R3, R4, R5, R6, R7, R9, R10, R11, R12, R13, R14, R15, R23, R24, R25, R26	10k	Resistor, 10k, 1%, SMD0603, 1/8W	Panasonic
R113, R114, R115	1M5	Resistor, 1.5M, 1%, SMD0603 1/8W	Panasonic
R116	1M	Resistor, 1M, 1%, SMD0603, 1/8W	Panasonic
R121, R123, R125, R127, R129, R131, R133, R136	750R	Resistor, 750R, 1%, SMD0603, 1/8W	Panasonic
R155, R157, R237, R239	220R	Resistor, 220R, 1%, SMD00603, 1/8W	Panasonic
R156, R238	360R	Resistor, 360R, 1%, SMD0603, 1/8W	Panasonic
R34, R158, R240	100R	Resistor, 100R, 1%, SMD0603, 1/8W	Panasonic
R159	3k3	Resistor, 3.3k, 1%, SMD0603, 1/8W	Panasonic
R165, R166, R167, R168, R169, R171, R172, R173	510R	Resistor, 510R, 1%, SMD0603, 1/8W	Panasonic
R17, R18, R19, R20, R21, R182	470R	Resistor, 470R, 1%, SMD0603, 1/8W	Panasonic
R170, R174, R175, R176	22k	Resistor, 22k, 1%, SMD0603, 1/8W	Panasonic
R30, R31, R32, R33	1k	Resistor, 1k, 1%, SMD0603, 1/8W	Panasonic
R35, R36, R47, R48, R55	4k7	Resistor, 4.7k, 1%, SMD00603, 1/8W	Panasonic
R37, R41	12R	Resistor, 12R, 1%, SMD0603, 1/8W	Panasonic
R40	7k5	Resistor, 7.5k, 1%, SMD0603, 1/8W	Panasonic
R42, R45, R46	0R	Resistor, 0R, SMD0603, 1/8W	Panasonic
R49, R50	33R	Resistor, 33R, 1%, SMD00603, 1/8W	Panasonic

Table 25 Components mounted on the Board (cont'd)

	Part Number	Description	Source
R51, R54, R57, R60	49R9	Resistor, 49.9R, 1%, SMD0603, 1/8W	Panasonic
R52, R53, R112, R134, R137, R138, R139, R140, R141	2k2	Resistor, 2.2k, 1%, SMD0603, 1/8W	Panasonic
R56, R58, R59, R81, R117, R118, R119, R120, R191	10k	Resistor, 10k, 1%, SMD0603, 1/8W	Panasonic
R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R74, R76, R78, R162, R163, R164, R181	560R	Resistor, 560R, 1%, SMD0603, 1/8W	Panasonic
R72, R73, R80	200k	Resistor, 200k, 1%, SMD0603, 1/8W	Panasonic
R75, R186, R187, R188, R189	100k	Resistor, 100k, 1%, SMD0603, 1/8W	Panasonic
R77	820k	Resistor, 820k, 1%, SMD0603, 1/8W	Panasonic
R79	910k	Resistor, 910k, 1%, SMD0603, 1/8W	Panasonic
R82	680k	Resistor, 680k, 1%, SMD0603, 1/8W	Panasonic
R83	360k	Resistor, 360k, 1%, SMD0603, 1/8W	Panasonic
R84, R85, R98, R99	1k6	Resistor, 1.6k, 1%, SMD0603, 1/8W	Panasonic
R86, R89, R90, R91, R92, R93, R94, R95, R96, R97, R100, R103, R104, R105, R106, R107, R108, R109, R110, R111, R122, R124, R126, R128, R130, R132, R135, R142, R143, R144, R145, R146, R147, R148, R149, R150, R151, R190	0R	Resistor, 0R, SMD0603, 1/8W	Panasonic
R87, R88, R101, R102	680R	Resistor, 680R, 1%, SMD0603, 1/8W	Panasonic
RP1	10k	Resistor array 15 x 10k, 1%, SMD 16 pole, 1/8W	Panasonic
RP2, RP3, RP4	10k	Resistor array 4 x 10k, 1%, SMD1206, 8 pole, 1/8 W	Panasonic

Table 25 Components mounted on the Board (cont'd)

	Part Number	Description	Source
Q1	20MHz	crystal 20 MHz HC49/U	VERCTRON
X1, X2	AMP 179-030-5	Board to Board connector	AMP
X3	VCC1-B1D-24M576	oscillator 24.576MHz +/-30ppm, 3.3V	VECTRON
TR1	HALO TG-74 1406N1	Ethernet transformer	Halo
ST2	Westen Modular Jack	Internet Interface connector 8 pole	TYCO
ST3	D-Sub9 male	EthernetConnector	TYCO
ST4	D-Sub 9 female	IOM-2 Interface Connector SAC	TYCO
ST6, ST7	AMP 0-0100-147-1	110 pin SLIC Connector	TYCO
ST8, ST9, ST10, ST11	HC-2532-10	10 pin Connector	Seltronics
ST12	Power Connector	Power Connector 11 pins	Stocko
ST14	D-Sub25 female	Debug Interface female connector	TYCO
S1	Reset	push-button key	TYCO
S2	DIP-Shwitch	10 pins DIP-switch	TYCO
MPC Module	MPC862 80 MHz Module	MPC862 with 80 MHz, 8 MByte Flash, 16 MByte SDRAM, no 1. and 2. CAN interface, with RS232 driver and with switch power supply	TQC
F1, F2	1 A Fuse	1 A, Fuse, SMD, carrier	Seltronics
F3, F4, F5, F6	0.75 A Fuse	0.75 A Fuse, SMD, Carrier	Seltronics

Table 26 Components not mounted on the Board

	Part Number	Description	Source
C25, C33	100n	Ceramic Chip Capacitor, X7R, 100nF/50V 10%, SMD 0603	EPCOS
IC13	PEB 3324	VINETIC LBGA-176	Infineopn Technologies
IC21	LT1086CT	adjustable voltage regulator 3A	Linear Technologies
IC22	LT1086CM	adjustable voltage regulator 1A	Linear Technologies
R235, R236	0R	Resistor, 0R, 1%, SMD0603, 1/8W	e.g. Panasonic
R38,R39,R43,E44	4k7	Resistor, 4.7k, 1%, SMD0603, 1/8W	e.g. Panasonic

Table 26 Components not mounted on the Board (cont'd)

	Part Number	Description	Source
R8, R16, R22, R27, R29	nm	Resistor, SMD0603, 1/8W	e.g. Panasonic
ST13	Connector 40x2 pins female	40x2 pins, female connector, SMD, (COBALT)	FCI

6.18 Floor Plan of the EASY 334 VINETIC Evaluation Board

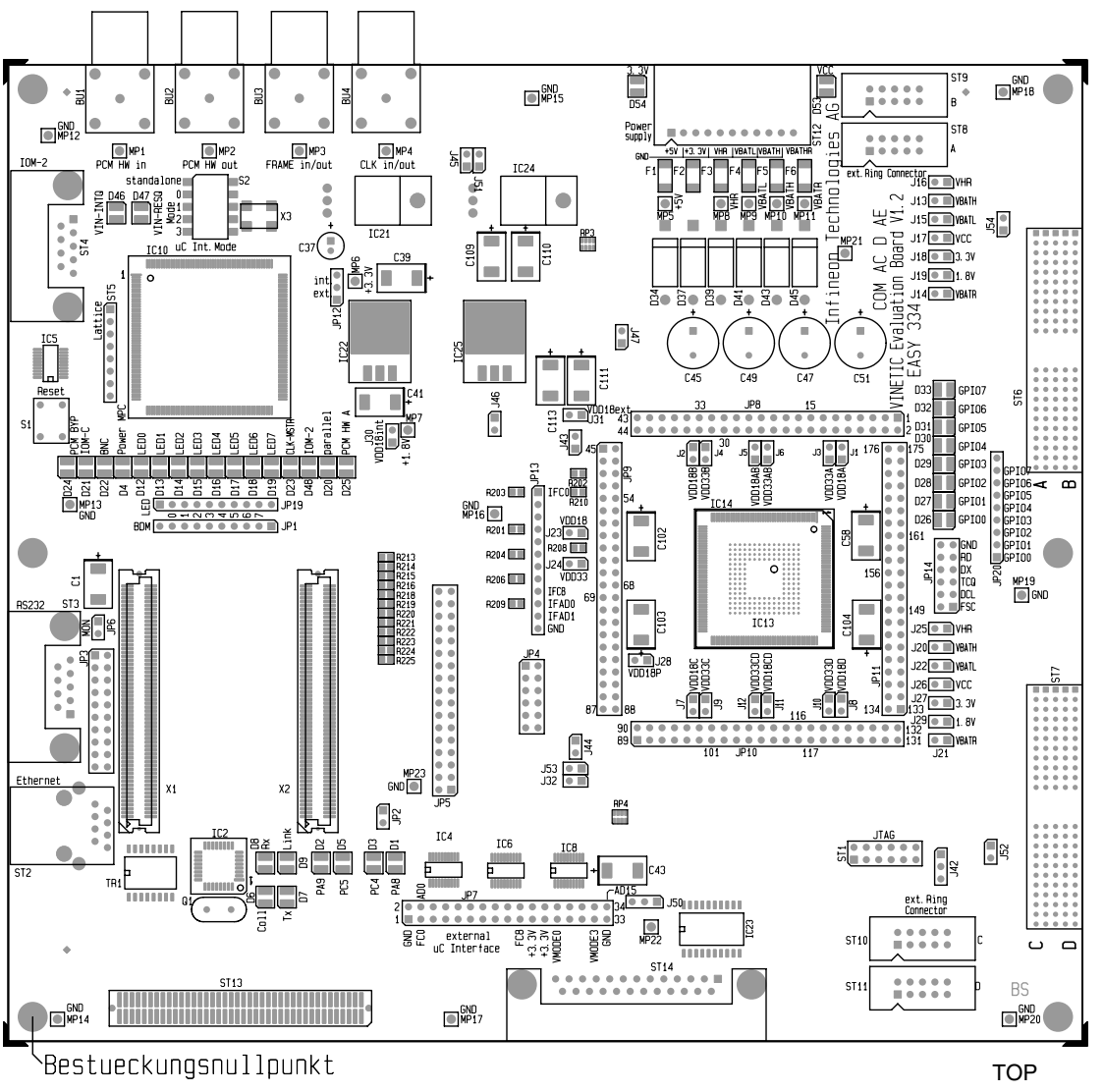


Figure 24 Floor Plan of the VINETIC Evaluation Board (Top View)

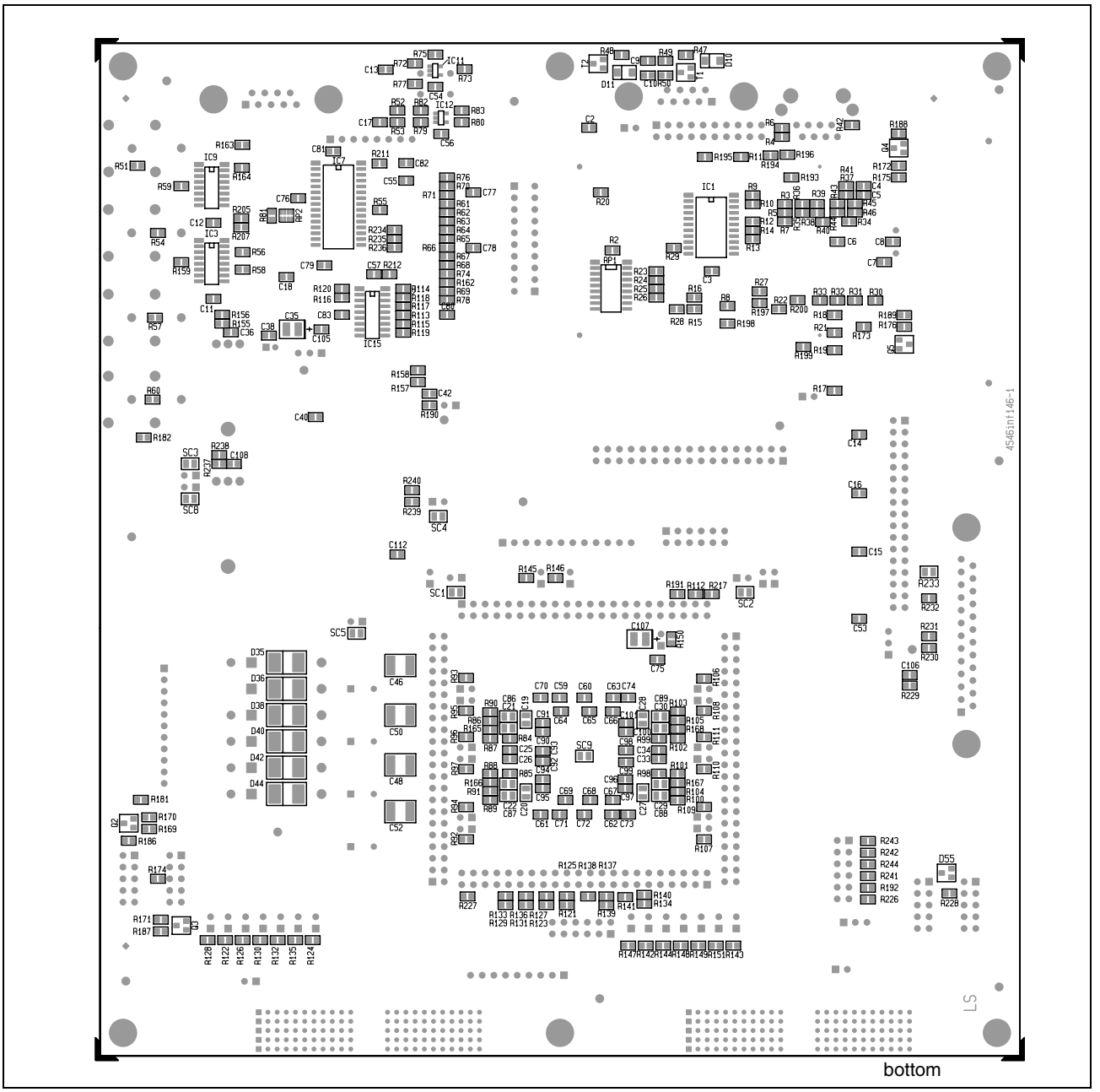


Figure 25 Floor Plan of the VINETIC Evaluation Board (Bottom View)

6.19 Default Jumper Setting

The board is delivered with the following jumper setting shown in **Figure 26**.

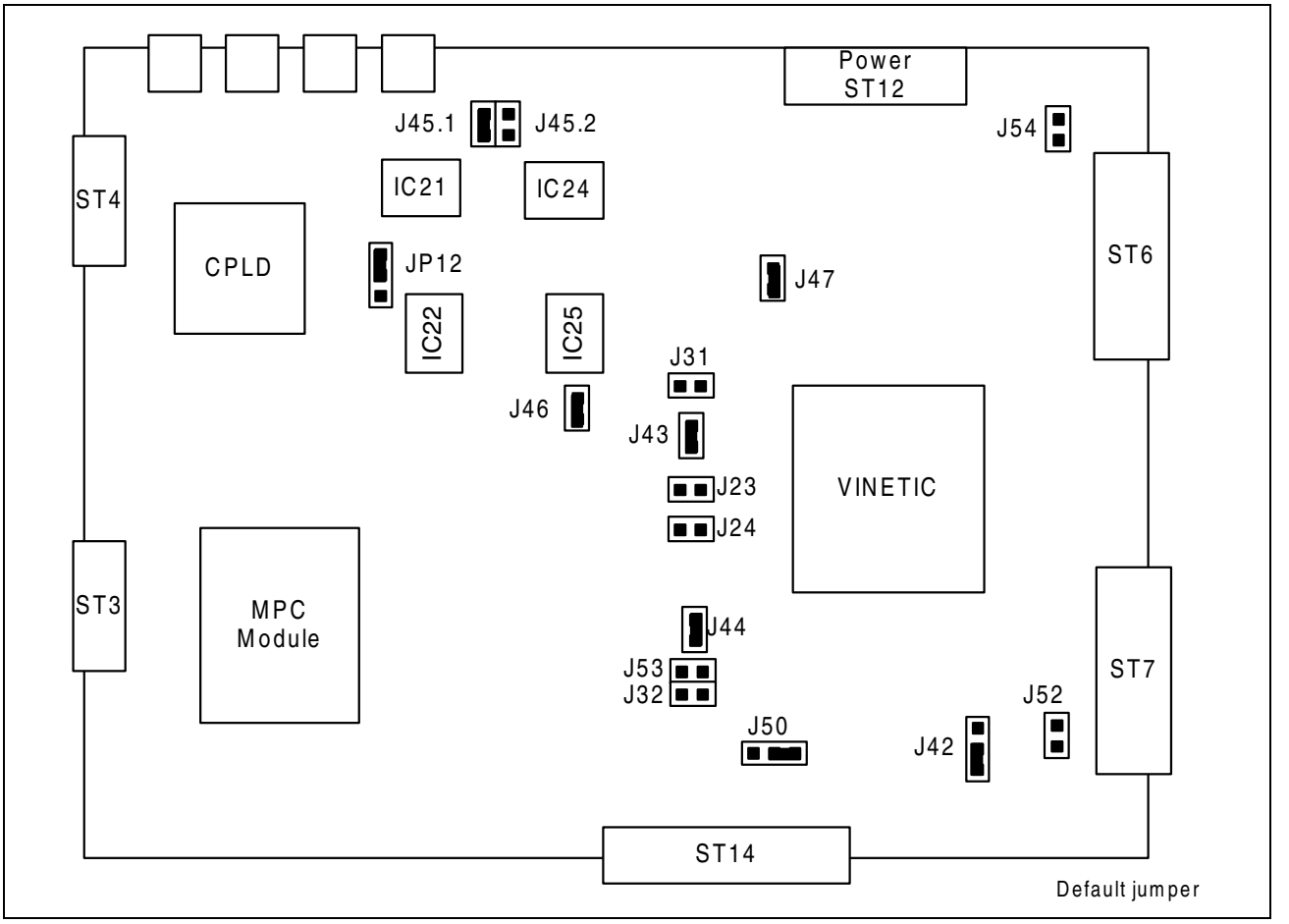


Figure 26 Default Jumper Setting

The following two jumper setting are depends of the mounted voltage regulators.

- J45.1 must be open, when IC24 is mounted.
- J46 must be open, when IC25 is mounted.

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