

# VINETIC<sup>®</sup>

Voice and Internet Enhanced Telephony  
Interface Circuit

VINETIC<sup>®</sup>-4VIP, PEB 3324, V1.4

VINETIC<sup>®</sup>-2VIP, PEB 3322, V1.4

VINETIC<sup>®</sup>-2CPE, PEB 3332, V1.4

VINETIC<sup>®</sup>-0, PEB 3320, V1.4

VINETIC<sup>®</sup>-4M, PEB 3314, V1.4

VINETIC<sup>®</sup>-4C, PEB 3394, V1.4

VINETIC<sup>®</sup>-4S, PEB 3304, V1.4

Software Description

Wireline Communications



Never stop thinking.

ABM<sup>®</sup>, ACE<sup>®</sup>, AOP<sup>®</sup>, ARCOFI<sup>®</sup>, ASM<sup>®</sup>, ASP<sup>®</sup>, DigiTape<sup>®</sup>, DuSLIC<sup>®</sup>, EPIC<sup>®</sup>, ELIC<sup>®</sup>, FALC<sup>®</sup>, GEMINAX<sup>®</sup>, IDEC<sup>®</sup>, INCA<sup>®</sup>, IOM<sup>®</sup>, IPAT<sup>®</sup>-2, ISAC<sup>®</sup>, ITAC<sup>®</sup>, IWE<sup>®</sup>, IWORX<sup>®</sup>, MUSAC<sup>®</sup>, MuSLIC<sup>®</sup>, OCTAT<sup>®</sup>, OptiPort<sup>®</sup>, POTSWIRE<sup>®</sup>, QUAT<sup>®</sup>, QuadFALC<sup>®</sup>, SCOUT<sup>®</sup>, SICAT<sup>®</sup>, SICOFI<sup>®</sup>, SIDEC<sup>®</sup>, SLICOFI<sup>®</sup>, SMINT<sup>®</sup>, SOCRATES<sup>®</sup>, VINETIC<sup>®</sup>, 10BaseV<sup>®</sup>, 10BaseVX<sup>®</sup> are registered trademarks of Infineon Technologies AG. 10BaseS<sup>™</sup>, EasyPort<sup>™</sup>, VDSLite<sup>™</sup> are trademarks of Infineon Technologies AG. Microsoft<sup>®</sup> is a registered trademark of Microsoft Corporation, Linux<sup>®</sup> of Linus Torvalds, Visio<sup>®</sup> of Visio Corporation, and FrameMaker<sup>®</sup> of Adobe Systems Incorporated.

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Page	Subjects (major changes since last revision)
<b>Changes from previous version</b>	
	The following chapters have been removed: “Firmware Architecture”, “Data Packets [M-V]”, “EOP Commands (for the EDSP)”, “VOP and EVT Command (for Packet Handling) [M-V]”. These chapters can be found in the <Helvetica italic>Preliminary User’s Manual - EDSP Firmware Description.
	Include markers for VINETIC®-2CPE
<b>Page 66</b>	Add restriction on Command/Data Structure for two channel devices VINETIC®-2CPE and VINETIC®-2VIP.
<b>Page 95</b>	All register description have been combined into one chapter, chapter 7.
<b>Page 135</b>	Update register description AUTOMOD. Add bits AUTO-RING-EN, AUTO-MET-START and AUTO-MET-EN.
<b>Page 146</b>	Add register description AUTOMETCONF
<b>Page 149</b>	Add register description AUTORINGCONF1 through AUTORINGCONF5
<b>Page 160</b>	Update Register Description for MF-SRE1 and MR-SRE1. Add status bits CPT, CIDR-OF,UTG-ACT
<b>Page 163</b>	Update Register Description for MR-SRE2 and MF-SRE2. Add status bits EPOU-STAT, DEC-CHG-OF, remove DEC-ERR
<b>Page 193</b>	Rename Bit of register GCR1 (“DU-GPIOx” renamed to “DD-GPIOx”)
<b>Page 204</b>	Update Register Description for SRE1. Add status bits CPT, CIDR-OF,UTG-ACT
<b>Page 204</b>	Update Register Description for SRE2. Add status bits EPOU-STAT, DEC-CHG-OF, remove DEC-ERR
<b>Page 228</b>	Update Register Description for I-SRE1. Add status bits CPT, CIDR-OF,UTG-ACT
<b>Page 230</b>	Update Register Description for I-SRE2. Add status bits EPOU-STAT, DEC-CHG-OF, remove DEC-ERR

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## Preface

This *Preliminary User's Manual - Software Description* documents the internal hardware blocks, the interfacing on a software level by a host controller and gives a detailed description of all internal registers of the Voice and Internet Enhanced Telephony Interface Circuit (VINETIC®) Version 2.1 chip set family.

VINETIC® is equipped with a powerful DSP (EDSP - Enhanced Digital Signal Processor) for voice and packet processing. All functions covered by the EDSP and the corresponding host commands for configuration and operation of the VINETIC® are documented in the *Preliminary User's Manual - EDSP Firmware Description*.

This document is part of the VINETIC® Data documentation package. For more VINETIC® related documents, please see our web page at <http://www.infineon.com/vinetic>.

To simplify matters, the following synonyms and abbreviations are used:

**VINETIC®-x:** Synonym used for all codec versions VINETIC®-4VIP, VINETIC®-2VIP; VINETIC®-0, VINETIC®-2CPE, VINETIC®-4M; VINETIC®-4C and VINETIC®-4S.

**SLIC:** Synonym used for all SLIC versions SLIC-S/-S2, TSLIC-S, SLIC-E/-E2, TSLIC-E, SLIC-LCP and SLIC-P.

**[M-V-C]:** Feature or description is only valid for VINETIC®-4VIP, VINETIC®-2VIP, VINETIC®-0, VINETIC®-4M and VINETIC®-4C.

**[M-V]:** Feature or description is only valid for VINETIC®-4VIP, VINETIC®-2VIP, VINETIC®-0 and VINETIC®-4M.

**[CPE]:** Feature or description is only valid for VINETIC®-4VIP, VINETIC®-2VIP, VINETIC®-0, VINETIC®-2CPE and VINETIC®-4M.

**[V]:** Feature or description is only valid for VINETIC®-4VIP, VINETIC®-2VIP and VINETIC®-0.

**Note:** The *TSLIC-S (PEB 4364)* and *TSLIC-E (PEB 4365)* chips are dual channel versions of the *SLIC-S (PEB 4264)* and *SLIC-E (PEB 4265)* with identical technical specifications for each channel. Therefore whenever *SLIC-S* or *SLIC-E* are mentioned in the specification, also *TSLIC-S* and *TSLIC-E* can be deployed.



**CONFIDENTIAL****Organization of this Document**

This document is divided into 14 chapters and two appendices. It is organized as follows:

- **Chapter 1, Overview**  
A general description of the chip set, key features, typical applications.
- **Chapter 2, VINETIC®-x Hardware Modules**  
Logic symbol of chip, Hardware blocks, Basic setup.
- **Chapter 3, Operational Description**  
Operating and automatic modes, boot sequence, reset behavior, test modes, interrupt handling and some other functionality.
- **Chapter 4, Command/Data Structure**  
Command structure and data transfer for commands and packets
- **Chapter 5, Mailbox Concept, Data Handling**  
Data handling for commands and packets
- **Chapter 6, Interface Description**  
Interface description of parallel and serial host interface and PCM interface
- **Chapter 7, Register Description**  
Register overview and detailed description of ALM registers which are accessed using the SOP command, Coefficient RAM (CRAM) registers which are accessed using the COP command, and PHI registers which are accessed using the IOP command and short commands.
- **Terminology**  
List of abbreviations and descriptions of symbols.
- **Index**
- **Appendix**  
Register description format and list of used standards

**CONFIDENTIAL****Related Documentation**

- *Product Overview:*  
VINETIC® Prel. Product Overview Rev. 2.0, 2004-05-11
- *Preliminary User's Manual - System Reference:*  
VINETIC® Version 1.4 Prel. User's Manual – System Reference DS1, 2003-10-15
- *Preliminary Data Sheets:*  
VINETIC®-4VIP (PEB 3324) Version 1.4 Prel. Data Sheet DS1, 2003-08-07  
VINETIC®-4S (PEB 3304) Version 1.4 Prel. Data Sheet DS1, 2003-08-04  
VINETIC®-4M (PEB 3314) Version 1.4 Prel. Data Sheet DS1, 2003-08-07  
VINETIC®-4C (PEB 3394) Version 1.4 Prel. Data Sheet DS1, 2003-09-24  
VINETIC®-2VIP (PEB 3322) Version 1.4 Prel. Data Sheet DS1, 2003-08-07  
VINETIC®-2CPE (PEB 3332) Version 1.4 Prel. Data Sheet Rev. 1.0, 2004-05-12  
VINETIC®-0 (PEB 3320) Version 1.4 Prel. Data Sheet DS1, 2003-08-07
- *Preliminary User's Manual - EDSP Firmware Description:*  
VINETIC® Version 1.4/2.1 Prel. User's Manual – EDSP Firmware Description Rev. 1.0, 2004-06-18
- *Firmware Overview EDSP:*  
VINETIC® Version 1.4 Firmware Overview EDSP
- *Other related documents:*  
VINETIC® Firmware Release Notes EDSP  
VINETIC® Version 1.4 Preliminary Status Sheet EDSP Firmware Rev. 3, 2004-02-24  
VINETIC® Version 1.4 Prel. Status Sheet ALM Downloads Rev. 1.0, 2003-12-19

*Note: Please refer to the latest revision of the documents.*

# 1 Overview

The VINETIC® is a product line of devices for accessing the analog telephone line. VINETIC® devices are available in different granularity (0, 2, 4 and 8 analog voice channels) and also with different levels of DSP performance (VIP, CPE, M, C, S). The seamless connection to a broad range of SLICs provides the most effective solution for each application.

The VINETIC® performance facilitates the utilization of the device in linecards as well as in CPE applications. Further integration on the existing board space is easily achieved by having an integrated DSP both for voice processing and packetization.

The VINETIC® provides system solutions for the following applications:

- Access Network:
  - Central Office - TDM
  - Digital Loop Carrier - TDM, VoATM, VoIP
  - FTTH - TDM, VoATM, VoIP
  - WLL - TDM, VoIP
- PBX:
  - Analog Linecard - TDM, VoIP
- Customer Premises Equipment:
  - Residential Gateway / Home Gateway / Internet Telephony Gateway (ITG) - VoIP
  - Integrated Access Device (IAD) - VoIP, VoATM
  - Cable Modems / Media Terminal Adapter (MTA) - VoIP
  - Analog Telephony Adapter (ATA) - VoIP

To cover these applications, the VINETIC® devices are pin- and software-compatible, allowing the maximum flexibility while offering the optimized feature set per application.

**Table 1 on Page 11** and **Table on Page 13** give an overview of the features of the different VINETIC® devices.

**Table 1 VINETIC® Devices**

Chip Set <sup>1)</sup>	VINETIC®- 4VIP/2VIP	VINETIC®- 2CPE	VINETIC®- 0	VINETIC®- 4M/8M	VINETIC®- 4C
Product ID	PEB 3324	PEB 3332	PEB 3320	PEB 3314 PEB 3318	PEB 3394
Analog Channels	4/2	2	0	4/8	4
Echo Cancellation (G.165, G.168)	up to 128 ms	up to 16 ms	up to 128 ms	up to 16 ms	up to 16 ms
ADPCM (G.726)	Yes	Yes	Yes	Yes	Yes

**Table 1 VINETIC® Devices**

Chip Set <sup>1)</sup>	VINETIC®- 4VIP/2VIP	VINETIC®- 2CPE	VINETIC®- 0	VINETIC®- 4M/8M	VINETIC®- 4C
Complex Voice Codecs (G.723, G.728, G.729) <sup>2)</sup>	Yes	Yes	Yes	No	No
Fax Relay T.38	Yes	Yes	Yes	No	No
Signal processing functions <sup>3)</sup>	Yes	Yes	Yes	Yes	Yes
AAL2, RTP packetization, Jitter Buffer	Yes	RTP only	Yes	Yes	No
Integrated Code RAM for Firmware Download	Yes	Yes	Yes	Yes	No <sup>6)</sup>
Line testing AITDF <sup>4)</sup>	Yes	GR909 only	Yes	Yes	Yes
World wide programmability of analog BORSCHT <sup>5)</sup> functions	Yes	Yes	–	Yes	Yes

<sup>1)</sup> All 4-, 2- and 0-channel devices are pin- and software compatible, except the VINETIC-2CPE that is optimized for CPE market; for 8-channel codecs contact local sales.

<sup>2)</sup> Patent indemnification available.

<sup>3)</sup> e.g. DTMF generation and detection, Caller ID (CLIP) generation (FSK), Universal Tone Detection (UTD), Answering Tone Detection (ATD), Caller-ID detection, Universal Tone Generator (covering Japanese Tones), Call Progress Tone detector.

<sup>4)</sup> Advanced Integrated Test and Diagnosis Functions.



- 5) Battery feed, Ringing, Signaling (supervision), Coding, Hybrid for 2/4-wire conversion, Testing, Hook thresholds, Teletax metering.
- 6) Versions up to v1.4 provide also RAM for firmware download

## Firmware Variants

Due to the big variety in functionality of the different VINETIC® devices the EDSP firmware is supplied in different variants and versions. An EDSP Firmware variant comprises a specific set of functions and can be downloaded to one specific VINETIC® device only. The limitation in memory space and processing power makes it necessary that even for one specific VINETIC® device different firmware variants may be supplied. Dependent on the required packetization protocol, type and number of coder channels the specific firmware has to be downloaded.

This user's manual gives a description of all functions provided by different EDSP firmware variants. The document *Firmware Overview VINETIC® EDSP* provides a summary of the currently available VINETIC® EDSP firmware variants. The detailed listing of modules, coders and commands which are supported within a specific firmware variant can be found in the corresponding *Prel. VINETIC® Firmware Release Notes*.

**Table 2 VINETIC® Features**

VIP	CPE	M	C	S	0	VINETIC® Features
<b>Common Features</b>						
2/4	2	4/8	4	4/8	0	Number of fully programmable codecs with enhanced signal processing capabilities <sup>1)</sup>
•		•	•	•	•	Pin-compatible and software compatible
•	•	•	•	•		Glueless interface to Infineon SLICs family: SLIC-S/-S2, TSLIC-S, SLIC-E/-E2, TSLIC-E and SLIC-P, SLIC-LCP and SLIC-DC, GEMINAX-S, GEMINAX-S MAX
<b>Integrated DSP Features</b>						
•	•	•			•	Integrated DSP with RAM for VoIP/VoDSL/VoATM and software download capability <sup>2)</sup>
•	•	•	•		•	for enhanced signal processing
•	•	•			•	RTP packetization & jitter buffer (adaptive and fixed; 200 ms)
•	•	•			•	RTCP support

**CONFIDENTIAL**
**Overview**
**Table 2 VINETIC® Features (cont'd)**

VIP	CPE	M	C	S	0	VINETIC® Features
•		•			•	AAL2 cell generation & jitter buffer (adaptive and fixed; 200 ms)
•		•			•	Compatible with ITU-T I.366.2
•	•	•			•	Compatible with RFC 1889 specification
•	•	•			•	Compatible with Packet Cable specification
•		•			•	PacketOverPCM functionality
•	•	•	•	•	•	Integrated DTMF generator
•	•	•	•		•	Integrated DTMF decoder
•	•	•	•		•	Integrated Caller ID (FSK) generator, according to Bellcore 202 and V.23
•	•	•	•		•	Integrated Caller ID (FSK) detector, according to Bellcore 202 and V.23
•	•	•	•		•	Integrated fax/modem detection by Universal Tone Detection unit (UTD), In-band tone detection
•	•	•	•		•	Integrated Universal Tone Generator (UTG) including holwer tone and japanese tone generation
•	•	•	•		•	Call Progress Tone (CPT) Detector
•		•	•	•		Optimized filter structure for modem transmission, enhanced modem performance for improvement of V.90 transmission
•	•	•	•		•	Multi-party conferencing
•	•	•			•	3-Party conferencing via packet network
•	•	•	•	•	•	G.711
•	•	•			•	G.711 Annex I (Packet Loss Concealment), G.711 Annex II (VAD + CNG)
•	•	•	•		•	G.726 ADPCM
•	•				•	G.729 A, B
•	•				•	G.723.1
•	•				•	G.728, G.728 Annex I (Packet Loss Concealment)
•	•				•	G.729 E

**Table 2 VINETIC® Features (cont'd)**

VIP	CPE	M	C	S	0	VINETIC® Features
•	•				•	iLBC <sup>3)</sup>
•	•	•			•	Voice Activity Detection (VAD)
•	•	•			•	Comfort Noise Generation (CNG)
•	•	•	•		•	Algorithms for Line Echo Cancellation exceeding G.165, G.168, G.168-2000, G.168-2002: up to 128 ms tail length up to 16 ms tail length
•	•	•			•	Voice Play Out (reordering, fixed and adaptive jitter buffer, clock synchronization)
•	•				•	T.38 Fax Relay Support including all required datapump algorithms V.17, V.21, V.27ter, V.29
•	•				•	Text phone support V.18

**Codec/SLIC Features**

•	•	•	•	•		Worldwide programmability for AC and DC parameters
•	•	•	•	•		Specification in accordance with ITU-T Recommendation Q.552 for interface Z
•		•	•	•		Specification in accordance with ITU-T Recommendation G.712, and applicable LSSGR (GR-506/507 etc.), GR-57, EIA/TIA-464 and other applicable worldwide standards.
•	•	•	•	•		Integrated balanced/unbalanced ringing capability fully software programmable up to 85 Vrms ringing voltage, Crest-factor selection between 1.2 and 1.6, frequency range between 15 and 75 Hz
•		•	•	•		External ringing support
•		•	•	•		Programmable 12/16 kHz teletax generation (metering) and integrated notch filtering
•	•	•	•	•		Programmable battery feeding with capability for driving longer loops
•	•	•	•	•		Ground/loop start signaling
•		•	•	•		Ground key detection

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**Overview**
**Table 2 VINETIC® Features (cont'd)**

VIP	CPE	M	C	S	0	VINETIC® Features
•	•	•	•	•		Polarity reversal
•	•	•	•	•		Message Waiting Indication
•	•	•	•	•		Automatic modes for POTS signaling and Power Management
•	•	•	•	•		Advanced Integrated Test and Diagnostic Functions (AITDF) for local loop monitoring (including GR-909) and board production test capabilities.
•	•	•	•	•		On-hook transmission
•	•	•	•	•		Power optimized architecture with power management capability (integrated battery switches)
•		•	•	•	•	Part of ADSL IVD and IPVD solution
•	•	•	•	•		Direct connection of Clare Litelink III device

**Interface Features**

•	•	•	•	•	•	PCM/μC interface selectable
2	1	2	2	2	2	PCM interface (number of highways)
•	•	•	•	•	•	Parallel Host interface: Intel/Motorola compatible
•	•	•	•	•	•	Serial control interface, SCI (Infineon) compatible, SPI compatible
•	•	•	•	•		SLIC interface compatible with DuSLIC® SLICs
•	•	•	•	•	•	JTAG interface for boundary scan

**Available Packages<sup>4)</sup>**

•	•	•	•	•	•	P-LQFP-176
•	•	•	•	•	•	P-LBGA-176
	•	• <sup>5)</sup>	• <sup>6)</sup>	• <sup>6)</sup>		PG-LBGA-144



**Table 2 VINETIC® Features (cont'd)**

VIP	CPE	M	C	S	0	VINETIC® Features
<b>Additional Features</b>						
•	•	•	•	•	•	SW compatible between different VINETIC devices
•		•	•	•	•	HW compatible between different VINETIC devices
•	•	•	•	•	•	Driver and API for Linux and VxWorks

1) 8-channel devices in preparation

2) All VINETIC® devices up to version Version 1.4 include RAM for download

3) In preparation

4) Green Packages in preparation, contact local sales for details

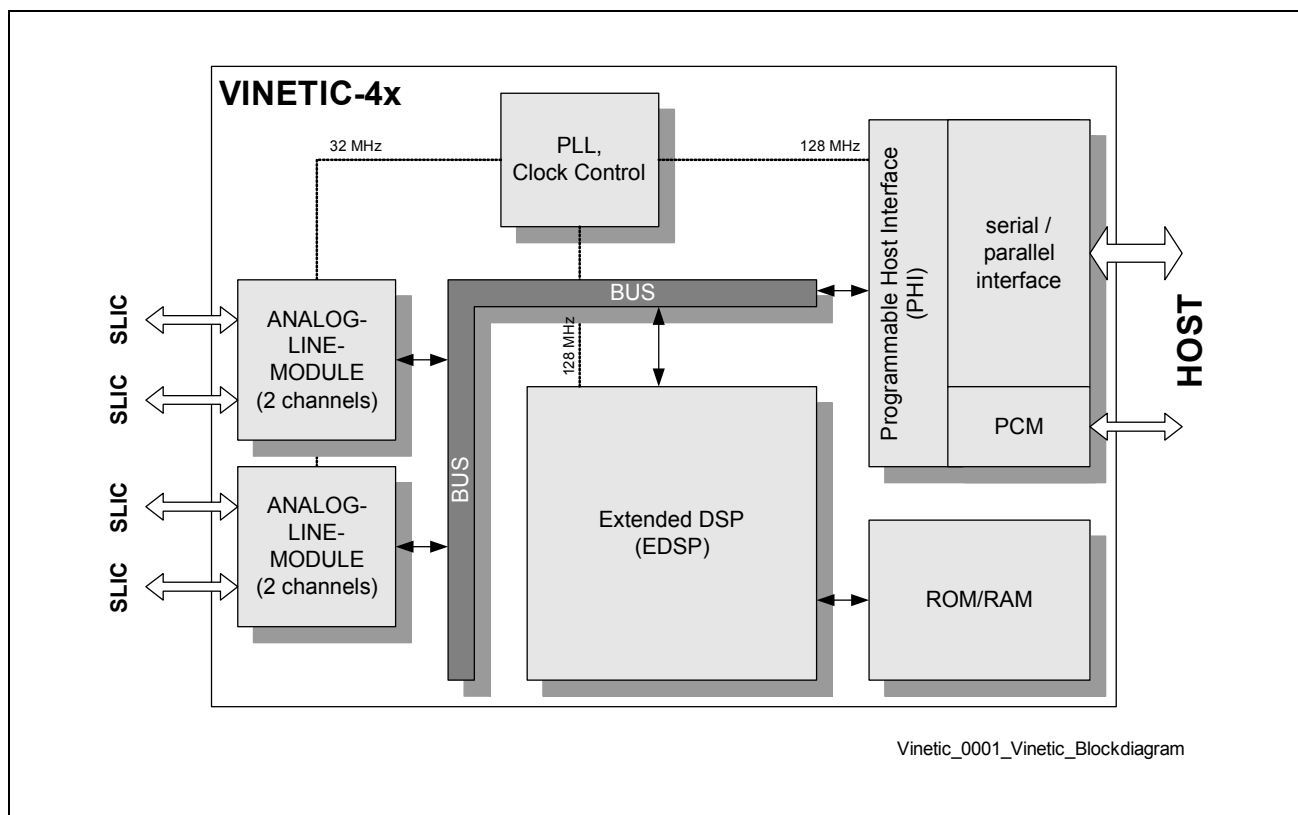
5) Only available for production from Version 2.1 onwards

The VINETIC®-x Version V1.4 firmware is available as a download file from Infineon in different builds. These different builds support different features, e.g. AAL2 or RTP support with different speech codecs. The mapping between firmware version and included feature is documented in the *Firmware Overview VINETIC® EDSP*.

## 2 VINETIC®-x Hardware Modules

### 2.1 Block Diagram VINETIC®-x

**Figure 1** shows the block diagram of VINETIC®-x with four analog channels. The main blocks of the VINETIC®-x are up to two Analog-Line-Modules (ALM, DCCTL), a powerful Enhanced Digital Signal Processor (EDSP), internal RAM and ROM and a Programmable Host Interface (PHI). The flexible internal bus (BUS) connects Analog-Line-Modules, EDSP and PHI.



**Figure 1** Block Diagram VINETIC®-x<sup>1)</sup>

The different blocks of the VINETIC®-x cannot be addressed directly. To access the different blocks, a flexible and hardware independent command structure is provided. Data transfer via the serial or parallel host interface is done via mail-boxes and with a special protocol (see flowcharts in **Figure 9 on Page 68**). Voice data which is transferred via the PCM interface is routed directly to/from the internal bus by the PHI. Control data and packetized voice data is directed to the mail-boxes.

<sup>1)</sup> VINETIC®-2VIP and VINETIC®-2CPE provide only one ALM with 2 channels.

**CONFIDENTIAL****VINETIC®-x Hardware Modules**

The VINETIC®-x chip provides the following setup and configuration possibilities for the different functional blocks:

**For ALM**

- Coefficient RAM (CRAM) download  
(see **“Download of Coefficient RAM (optional)” on Page 27**)
- ALM register configuration  
(see **“Register Accessed with SOP Commands (ALM)” on Page 101**, **“Registers Read with Short Commands (PHI, ALM and EDSP)” on Page 199**)
- optional: DCCTL program download  
(see **“Download of DCCTL Program Code (optional)” on Page 27**)

**For EDSP**

- Download of Program to EDSP Program and Data RAM  
(see **“Download of EDSP Firmware” on Page 26**)
- Configuration of Analog Line Interface Module, PCM Module, Signaling and Coder Software Modules (see *Preliminary User’s Manual - EDSP Firmware Description*)

**For PHI**

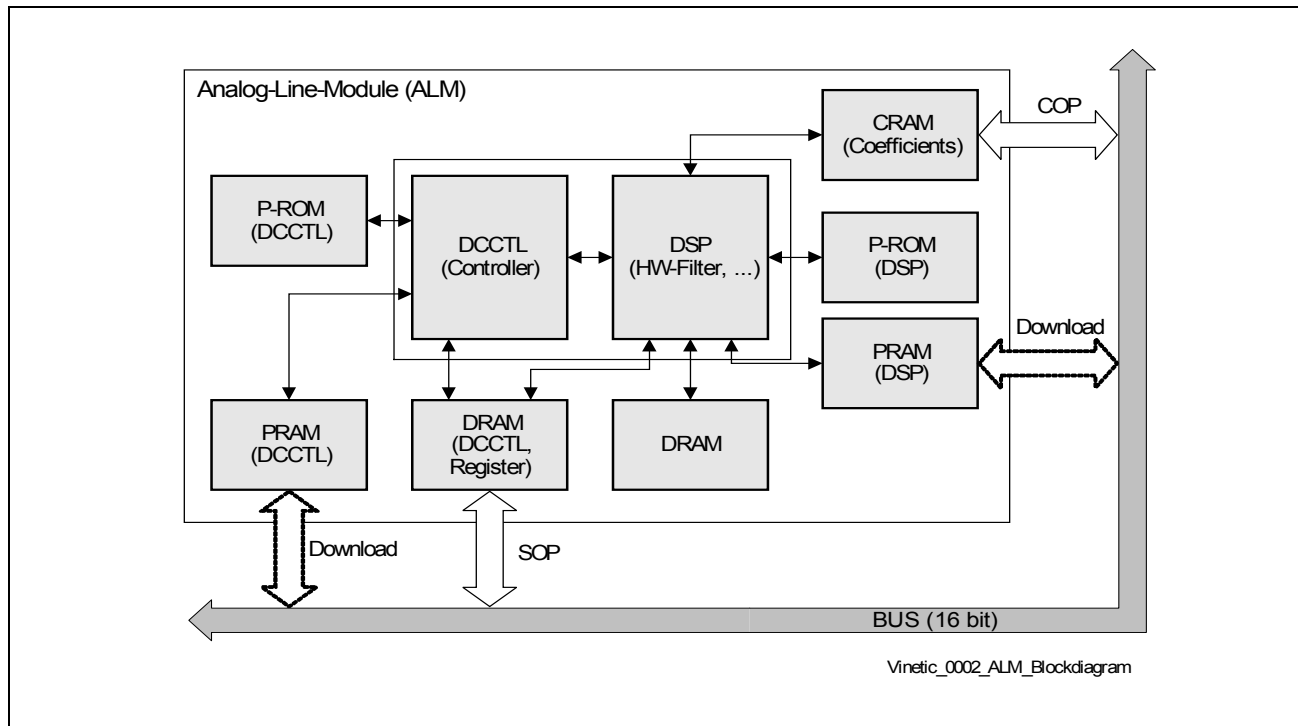
- register configuration  
(see **“Registers Read with Short Commands (PHI, ALM and EDSP)” on Page 199**, **“Register Accessed with IOP Commands (PHI)” on Page 160**, **“Common Registers” on Page 186** and **“Other PHI Related Registers” on Page 193**)
- optional: PHI program download  
(see **“Download of PHI Program Code” on Page 26**)

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**VINETIC®-x Hardware Modules**

## 2.2 Analog-Line-Module (ALM)

The following pages give an overview about the programming of the Analog-Line-Module.



**Figure 2 Block Diagram Analog-Line-Module (for Programmer's Purpose)**

The Analog-Line-Module contains a controller (DCCTL), a DSP, the coefficient RAM (CRAM), program ROMs (P-ROM DCCTL), program RAMs (PRAM DCCTL), and data RAMs (DRAM DCCTL) to enable a flexible adjustment to analog lines.

The CRAM contains all information to adjust the VINETIC®-x to country specific parameters. The coefficients can be computed with the VINETICOS tool, which enables an easy generation of the required coefficients. After generation, the coefficients can be written to the CRAM via COP (Coefficient OPERATION) commands.

Following parameters can be configured via COP commands (registers):

- Battery feed
- Ringing
- Signaling (supervision)
- Coding
- Hybrid for 2/4-wire conversion
- Testing
- Diagnostics

For detailed information concerning the different functions please refer to the *Preliminary User's Manual - System Reference*.



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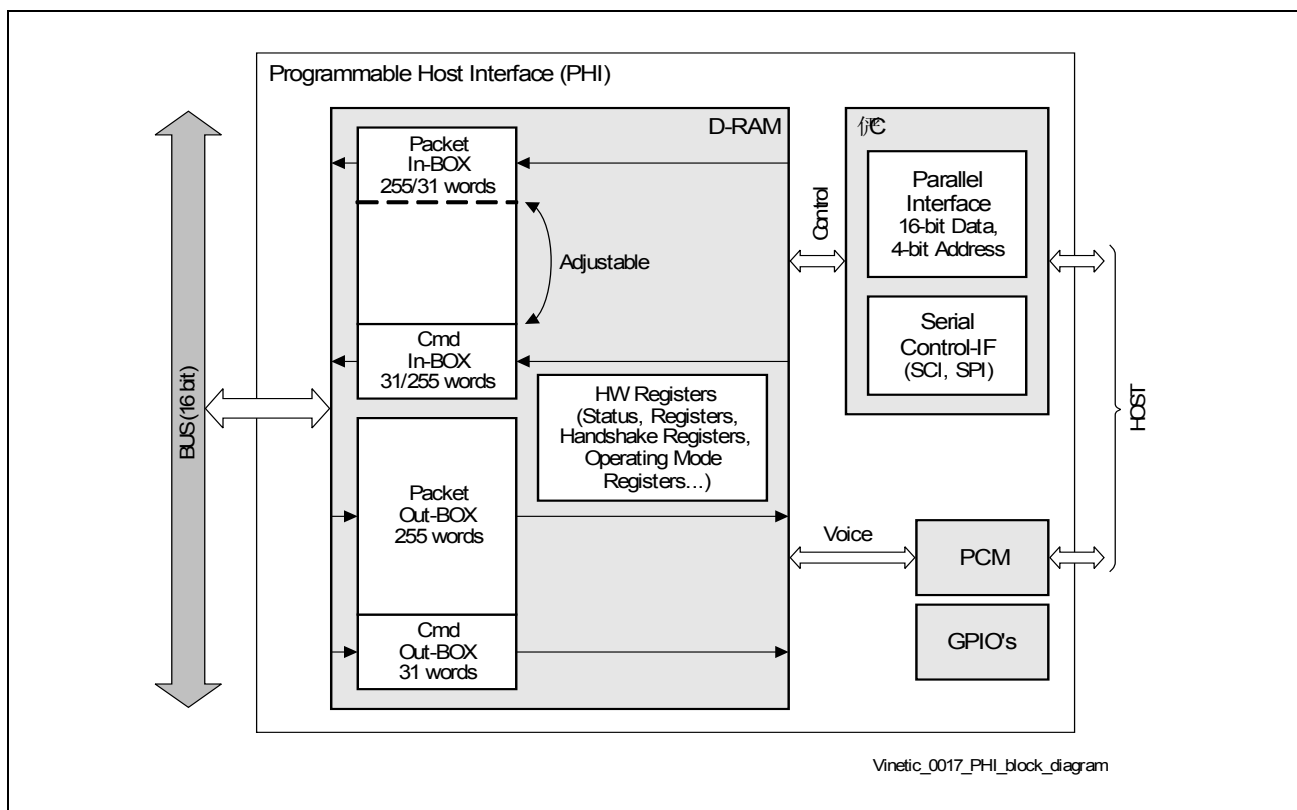
**VINETIC®-x Hardware Modules**

The command structure is described in [Chapter on Page 56](#). For coefficients and coefficient ranges which can be programmed with the VINETICOS tool see [Chapter 7.3 on Page 155](#).

The DCCTL DRAM contains registers for configuration of the Analog-Line-Module. Those registers (→ DRAM) can be accessed via SOP (Status OPeration) commands, which allow the addressing of the registers. SOP commands are described in [Chapter 7.2 on Page 101](#). They are transferred to the VINETIC®-x mail-box and the EDSP writes the data to the DCCTL DRAM. All registers which can be programmed via SOP commands are listed in [Table 16 on Page 96](#).

## 2.3 Programmable Host Interface (PHI)

The PHI includes a micro controller for handling data/command/packet transfer via the host interfaces. As the interface lines are also controlled by Software the PHI represents a very flexible solution. Changes in the interface can be done by software download.



**Figure 3 Programmable Host Interface (PHI)**

The PHI supports following parallel interfaces:

- 16-bit Motorola,
- 16-bit Intel (multiplexed and demultiplexed),
- 8-bit Motorola and
- 8-bit Intel (multiplexed and demultiplexed).

**CONFIDENTIAL****VINETIC®-x Hardware Modules**

The PHI supports two serial interfaces:

- PCM and
- SCI - a DuSLIC® compatible as well Motorola SPI slave mode compatible serial interface.

The PHI includes four mailboxes. Two mailboxes for commands in up- and downstream direction and two mailboxes for packets in up- and downstream direction. To optimize the speed during download activities it is possible to change the mailbox sizes of the command and packet boxes in downstream direction.

Data transferred from the host to the VINETIC®-x via the host interface are first interpreted by the PHI: Single word commands (= short commands) are processed by the PHI directly, packet data are transferred to the packet in-box and command data are transferred to the command in-box. In Upstream direction the data are stored in a command out-box or packet out-box respectively and an interrupt is generated to signal that data is ready for reading.

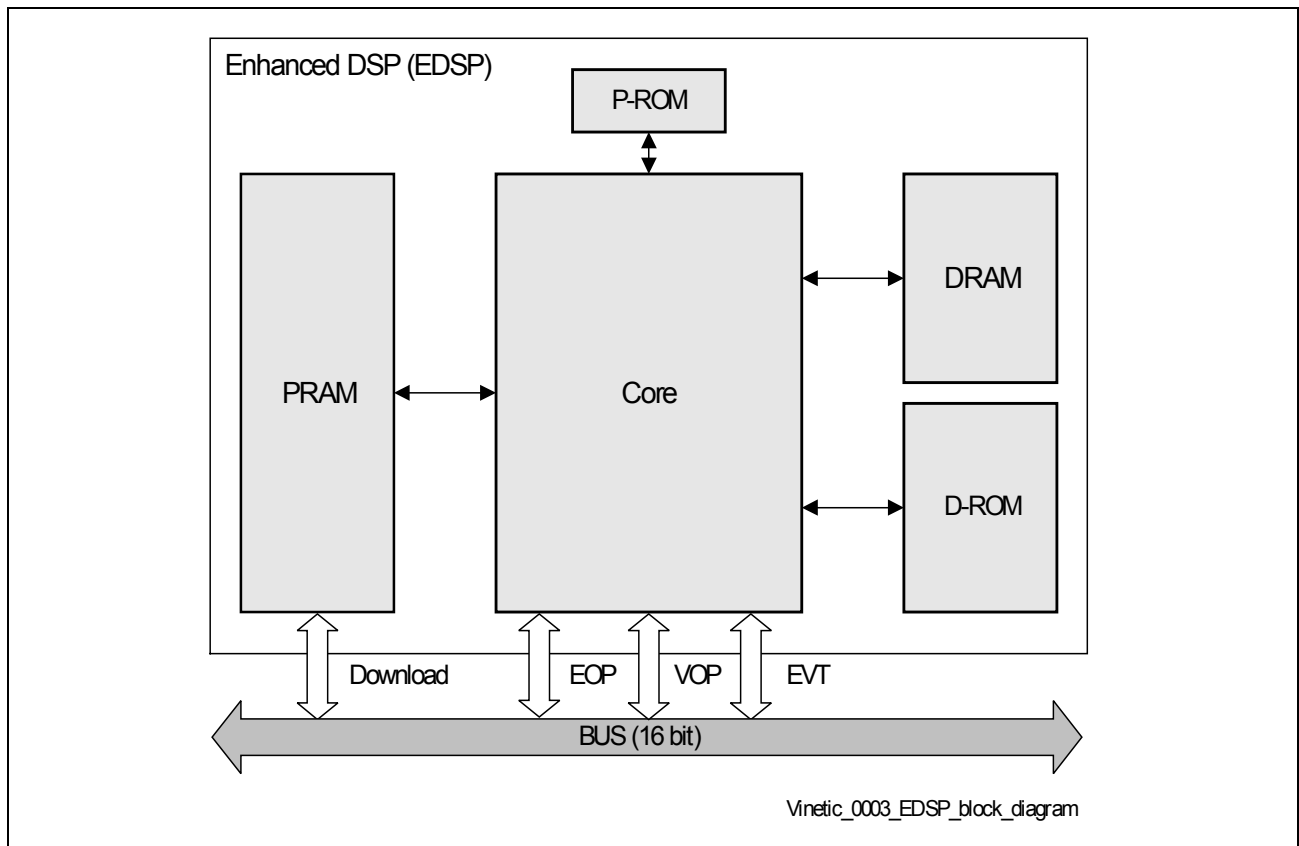
The PHI also includes HW-registers for interface handshake, status information, operating modes and other information. Status information and the handshake registers can be read via single word commands (short commands). A description of all possible short commands is given in **Table 5 on Page 50**. All other registers of the PHI can be configured via IOP commands.

A description of all registers which can be read via short commands or IOP commands is given in **Chapter 7 on Page 95**.

The VINETIC®-x has also a possibility to download a program to the program memory of the PHI. These feature allows fast bug fixes and/or feature enhancements.

## 2.4 Enhanced Digital Signal Processor (EDSP)

The following description gives a rough overview about the programming of the EDSP.



**Figure 4 Block Diagram EDSP (for Programmer's Purpose)**

As shown in **Figure 4** the EDSP has a program RAM (PRAM), a program ROM (P-ROM), a data RAM (DRAM), data ROM (D-ROM) and several internal HW units. The program for the EDSP has to be downloaded before the EDSP can be activated. This download procedure is described in **Chapter 3.2.1 on Page 26**.

The programming of voice connections and algorithms can be done via EOP commands. EOP commands consist of a two word header containing the information which and how much data should be written or read. They are transferred via the VINETIC®-x command mail-boxes. The structure of EOP commands is described in **Chapter 4 on Page 35**. All EOP commands are described in the *Preliminary User's Manual - EDSP Firmware Description*.

If a packetized voice connection has been established, the EDSP will process and transfer voice packets and status information. Voice packets are transferred via VOP commands. VOP commands have a two word header containing information about the following voice data, which have an additional header (RTP or AAL2) for itself. Some status information like DTMF tones can be transferred via EVT commands, which carry

**CONFIDENTIAL****VINETIC®-x Hardware Modules**

the DTMF information in the following data words. EVT commands have a two word header also. The EVT and VOP commands are described in [Chapter 4 on Page 35](#).

The firmware of the VINETIC®-x has a modular architecture, which allows a flexible programming of the VINETIC®-x. A detailed description of the firmware modules can be found in the *Preliminary User's Manual - EDSP Firmware Description*.

All features and algorithms which can be handled by the EDSP are shown in the feature list of [Table on Page 13](#).

## 3 Operational Description

### 3.1 Hardware Reset

A hardware reset of the VINETIC®-x is initiated by a power-on reset or by activating the RESETQ pin. A defined reset is generated if the RESETQ pin is set to low for at least 4  $\mu$ s and with the rising edge of the RESETQ signal all external clocks signals must be applied and have to be stable.

The internal reset routine will then initialize the entire chip to a default condition (see reset values for registers in [Chapter 7 on Page 95](#)). The completion of the internal reset routine is indicated by the RESET interrupt. After a hardware reset the RESET and MBX-EMPTY interrupt will be active in any case. Other interrupts can occur additionally. Before the host can continue with the firmware download all active interrupts have to be cleared.

After a reset the EDSP will stay in boot state, until the host sends the EDSP firmware. When the download is finished the EDSP has to be activated.

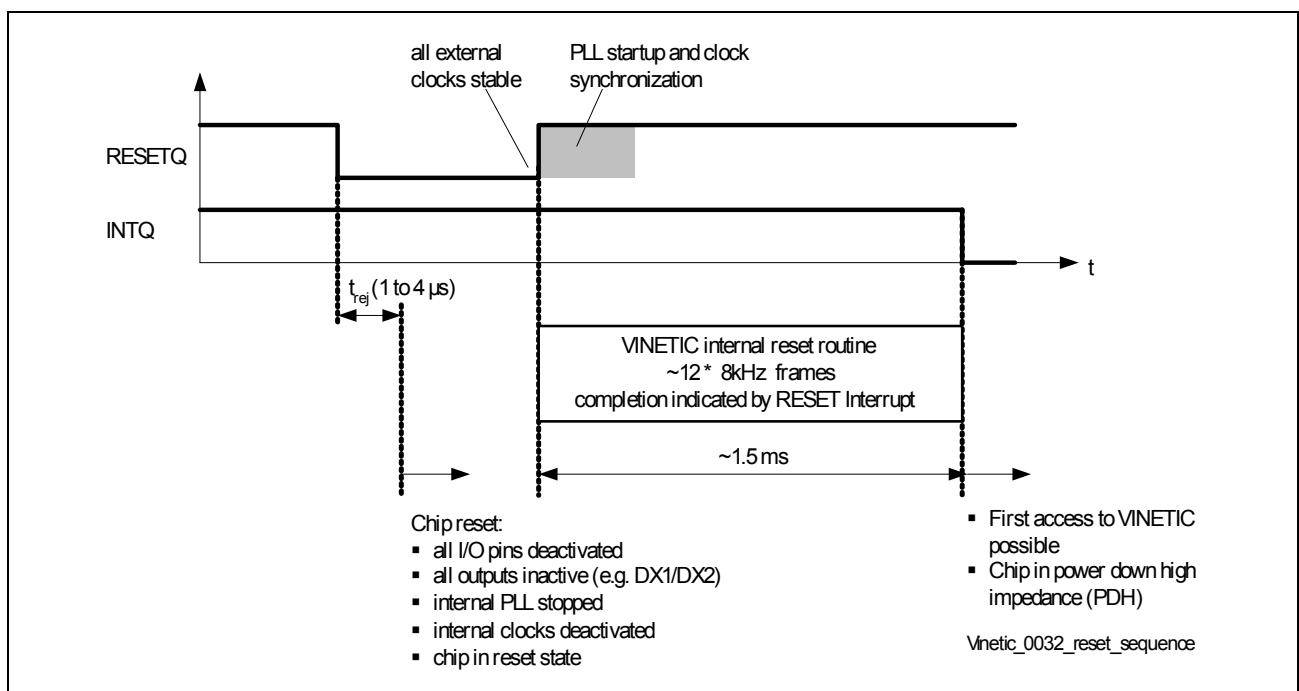


Figure 5 VINETIC® Reset Sequence

### 3.2 Boot

There is dedicated RAM area in the EDSP, the PHI and in both of the analog line modules (DCCTL), which allow downloading of micro program extensions (firmware). The PHI and the analog line modules also contain ROM memory.

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**Operational Description**

After reset VINETIC®-x supports Intel 16-bit Demultiplexed, Motorola 16-bit and Serial Microcontroller interface (SCI). In order to use an alternate Microcontroller interface, PHI micro program extensions have to be downloaded.

The EDSP ROM only contains a program code for the download function. All EDSP application functions are controlled completely by EDSP RAM. Therefore it is mandatory to download EDSP program code in order to get the specified functionality. The ROM of the analog line module covers completely the specified functionality. Downloading additional micro program code therefore is only necessary if the functions implemented in the ROM have to be corrected or supplemented.

Additional to the program ROM/RAM, the Analog Line Modules also contain RAM area for coefficients (CRAM = Coefficient RAM).

**Table 3 Overview VINETIC Download Functions**

PHI Program Code	optional
EDSP Firmware Download	mandatory
CRAM Coefficient Download	optional
DCCTL Program Code	optional <sup>1)</sup>

<sup>1)</sup> VINETIC®-x Version 1.4 devices requires an additional download for each of the Analog Line Modules. Details of the download are described in Application Note "VINETIC Download Functions".

As the EDSP is also involved in the internal data communication between the modules, it is also not possible to access the Analog Line module, the Signaling Module or the PCM Module prior to an EDSP program download.

*Note: A detailed description of the download procedure and checksum calculation for the EDSP, PHI, DCCTL DSP and Coefficient RAM is available on request in form of an application note.*

### 3.2.1 Download of EDSP Firmware

After a power on reset of the VINETIC®-x the program memory (PRAM) and data memory (DRAM) has to be downloaded. The commands SOP, EOP, IOP and COP which configure the VINETIC®-x functionality are only possible after a successful EDSP download and after the EDSP has been started with the short command wSTEDSP.

### 3.2.2 Download of PHI Program Code

The Programmable Host Interface (PHI) has 2 K words (28-bit width) program memory ROM and additional 2 K word (28-bit width) RAM for extension of the interface and control software.

**CONFIDENTIAL****Operational Description**

The following interfaces are available without a PHI micro program download:

- Intel 16-bit Demultiplexed,
- Motorola 16-bit,
- Serial Microcontroller interface (SCI)

Micro programs extension for the PHI are provided by Infineon and cover the following interfaces:

- Intel 16-Bit Multiplexed
- Intel 8-Bit Demultiplexed
- Motorola 8 Bit
- Intel 8-Bit Multiplexed

*Note: A PHI Download Versions Overview is available on request.*

### **3.2.3 Download of DCCTL Program Code (optional)**

The VINETIC®-x with four channels includes two Analog Line Modules ALM (each with two POTS channels). Two channel devices (VINETIC®-2VIP and VINETIC®-2CPE) provide only one Analog Line Module. The control function of the analog channel is handled by an additional internal DSP. Program code for this DSP is hard coded in ROM. Additional to the ROM, there is also a RAM memory. By downloading program code, the ROM based functions of the ALM can be modified and supplemented. For normal operation, it is not necessary to download code into the DCCTL RAM. All standard functions of the ALM described in the VINETIC®-x data sheet, can be run from the DCCTL ROM. DCCTL DSP micro programs extensions are provided by Infineon.

*Note: In order to support SLIC-LCP a download of a DCCTL DSP micro program extension is necessary.*

### **3.2.4 Download of Coefficient RAM (optional)**

A download of the Coefficient RAM is necessary if country specific POTS requirements must be fulfilled. The download is done via COP commands. For detailed information refer to [Chapter 7.3 on Page 155](#).

## **3.3 Software Reset**

When performing a software reset (short command wSWRST), the VINETIC®-x sets the default settings of the configuration registers in the ALM (SOP registers). The software reset can be executed independently for each Analog Line Module channel. In this case the Analog Line Module for this channel, but not the EDSP, is reset. If the broadcast (BC) bit is set also the EDSP will be reset. The program memory of the EDSP is not cleared by this reset, so a new download is not necessary. Of course all coefficients in the D-RAM of the EDSP are set to the default values by a software reset.



*Note: The PHI registers and settings, that are accessible by IOP commands and short commands, are not reset with the wSWRST command. So after a software reset the operating mode is not reset to power down high impedance (PDH). To be sure to start in this mode after reset, this mode must be programmed for that channel before the wSWRST command.*

### 3.4 Watchdog

The EDSP is checked by a software watchdog in the PHI. The EDSP must send a toggling signal to this watchdog. If the EDSP doesn't send this signal within 64 ms the PHI will initiate a HW reset of the EDSP system and provide an interrupt to the host. The default setting for the watchdog is watchdog off. After a reset or a wLEMP command the watchdog is disabled and has to be enabled by setting the WDG-EN bit in the GCONF register.

### 3.5 Test Modes of the VINETIC®-x

The VINETIC®-x can be set to different production and analysis tests. All production tests are reserved and gated by the pin TEST which should be tied low all time during normal operation. In order to support boundary scan test a JTAG (IEEE 1149.1) interface is implemented.

### 3.6 Interrupt Handling

The VINETIC®-x can signal status changes via an interrupt to the host. The different status bits (indicate the state of PHI, ALM modules and EDSP software) are stored in status registers. The interrupt structure of VINETIC®-x is shown in [Figure 6](#). For interrupt generation four different register types are relevant:

#### 1. Status Register (HWSR1/2, BXSr1/2, SRGPIO, SRS1/2, SRE1/2)

These register indicate the current hardware status. An update of the current status is done every 0.5 ms. A description is given in [Chapter 7.5.1 on Page 199](#). Depending on the Values of the **Mask Registers** a rising (0 → 1 transition) and/or falling (1 → 0 transition) can cause an interrupt. In polling mode (all interrupts are masked) it is possible to determine the chip status by periodically reading out these registers.

#### 2. Mask Register

(MF-HWSR1/2, MR-HWSR1/2, MF-BXSr1/2, MR-BXSr1/2, MF-SRGPIO, MR-SRGPIO, MF-SRS1/2, MR-SRS1/2, MF-SRE1/2, MR-SRE1/2)

For each **Status Register** there exist two **Mask Register**. One register enables the interrupt generation on the rising edge (MR-xxxx register), the other register (MF-xxxx register) enables the generation of interrupts on the falling edge. If both possibilities are disabled, no interrupt is generated (no indication on the INTQ line, in the **Interrupt Register** and in the **Interrupt Status Register**). If both possibilities are enabled, an

interrupt is generated on every change of the related bit. The registers are described in [Chapter 7.4 on Page 160](#). After reset the SYNC-FAIL, HW-ERR, MCLK-FAIL, DL-RDY, RESET and all mailbox related interrupts are enabled, all other interrupts are disabled. Recommended Values for the **Mask Registers** are given in [Chapter 7.4.2 on Page 185](#)

### 3. Interrupt Status Register

(I-HWSR1/2, I-BXSR1/2, I-SRGPIO, I-SRS1/2, I-SRE1/2)

If a bit in a **Status Register** changes an interrupt will be issued according to the setting of the **Mask Register**. Thus, if the status bit is not masked the corresponding bit in the **Interrupt Status Register** is set to “1” and the INTQ line is activated. All interrupt sources are collected until a read access to these registers is done. After a read access with the corresponding short command the content is reset to 0000<sub>H</sub> and the INTQ pin is set inactive. The registers are described in [Chapter 7.5.3 on Page 228](#).

If a status bit issues an interrupt only on a rising **or** falling edge, it is sufficient to read out the **Interrupt Status Register** in order to get the actual value of the status bit after an interrupt. For status bits that issue an interrupt on rising **and** falling edge the corresponding **Status Register** also must be read out in order to determine the actual value of the corresponding status.

### 4. Interrupt Register (IR)

This register indicates which **Interrupt Status Register** caused the interrupt. Reading the **Interrupt Register** with short command rIR will clear the INTQ line. The subsequent reading of the corresponding **Interrupt Status Registers** will reset the bits in the **Interrupt Register**.

Exception for resetting Interrupt Register (IR):

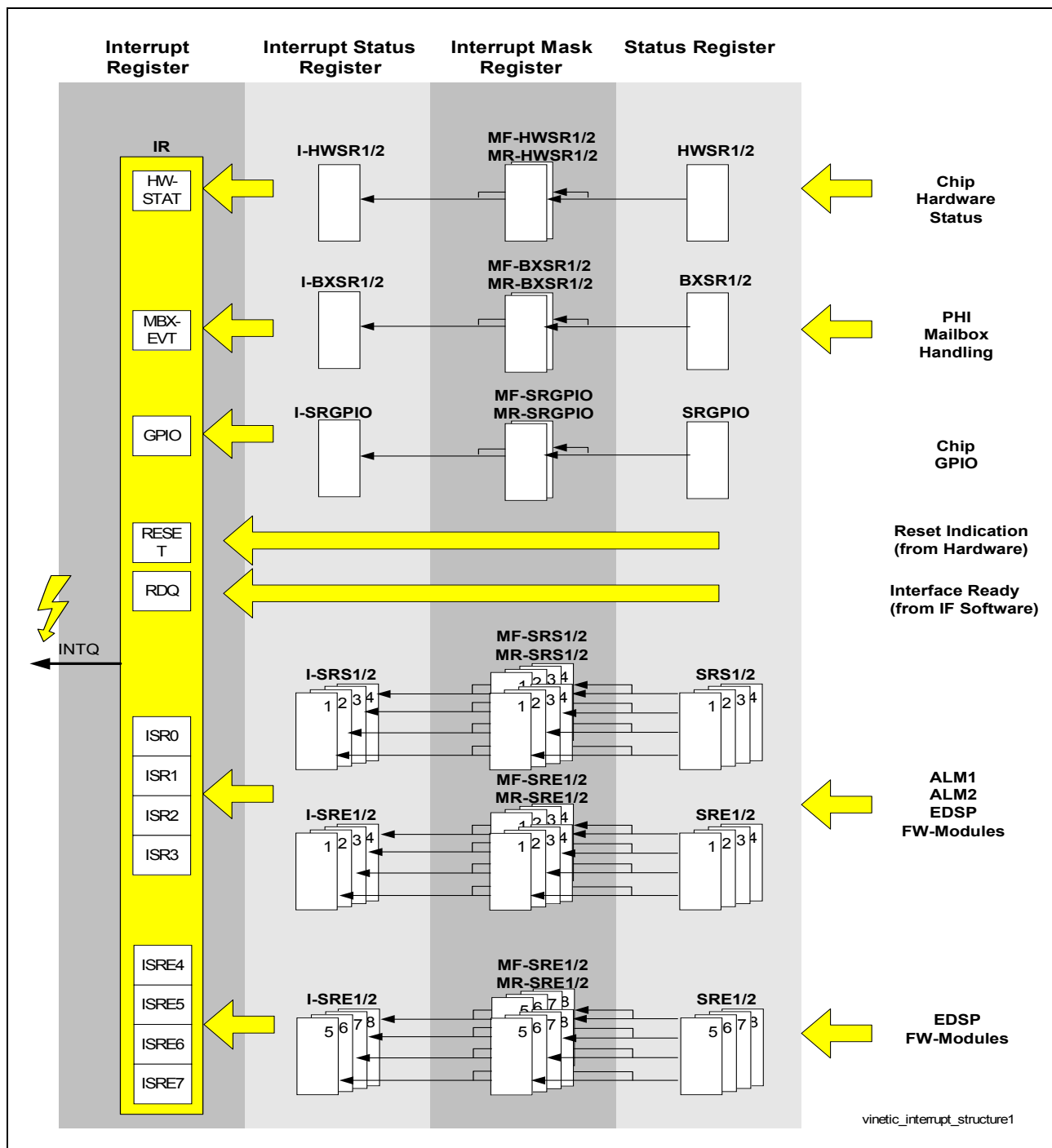
- The **RESET bit** is cleared immediately with reading of the Interrupt Register by short command rIR. No subsequent reading of an Interrupt Status Register is necessary.

*Note: The RESET bit will not be cleared by reading the Interrupt Register via direct interrupt register access (DIA). DIA should only be used to access the RDYQ bit for SW handshaking!*

- Any change of **RDYQ bit** does not cause an interrupt. The RDYQ bit indicates if VINETIC®-x is ready for the next access (8 bit or 16 bit) via the host interface. For software handshaking the actual state of the RDYQ bit can only be accessed via direct interrupt register access (DIA) or via the RDYQ pin.

*Note: When reading the Interrupt Register with short command rIR the RDYQ bit will always reflect a “0”.*

A description of this register is given in [Chapter 7.5.1 on Page 199](#).



**Figure 6** Interrupt Structure of VINETIC®-x

Independent of the selected interface mode, the general behavior of the interrupt is as follows (if the interrupt isn't disabled):

- A change of any bit in one of the Status Registers (depending on the Interrupt Mask Registers) leads to the setting of the corresponding bit in the Interrupt Status Register, to the setting of the corresponding bit in the IR and thus to an interrupt.

**CONFIDENTIAL****Operational Description**

- All changes that generate an interrupt are collected in the Interrupt Status Registers. The interrupt line (INTQ) is drawn to zero (active low) to signal that an interrupt is pending.
- The interrupt bit in the IR is cleared by reading all associated Interrupt Status Registers of the corresponding IR status bit. Since for the RESET bit there is no corresponding Interrupt Status Register, a read access via the short command rIR clears the RESET bit and deactivates the INTQ line.

The interrupt behavior of the different blocks in VINETIC®-x are described below:

**Analog-Line-Modules Channels**

A change of any status bit in the status registers of the Analog-Line-Module Channel (SRS1, SRS2) leads to an interrupt. Which channel caused the interrupt is indicated by the bits ISR0..ISR3 (channel 0..3) of the interrupt register. In order to clear the interrupts bits ISR0..ISR3 the interrupt status registers I-SRS1 and I-SRS2 of the corresponding channel have to be read.

**Signaling Module and Coder Modules of EDSP**

A change of any status bit in the status registers of the EDSP (SRE1, SRE2) leads to an interrupt. The status registers reflect the status of the Signaling-Module and Coder-Module of the EDSP. Which channel caused the interrupt is indicated by the bits ISR0..ISR3 (channel 0..3) and ISRE4..ISRE7 (channel 4..7) of the interrupt register. In order to clear the interrupt bits ISR0..ISR3 (channel 0..3) the interrupt status registers I-SRE1, I-SRE2, I-SRS1 and I-SRS2 of the corresponding channel have to be read.

In order to clear the interrupts bits ISRE4..ISRE7 (channel 4..7) the interrupt status registers I-SRE1, I-SRE2 of the corresponding channel have to be read.

**General Purpose IO Pins**

A change of any status bit in the GPIO status register (SRGPIO) leads to an interrupt. The GPIO bit in the IR is set. The corresponding bits for the status change in I-SRGPIO are set. The GPIO bit in the IR is cleared after the host has read I-SRGPIO.

**Mailboxes**

A change of any status bit in the mailbox status registers (BXSR1, BXSR2) leads to an interrupt. The MBX-EVT bit in the IR is set. The corresponding bits for the status change in I-BXSR1 and I-BXSR2 are set. The MBX-EVT bit in the IR is cleared after the host has read I-BXSR1 and I-BXSR2.

**Hardware Status**

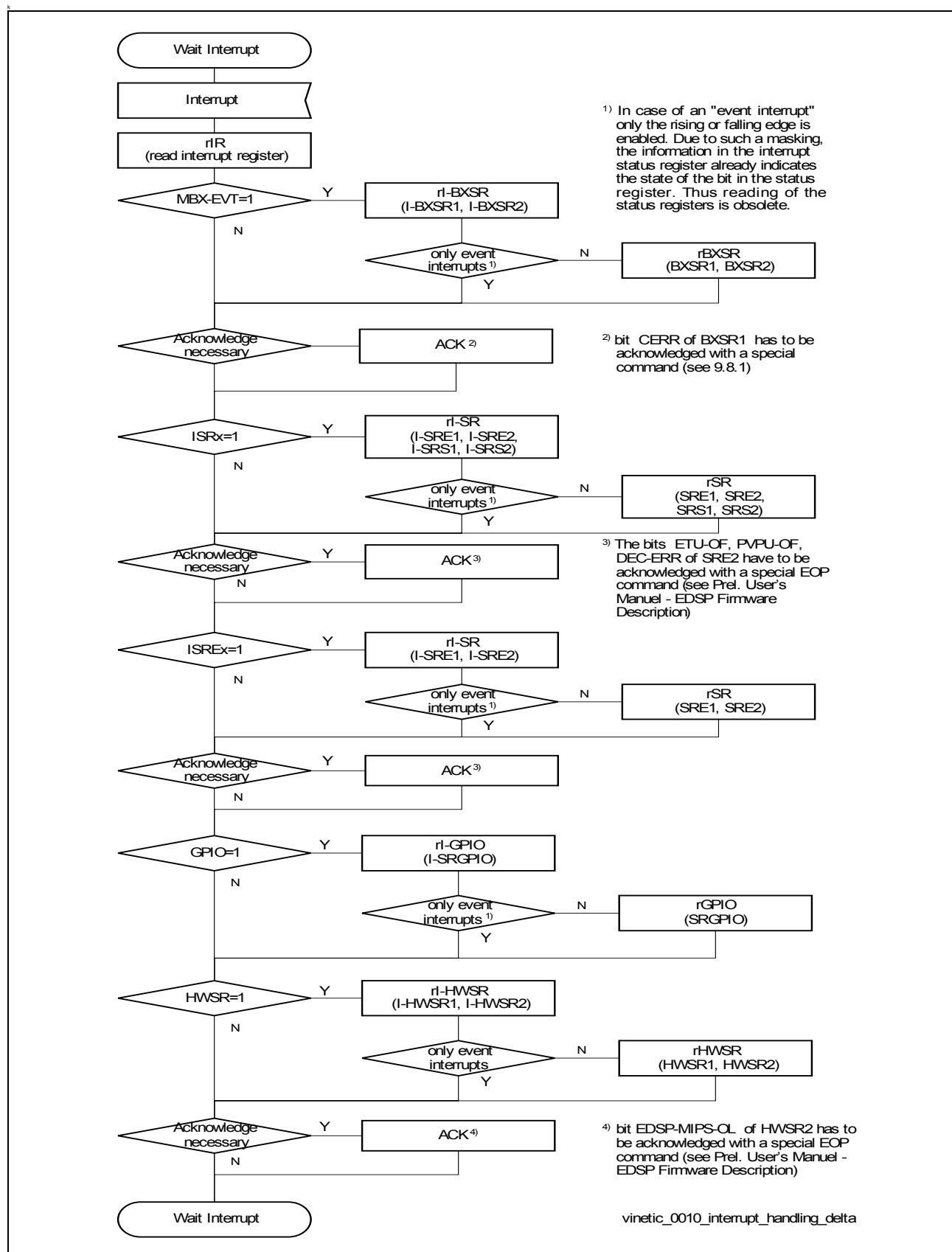
A change of any status bit in the hardware status registers (HWSR1, HWSR2) leads to an interrupt. The HW-STAT bit in the IR is set. The corresponding bits for the status

change in I-HWSR1 and I-HWSR2 are set. The HW-STAT bit in the IR is cleared after the host has read I- HWSR1 and I-HWSR2.

### **Power On Reset**

A hardware or power-on reset of the chip clears all pending interrupts and resets the interrupt line (INTQ pin) to inactive. After the VINETIC®-x internal reset routine is finished, the RESET bit in the IR register is set and the interrupt line is set to active (low). A similar behavior is shown after a software reset of all channels, the interrupt line switches to non-active within 500 µs. A software reset of one channel deactivates the interrupt signal if there is no active interrupt on the other channels.

**Figure 7 on Page 33** shows a possible host flowchart for reading the interrupts. The used short commands rIR, rSR, rHWSR, rSRGPIO, rBXSR, rl-SR, rl-HWSR, rl-SRGPIO and rl-BXSR are described in **Table 5 on Page 50**. The bit names of the IR (ISREx, ISRx, GPIO, MBX-EVT, HW-STAT) and the registers (IR, SRE1, SRE2, SRS1, SRS2, HWSR1, HWSR2, BXSR1, BXSR2, SRGPIO, I-SRE1, I-SRE2, I-SRS1, I-SRS2, I-HWSR1, I-HWSR2, I-BXSR1, I-BXSR2, I-SRGPIO) are described in **Chapter 7**.

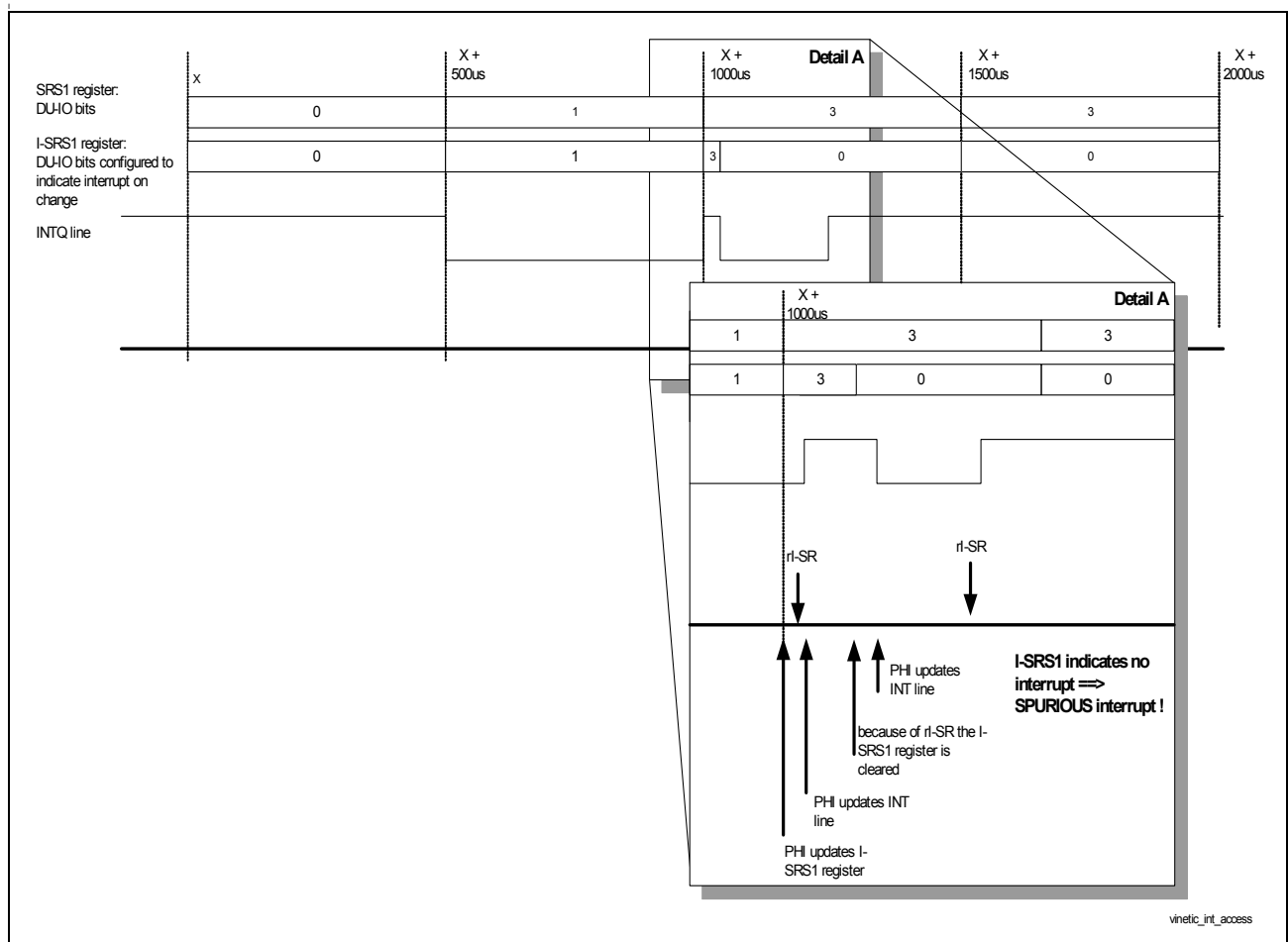


**Figure 7 Interrupt Handling of VINETIC®-x**

## VINETIC® Interrupt Handling and Spurious Interrupt

The interrupt information is generated and updated every 500  $\mu$ s. The new values for the interrupt status registers and the new state of the interrupt line is generated by the internal PHI software. Since this can be interrupted by an external access to the interrupt status registers, a situation like depicted in **Figure 8** may happen. In these rare cases, no information is lost, but an interrupt that does not have any information (spurious interrupt) may be generated.

*Note: DU-IO in **Figure 8** are shown as examples, but applies to all other interrupt sources.*



**Figure 8 Spurious Interrupt**



## 4 Command/Data Structure

To address the different parts of the VINETIC®-x chip a flexible, hardware independent command structure is used.

All commands are usable with the different types of interfaces (parallel or serial).

Big/little Endian Control is supported for data packet transmission (VOP and EVT-command). The first and second command word are not affected by the big/little endian setting only the MSB and LSB ordering of the following words is swapped if little endian is selected.

This chapter does not cover the detailed handling of the interface and mailboxes, which has to be obeyed in order to write respectively read data to/from VINETIC®-x. For information on interfaces and mailboxes see [“Interface Description” on Page 83](#)

*Note:*

- 1. The Big/Little Endian Control does not have any effect on any of the command words of SOP, COP, IOP and EOP commands. Thus those commands have always to be sent as specified!*
- 2. Within this document in all diagrams, figures, tables and inside the text the big endian format is used, which is the default configuration. For more information please refer to the Preliminary User's Manual - EDSP Firmware Description.*

### 4.1 Command/Data Structure Overview in Downstream Direction

The detailed bit description of the command structure is shown in [Chapter 4.3 on Page 46](#) and following.

Each command consists either of one single command word, or of two command words followed by data. The first command word contains information about the read/write status, the type of the command/mode and the used channel. The second command word defines length and destination (or source respectively) for control data or in case of packet data only the length information. Four different command types can be distinguished:

- Packets
- Read/Write Commands for Register Access
- Read/Write Commands for EDSP Operation
- Short Commands

#### 4.1.1 Packets [M-V, CPE]

Packets are indicated by a voice packet operation identifier (VOP) or a packet based event transmission operation identifier (EVT) within the CMD-bits of the first command word (see [Table 4 on Page 49](#)). The R/W-bit (bit 15) is set to zero and the “channel” field contains the channel information. The second command word includes the number of

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following data words and the information if there are even or odd number of bytes in the packet.

**Write Command**

**From the Host**

1 <sup>st</sup>	First Command
2 <sup>nd</sup>	Second Command
1	Data_1
2	Data_2
	...
n	Data_n

**First Command**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	0	0	VOP/EVT					Res				CHAN			

**Second Command**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res		ODD	Res					LENGTH							

*Note: CHAN ... Channel*  
*Res ... Reserved*  
*ODD ... Even or odd number of bytes in packet*  
*LENGTH ... Number of following data words*  
*R/W ... Read or write command*

**4.1.2 Read/Write Commands for Register Access**

There are three types of read/write commands (depending on the HW-module which should be addressed) which are differentiated within the CMD-bits of the first command word (see also [Table 4 on Page 49](#)):

- status operation (SOP) commands provides access to configuration and status register of the Analog-Line-Modules.
- coefficient operation (COP) commands enables the configuration of the coefficient registers of the Analog-Line-Modules.

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c. Interface operation (IOP) commands are needed to set all registers related to the Programmable Host Interface (PHI).

The first command word contains read/write (bit 15), broadcast (bit 13 - is zero in case of read commands) and channel information also. The second command word includes the offset of the register address and the number of following data words

**Read/Write Command**
**From the Host**

1 <sup>st</sup>	First Command
2 <sup>nd</sup>	Second Command
1	Data_1 (only write commands)
2	Data_2 (only write commands)
	...
n	Data_n (only write commands)

**First Command**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>R/W</b>	<b>0</b>	<b>BC</b>	<b>SOP/COP/IOP</b>					<b>Res</b>				<b>CHAN</b>			

**Second Command**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>OFFSET</b>								<b>LENGTH</b>							

*Note: CHAN ... Channel*  
*Res ... Reserved*  
*BC ... Broadcast*  
*LENGTH ... Number of following data words*  
*OFFSET ... Address offset for the register*  
*R/W ... Read or write command*

**4.1.3 Read/Write Commands for EDSP Operation**

EDSP operations are indicated by a EDSP operation command identifier (EOP) within the CMD-bits of the first command word (see [Table 4 on Page 49](#)). The first command word contains read/write (bit 15), broadcast (bit 13 - is zero in case of read commands)

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and channel information also. The second command word includes information about the SW-module which should be addressed, the command and the length of the following data.

*Note: With VINETIC®-4S only few of the EOP commands are supported (see Firmware Overview EDSP)*

**Read/Write Command**
**From the Host**

1 <sup>st</sup>	First Command
2 <sup>nd</sup>	Second Command
1	Data_1 (only write commands)
2	Data_2 (only write commands)
...	...
n	Data_n (only write commands)

**First Command**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	0	BC	EOP					Res				CHAN			

**Second Command**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOD			ECMD					LENGTH							

*Note: CHAN ...*      *Channel*  
*Res ...*            *Reserved*  
*LENGTH ...*      *Number of following data words*  
*ECMD ...*        *EDSP command*  
*MOD ...*        *Addressed module or resource command*  
*R/W ...*         *Read or write command*

**4.1.4 Short Commands**

Short commands consist of the first command word only (exception: the optional wLPMP command). They are indicated with the SC-bit (bit 14) in the first command word (see

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**Table 5 on Page 50**). The first command word contains read/write (bit 15), broadcast (bit 13) and channel information also.

**Read/Write Command**

**From the Host**

1<sup>st</sup>

First Command
---------------

**First Command**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	1	BC	Command or Operating State									CHAN			

*Note: CHAN ... Channel*  
*BC ... Broadcast*  
*R/W ... Read or write command*

*The short command bit (SC) is always set to 1 for short commands.*

## 4.2 Command/Data Structure Overview in Upstream Direction

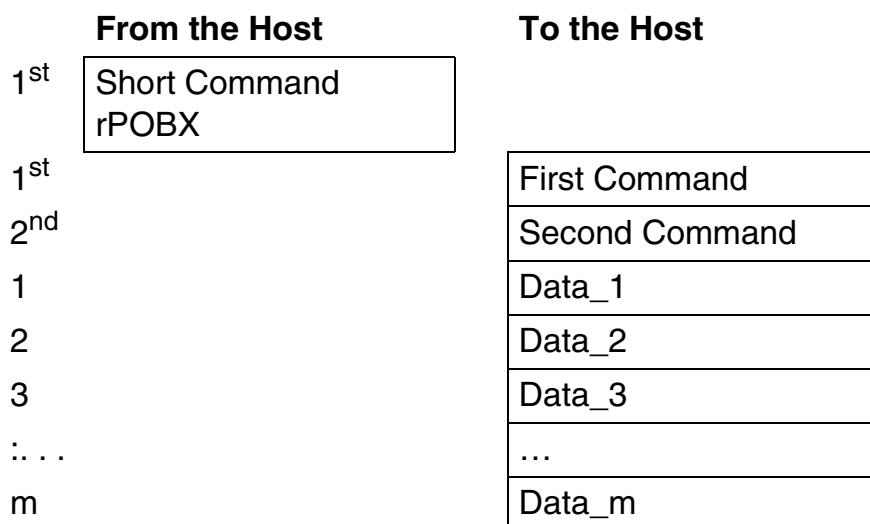
The detailed bit description of the command structure is shown in [Chapter 4.3 on Page 46](#) and following. Data in upstream direction is transferred to the command or packet out-box by the EDSP and is read from there by the host via short commands. In upstream direction also four different data types can be distinguished:

- Packets
- Responses to Read Commands for Register Access
- Responses to Read Commands for EDSP Operation
- Responses to short commands

### 4.2.1 Packets [M-V-CPE]

Packets in upstream direction have the same command structure as packets in downstream direction but the R/W-bit of the first command word is set. The SC-bit is always cleared, the CMD-bits indicate a voice packet operation (VOP) or a packet based event transmission operation (EVT) and the CHAN-bits specify the corresponding channel. The second word includes the number of following data words and the information if there are even or odd number of bytes in the packet.

#### Read Command



#### First Command

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	VOP/EVT					Res			CHAN				

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**Second Command**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Res</b>		<b>ODD</b>	<b>Res</b>					<b>LENGTH</b>							

**4.2.2 Responses to Read Commands for Register Access**

Responses to read commands for register access start with the copy of the corresponding read command (first and second command word) sent by the host, followed by the requested data. The response to the host, can be read via a polling or interrupt routine for details on this procedures see [Figure 15 on Page 77](#).

**Read Command**

<b>From the Host</b>		<b>To the Host</b>	
1 <sup>st</sup>	First Command	1 <sup>st</sup>	First Command
2 <sup>nd</sup>	Second Command	2 <sup>nd</sup>	Second Command
1		1	Data_1
2		2	Data_2
3		3	Data_3
...		...	...
n		n	Data_n

**First Command**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>1</b>	<b>0</b>	<b>0</b>	<b>SOP/COP/IOP</b>					<b>Res</b>			<b>CHAN</b>				

**Second Command**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>OFFSET</b>								<b>LENGTH</b>							



### 4.2.3 Responses to Read Commands for EDSP Operation

Responses to read commands for EDSP operation start with the copy of the corresponding read command (first and second command word), which were sent by the host, followed by the requested data. The response to the host, can be read via a polling or interrupt routine for details on this procedures see [Figure 15 on Page 77](#).

*Note: With VINETIC®-4S only few of the EOP commands are supported (see EOP commands)*

#### Read Command

	From the Host	To the Host
1 <sup>st</sup>	First Command	First Command
2 <sup>nd</sup>	Second Command	Second Command
1 <sup>st</sup>		Data_1
2 <sup>nd</sup>		Data_2
1		Data_3
2		...
3		Data_n
...		
n		

#### First Command

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	EOP					Res				CHAN			

#### Second Command

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOD			ECMD					LENGTH							

### 4.2.4 Responses to Short Commands

Responses to short commands do not start with the command header, because they will be provided within a given command recovery time (see also the timing specifications in the *Preliminary Data Sheet*).

### Read Command general

	From the Host	To the Host
1 <sup>st</sup>	Short Command	
1		Data_1
2		Data_2
3		Data_3
...		...
n		Data_n

### Read Interrupt Status Registers for channel 0..3

	From the Host	To the Host
1 <sup>st</sup>	rl-SR chan= [0..3]	
1		I-SRE1
2		I-SRE2
3		I-SRS1
4		I-SRS2

### Read Interrupt Status Registers for channel 4..7

	From the Host	To the Host
1 <sup>st</sup>	rl-SR chan= [4..7]	
1		I-SRE1
2		I-SRE2

### Read Interrupt Status Register for all channels

	From the Host	To the Host
1 <sup>st</sup>	rl-SR BC=1	
1		I-SRE1 (channel 0)
2		I-SRE2 (channel 0)
3		I-SRS1 (channel 0)
4		I-SRS2 (channel 0)
5		I-SRE1 (channel 1)

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6	I-SRE2 (channel 1)
7	I-SRS1 (channel 1)
8	I-SRS2 (channel 1)
9	I-SRE1 (channel 2)
10	I-SRE2 (channel 2)
11	I-SRS1 (channel 2)
12	I-SRS2 (channel 2)
13	I-SRE1 (channel 3)
14	I-SRE2 (channel 3)
15	I-SRS1 (channel 3)
16	I-SRS2 (channel 3)
17	I-SRE1 (channel 4)
18	I-SRE2 (channel 4)
19	I-SRE1 (channel 5)
20	I-SRE2 (channel 5)
21	I-SRE1 (channel 6)
22	I-SRE2 (channel 6)
23	I-SRE1 (channel 7)
24	I-SRE2 (channel 7)

*Note: With the Short command rl-SR and BC=1 VINETIC®-2VIP and VINETIC®-2CPE Version 1.4 will return the status registers (I-SRS1,I-SRS2) for analog line channel 2 and 3 and channel 4-7 (I-SRE1,I-SRE2) with invalid data.*

**Read Interrupt Status Registers for ALM channel 0..3**

	<b>From the Host</b>	<b>To the Host</b>
1 <sup>st</sup>	rl-SRS chan= [0..3]	
1		I-SRS1
2		I-SRS2

**Read Interrupt Status Registers for all ALM channels**

	<b>From the Host</b>	<b>To the Host</b>
1 <sup>st</sup>	rl-SRS BC=1	
3		I-SRS1 (channel 0)
4		I-SRS2 (channel 0)
7		I-SRS1 (channel 1)
8		I-SRS2 (channel 1)
11		I-SRS1 (channel 2)
12		I-SRS2 (channel 2)
15		I-SRS1 (channel 3)
16		I-SRS2 (channel 3)

*Note: With the Short command rl-SRS and BC=1 VINETIC®-2VIP and VINETIC®-2CPE Version 1.4 will return the status registers (I-SRS1,I-SRS2) for analog line channel 2 and 3 with invalid data.*

**rl-HWSR**

**Read Interrupt Hardware Status Register**

	<b>From the Host</b>	<b>To the Host</b>
1 <sup>st</sup>	rl-HWSR	
1		I-HWSR1
2		I-HWSR2

**rl-BXSR**

**Read Mailbox Interrupt Status Register**

	<b>From the Host</b>	<b>To the Host</b>
1 <sup>st</sup>	rl-BXSR	
1		I-BXSR1
2		I-BXSR2

The order of registers returned to the short commands rSR, rSRS, rHWSR and rBXSR is the same as with short commands rl-SR, rl-SRS, rl-HWSR and rl-BXSR.

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**Command/Data Structure**
**4.3 First Command Word**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	SC	BC	CMD					SUBCMD				CHAN			

Field	Bits	Description
R/W	15	<b>Read/Write bit</b> 0 Write data to chip 1 Read data from chip
SC	14	<b>Short Command bit</b> 0 The CMD[4:0] bits are interpreted as one of the commands shown in <a href="#">Table 4 on Page 49</a> 1 No further words are expected and the CMD-bits of the first command word will be interpreted in the following way: <ul style="list-style-type: none"> <li>If the Operating Mode (OM)<sup>1)</sup> bit of CMD[4:0] is zero, the CMD bits and the SUBCMD bits will be interpreted as a short command as described in <a href="#">Table 5 on Page 50</a>).</li> <li>If the Operating Mode (OM)<sup>1)</sup> bit of CMD[4:0] is set, the CMD bits and the SUBCMD bits will be interpreted as an operating mode described in <a href="#">Table 6 on Page 57</a>.</li> </ul>
BC	13	<b>Broadcast bit</b> 0 No broadcast message 1 Broadcast message. In case of a write command (R/W = 0) the VINETIC®-x will broadcast the data to all channels. In case of a read short command (R/W = 1) the VINETIC®-x will provide all requested data starting with channel 0, followed by channel 1 data, up to the last channel. In case of BC=1 the CHAN field of the first command word is ignored.  <i>Note: For VINETIC®-x Version 1.4 broadcast read (R/W=1) is only supported with short commands!            Broadcast write (R/W=0) is only supported with SOP and COP commands.            The Broadcast function is not available for IOP commands.            With the Version V1.4 two channel devices VINETIC®-2VIP and VINETIC®-2CPE the usage of the BC bit is restricted (see <a href="#">Chapter 4.8 on Page 66</a>).</i>

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Field	Bits	Description
<b>CMD</b>	[12:8]	<p><b>Command bits</b></p> <p>If the bit SC = 0, the CMD[4:0] bits are interpreted as one of the commands depicted in <a href="#">Table 4 on Page 49</a>.</p> <p>If the bit SC = 1, the CMD[4:0] bits are interpreted as described in the SC bit description.</p> <p><i>Note: Depending on the usages, the CMD[4:0] bits are named C4, C3, C2, C1, C0 (voice and data operation commands, see <a href="#">Table 4 on Page 49</a>), OM, C3, C2, C1, C0 (mail-box and download commands, see <a href="#">Table 5 on Page 50</a>) or OM, M3, M2, M1, M0 (operating mode of the VINETIC®-x, see <a href="#">Table 6 on Page 57</a>)</i></p>
<b>SUBCMD</b>	[7:4]	<p><b>Sub Command bits</b></p> <p>These bits are only evaluated in case of short commands (SC-bit is set). For coding see <a href="#">Table 5 on Page 50</a>, <a href="#">Table 6 on Page 57</a> and <a href="#">Table 7 on Page 60</a>.</p> <p>In all other cases these bits are zero (reserved for future use).</p>

Field	Bits	Description
<b>CHAN</b>	[3:0]	<p><b>Channel Number (binary coded)</b></p> <ul style="list-style-type: none"> <li>In case of SOP and COP commands on registers of “Allocation C” CHAN[3:0] specifies one of the four analog line channels of the VINETIC®-x.</li> <li>In case of SOP and COP commands on registers of “Allocation M” (Analog-Line-Module specific registers). For reading/writing these registers CHAN[3:0] of the first command word has to indicate:  “0”, to address the first Analog-Line-Module (corresponds to channel 0 and 1) and  “2”, to address the second Analog-Line-Module (corresponds to channel 2 and 3).</li> <li>In case of IOP commands the meaning of the CHAN[3:0] bits depends on the register which should be read/written. For detailed information see <a href="#">Chapter 7</a>.</li> <li>In case of EOP commands CHAN[3:0] specifies four, eight or sixteen channels of the corresponding SW-module. For detailed information see the <i>Preliminary User’s Manual - EDSP Firmware Description</i>.</li> <li>In case of VOP/EVT data packets CHAN[3:0] specifies one of up to eight voice channels. Channel zero to three address the four analog line channels, channel four to seven address external<sup>2)</sup> channels. [M-V-CPE]</li> <li>In case of the short commands the CHAN[3:0] bits specifies one of up to eight channels. Channel zero to three address the four analog line channels, channel four to seven address external<sup>2)</sup> channels</li> </ul> <p><i>Note: If the BC bit is set and valid (see description of BC-bit), the CHAN[3:0] bits will be ignored and the data will be broadcast to all channels.</i></p> <p><i>With the 2 channel devices VINETIC®-2VIP and VINETIC®-2CPE only two analog channels (0,1) and 4 coder channels (0..3) can be addressed via the CHAN field.</i></p>

<sup>1)</sup> The Operating Mode (OM) bit of CMD[4:0] exists only if bit SC = 1 (see [Table 5 on Page 50](#) and [Table 6 on Page 57](#)).

<sup>2)</sup> An external channel is a channel for that the VINETIC®-x provides DSP resources, but that cannot be terminated in the ALM.



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In **Table 4**, **Table 5** and **Table 6** the three basic submodes for the CMD and SUBCMD bits are described:

- Commands: bit SC = 0
- Short Commands: bit SC = 1, bit OM = 0
- Operating Modes: bit SC = 1, bit OM = 1

**Table 4      Coding of the CMD-Bits if Bit SC = 0**

<b>C4..C0</b>		<b>Description</b>
HEX	BIN	
00 <sub>H</sub>	00000	Reserved
01 <sub>H</sub>	00001	Status operation ( <b>SOP</b> )
02 <sub>H</sub>	00010	Coefficient operation ( <b>COP</b> )
03 <sub>H</sub>	00011	Interface operation ( <b>IOP</b> )
04 <sub>H</sub>	00100	Voice Packet operation ( <b>VOP</b> ) [M-V-CPE]
05 <sub>H</sub>	00101	Event Transmission Operation ( <b>EVT</b> ) [M-V-CPE]
06 <sub>H</sub>	00110	EDSP operation ( <b>EOP</b> )
07 <sub>H</sub> - 0F <sub>H</sub>	. . .	Reserved
10 <sub>H</sub>	10000	Fax Relay Data ( <b>FRD</b> ) [V-CPE]
11 <sub>H</sub>	10001	Fax Relay Status ( <b>FRS</b> ) [V-CPE]
12 <sub>H</sub> - 13 <sub>H</sub>	. . .	Reserved
14 <sub>H</sub>	10100	Caller Identification ( <b>CID</b> )
1F <sub>H</sub>	11111	Reserved

**Table 5 Coding Short Commands**
**Coding of the CMD- & SUBCMD-Bits if Bit SC = 1 & Bit OM = 0**

<b>OM</b>	<b>CMD</b>	<b>SUBCMD</b>	<b>Short Command Description</b>
	<b>C3..C0</b>	<b>S3..S0</b>	<b>See also <a href="#">Chapter 5 (Mailbox Concept, Data Handling)</a></b>
0	0000 0000		<b>rIR:</b> read Interrupt Register (IR <a href="#">Page 199</a> ) CHAN bits and BC bit will be ignored (read only) For register details see <a href="#">Page 199</a> .
0	0000 0001		<b>rSR:</b> read Status Register (SRS1/2, SRE1/2,). Read all status registers of specified channel/resource (CHAN[3:0]). If CHAN[3:0] = 0..3, the host has to read SRE1, SRE2, SRS1, SRS2.  If CHAN[3:0] 4..7 (CHAN[3:0]) the host has only to read SRE1 and SRE2. If BC bit is set, all status registers of all channels will be returned. See also “ <a href="#">Responses to Short Commands</a> ” on <a href="#">Page 42</a> <i>Note: Because of compatibility reasons VINETIC®-4S also returns the registers SRE1/2.</i>  For register details see <a href="#">Page 204</a> , <a href="#">Page 209</a> , <a href="#">Page 214</a> , <a href="#">Page 217</a> .
0	0000 0010		<b>rHWSR:</b> read Hardware Status Register (HWSR1/2) CHAN bits and BC bit will be ignored (read only). For register details see <a href="#">Page 219</a> , <a href="#">Page 221</a> .
0	0000 0011		<b>rSRGPIO:</b> read Status Register for GPIO's (SRGPIO) CHAN bits and BC bit will be ignored (read only) For register detail see <a href="#">Page 226</a>
0	0000 0100		<b>rBXSr:</b> read mailBoX Status Register (BXSr1, BXSr2) CHAN bits and BC bit will be ignored (read only) For register details see <a href="#">Page 223</a> , <a href="#">Page 224</a>

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**Table 5 Coding Short Commands**
**Coding of the CMD- & SUBCMD-Bits if Bit SC = 1 & Bit OM = 0 (cont'd)**

<b>CMD</b>		<b>SUBCMD</b>	<b>Short Command Description</b>
<b>OM</b>	<b>C3..C0</b>	<b>S3..S0</b>	<b>See also <a href="#">Chapter 5 (Mailbox Concept, Data Handling)</a></b>
0	0000 0110		<b>rSRS:</b> read Status Registers of ALM channel (SRS1 , SRS2). With CHAN[3:0] = 0..3, <i>VINETIC®</i> -x will return SRS1 and SRS2 of the specified ALM channel If BC bit is set, the status register of all ALM channels will be returned. See also “ <a href="#">Responses to Short Commands</a> ” on <a href="#">Page 42</a> (read only) For register details see <a href="#">Page 214</a> , <a href="#">Page 217</a> .
0	...		Reserved
0	0000 1001		<b>rl-SR:</b> read Interrupt Status Register (I-SRS1, ISRS2, I-SRE1, I-SRE2). Read all interrupt status register of specified channel/resource If CHAN[3:0] = 0..3, <i>VINETIC®</i> -x will return I-SRE1, I-SRE2, I-SRS1, I-SRS2. If CHAN[3:0] = 4..7 <i>VINETIC®</i> -x will return I-SRE1 and I-SRE2. If BC bit is set, all status register of all channels will be return. (see also “ <a href="#">Responses to Short Commands</a> ” on <a href="#">Page 42</a> ). <i>Note: Because of compatibility reasons VINETIC®-4S also returns the registers I-SRE1 and I-SRE2.</i> For register details see <a href="#">Page 228</a> , <a href="#">Page 230</a>
0	0000 1010		<b>rl-HWSR:</b> read Hardware Interrupt Status Register (I-HWSR1, I-HWSR2) CHAN bits and BC bit will be ignored (read only) For register details see <a href="#">Page 236</a> , <a href="#">Page 237</a>
0	0000 1011		<b>rl-SRGPIO:</b> read Interrupt Status Register for GPIO's (I-SRGPIO) CHAN bits and BC bit will be ignored (read only) For register details see <a href="#">Page 240</a> .

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**Table 5 Coding Short Commands**
**Coding of the CMD- & SUBCMD-Bits if Bit SC = 1 & Bit OM = 0 (cont'd)**

<b>CMD</b>		<b>SUBCMD</b>	<b>Short Command Description</b>
<b>OM</b>	<b>C3..C0</b>	<b>S3..S0</b>	<b>See also Chapter 5 (Mailbox Concept, Data Handling)</b>
0	0000 1100		<b>rI-BXSR</b> : read mailBoX Interrupt Status Register (I-BXSR1, I-BXSR2) CHAN bits and BC bit will be ignored (read only) For register detail see <a href="#">Page 238</a> , <a href="#">Page 239</a>
	0000 1101		<b>wCHECKSUM</b> : start checksum calculation over PHI program RAM The checksum is calculated once. After the calculation is finished (after 15 frames or 125 µsec) the checksum result is available in PHICKR For register details see <a href="#">Page 198</a> .
0	0000 1110		<b>rI-SRS</b> : read Interrupt Status Registers (I-SRS1, I-SRS2). CHAN[3:0] = 0..3, <i>VINETIC®</i> -x will return I-SRS1, I-SRS2 of the specified channel If BC bit is set, all status registers of all ALM channels will be returned. (see also <a href="#">“Responses to Short Commands” on Page 42</a> ). (read only) For register details see <a href="#">Page 233</a> and <a href="#">Page 235</a>
0	...		Reserved
0	0001 0000		<b>rFIBXMS</b> : read Free In-BoX-Memory Space register (FIBXMS) This command has to be sent before the host wants to write commands and/or packets to the <i>VINETIC®</i> -x. The command returns the Free Command In-Box Space and Free Packet In-Box Space in register FIBXMS. CHAN bits and BC bit will be ignored (read only) For register details see <a href="#">Page 241</a> . <i>Note: VINETIC®-4S will return FF<sub>H</sub> in the field FREE-PBOX-SPACE of the FIBXMS register.</i>

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Command/Data Structure

Table 5 Coding Short Commands

Coding of the CMD- & SUBCMD-Bits if Bit SC = 1 & Bit OM = 0 (cont'd)

OM	CMD	SUBCMD	Short Command Description
	C3..C0	S3..S0	See also <a href="#">Chapter 5 (Mailbox Concept, Data Handling)</a>
0	0001 0001		<p><b>rOBXML</b>: read Out-Box Message Length register (OBXML).  This command has to be sent before the host wants to read data from the command and/or packet out-box of the VINETIC®-x  This command has to be sent before the host wants to write commands and/or packets to the VINETIC®-x. The command returns the Command Data Size and Packet data size of the Out-mailbox in register OBXMS.  CHAN bits and BC bit will be ignored (read only).  For register details see <a href="#">Page 242</a>  <i>Note: VINETIC®-4S will return "0" in the field PDATA-SIZE of the OBXML register.</i></p>
0	0001 0010		<p><b>rPOBX</b>: read Packet Out-BoX. [M-V-CPE]  This command is sent if the host wants to read packet(s)  CHAN bits and BC bit will be ignored (read only).</p>
0	0001 0011		<p><b>rCOBX</b>: read Command Out-BoX.  This command is sent if the host wants to read the result of a read command  CHAN bits and BC bit will be ignored (read only).</p>
0	0001 0100		<p><b>wMAXCBX</b>: MAXimize Command in-BoX size.  Command in-box size = 255 words /  Packet in-box size = 31 words  CHAN bits and BC bit will be ignored (write only)  <i>Note: This command may only be used before the wSTEDSP command is written to the VINETIC®-x. Before writing the wMAXCBX command the host has to check if the in-boxes are empty (bit MBX-EMPTY in register BXS2 is set to 1).</i></p>

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Command/Data Structure

Table 5 Coding Short Commands

Coding of the CMD- & SUBCMD-Bits if Bit SC = 1 & Bit OM = 0 (cont'd)

CMD		SUBCMD	Short Command Description
OM	C3..C0	S3..S0	See also <a href="#">Chapter 5 (Mailbox Concept, Data Handling)</a>
0	0001 0101		<b>wMINCBX</b> : MINimize Command in-BoX size. Command in-box size = 31 words / Packet in-box size = 255 words CHAN bits and BC bit will be ignored (write only) <i>Note: This command may only be used before the wSTEDSP command is written to the VINETIC®-x. Before writing the wMAXCBX command the host has to check if the in-boxes are empty (bit MBX-EMPTY in register BXS2 is set to 1).</i>
0	...		Reserved
0	0010 0011		<b>wLEMP</b> : Load EDSP Micro Program. This short command is used to start the download of the EDSP micro program. The download monitor routine is started in the EDSP and the EDSP can handle the subsequent commands.  CHAN bits and BC bit will be ignored (write only)
0	0010 0100		<b>wSTEDSP</b> : STart EDSP. This command has to be sent to activate the EDSP after a micro program has been loaded to the EDSP or an external reset. With this command all internal variables of the EDSP are set to the default values.  CHAN bits and BC bit will be ignored (write only)
0	...		Reserved

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**Command/Data Structure**
**Table 5 Coding Short Commands**
**Coding of the CMD- & SUBCMD-Bits if Bit SC = 1 & Bit OM = 0 (cont'd)**

<b>CMD</b>		<b>SUBCMD</b>	<b>Short Command Description</b>
<b>OM</b>	<b>C3..C0</b>	<b>S3..S0</b>	<b>See also <a href="#">Chapter 5 (Mailbox Concept, Data Handling)</a></b>
0	0011 0000		<b>wLPMP:</b> Load PHI Micro Program This short command is used to start the download of the PHI micro program. CHAN bits and BC bit will be ignored (write only) <i>Note: Contrary to the standard short command sequence, this command word must not be terminated with an EOM on the address lines. The data words follow directly after the command word. The last data word, has to be terminated with EOM.</i>
0	0011 0001		<b>wSWRST:</b> Software ReSeT of the corresponding Analog Line Module channel. The EDSP functionality for the corresponding channel will not be reset. The power mode remains unchanged. If the BC bit is set, all channels will perform a software reset. In this case the EDSP will be reset also, no EDSP download is necessary since the PRAM and DRAM are not cleared) (write only).
0	0011 0010		<b>wRESYNC:</b> Re-SYNChronize PCM clock. The PLL clock divider is reset. This command is useful after the SYNC-FAIL bit in HWSR1 shows up. CHAN bits and BC bit will be ignored (write only)
0	0011 0011		<b>wPHIERR:</b> acknowledge PHI ERRor. If the bits HOST-ERR, PIBX-OF or CIBX-OF are set in the BXSr2 register (this may also generate an interrupt) the error condition has to be acknowledged by this command. The bits will be cleared. (write only) <i>Note: It may take up to 500 µs till the bits of BXSr2 are reset</i>
0	...		Reserved
0	1111 1111		Reserved

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*Note: If the R/W bit is not set properly, the command will not be executed.*

*A description of the registers that are accessible with short commands is given in **Chapter 7.5 on Page 199**.*

*A write short command (wXXXX) must be written with an EOM address. A read short command (rXXXX) must be written with a NWD address, the last read data must be accompanied by a EOM address.*

*Attention: The write short command wLPMP makes an exception to this sequence. With the wLPMP command the data bytes follow right after the command byte, and the last data byte must be written with an EOM address.*



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**Command/Data Structure**
**Table 6 Coding Short Commands for Op. Modes without DCCTL extension**
**Coding of CMD- & SUBCMD-Bits if Bit SC = 1 & Bit OM = 1  
Without DCCTL micro program extension<sup>1)</sup>**

OM	CMD [4:0]	SUBCMD [3:0]	Operating Mode Configuration Description <sup>2)</sup>
	MODE M3..M0	SUBMODE S3..S0	
1	0000 0000		Power Down High Impedance
1	...		Reserved
1	0001 0000 0001 0100		Ring Pause
1	0001 0001		Ring Pause with HIT
1	0001 0010		Ring Pause with HIR
1	0001 0011		Ring Pause with HIRT
1	0001 0101		Ring Pause with Tip to Ground (if SLIC-P is used)
1	0001 0110		Ring Pause with Ring to Ground (if SLIC-P is used)
1	...		Reserved
1	0010 0000		Active High ( $V_{BATH}$ )
1	0010 0001		Active with HIT
1	0010 0010		Active with HIR
1	0010 0011		Active with HIRT
1	0010 0100		Active Boost ( $V_{BATR}$ )
1	0010 0101		Active with Tip to Ground (if SLIC-P is used)
1	0010 0110		Active with Ring to Ground (if SLIC-P is used)
1	0010 0111		Active High Resistive (if SLIC-E Vers. 1.2 is used, with C3 connected to $V_{DD}$ )
1	0010 1000		Active Low ( $V_{BATL}$ )
1	...		Reserved
1	0011 0000		Sleep Power Down Resistive on $V_{BATH}$ and $V_{BGND}$
1	...		Reserved
1	0011 0100		Sleep Power Down Resistive on $V_{BATR}$ and $V_{BGND}$ (if SLIC-P is used)
1	...		Reserved
1	0100 0000		Ground Start

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**Command/Data Structure**
**Table 6 Coding Short Commands for Op. Modes without DCCTL extension**
**Coding of CMD- & SUBCMD-Bits if Bit SC = 1 & Bit OM = 1 (cont'd)**  
**Without DCCTL micro program extension<sup>1)</sup>**

OM	CMD [4:0]	SUBCMD [3:0]	Operating Mode Configuration Description <sup>2)</sup>
	MODE M3..M0	SUBMODE S3..S0	
1	...		Reserved
1	0101 0000 0101 0100		Ringing
1	0101 0001		Ringing with HIT
1	0101 0010		Ringing with HIR
1	0101 0101		Ringing on Ring with Tip to Ground (if SLIC-P is used)
1	0101 0110		Ringing on Tip with Ring to Ground (if SLIC-P is used)
1	...		Reserved
1	0110 0000		Active High with Metering
1	0110 0001		Active with Metering with HIT
1	0110 0010		Active with Metering with HIR
1	...		Reserved
1	0110 0100		Active Boost with Metering
1	0110 0101		Active with Metering with Tip to Ground (if SLIC-P is used)
1	0110 0110		Active with Metering with Ring to Ground (if SLIC-P is used)
1	...		Reserved
1	0110 1000		Active Low with Metering
1	...		Reserved
1	0111 0000		Power Down Resistive on V <sub>BATH</sub> and V <sub>BGND</sub>
1	...		Reserved
1	0111 0100		Power Down Resistive on V <sub>BATR</sub> and V <sub>BGND</sub> (if SLIC-P is used: PDRR)
1	...		Reserved
1	1111 1111		Reserved

- 1) Without download of a micro program extension to the Analog Line Module (DCCTL) VINETIC® supports SLIC-E/-E2, SLIC-S/-S2, SLIC-P and GEMINAX-S/-S2.
- 2) For an explanation of the different operating modes (including the SLIC modes) please refer to the *Preliminary User's Manual - System Reference*

**Table 7 Coding Short Commands for Op. Modes with DCCTL extension**

**Coding of the CMD- & SUBCMD-Bits if Bit SC = 1 & Bit OM = 1**  
**With DCCTL micro program extension<sup>1)</sup>**

<b>CMD [4:0]</b>		<b>SUBCMD [3:0]</b>	<b>Operating Mode Configuration Description<sup>2)</sup></b>
<b>OM</b>	<b>MODE M3..M0</b>	<b>SUBMODE S3..S0</b>	
1	0000 0000		Power Down High Impedance
1	...		Reserved
1	0001 0000 0001 0100		Ring Pause
1	0001 0001		Ring Pause with HIT
1	0001 0010		Ring Pause with HIR
1	0001 0011		Ring Pause with HIRT
1	0001 0101		Ring Pause with Tip to Ground (if SLIC-P is used)
1	0001 0110		Ring Pause with Ring to Ground (if SLIC-P is used)
1	...		Reserved
1	0010 0000		Active High ( $V_{BATH}$ )
1	0010 0001		Active with HIT
1	0010 0010		Active with HIR
1	0010 0011		Active with HIRT
1	0010 0100		Active Boost ( $V_{BATR}$ )
1	0010 0101		Active with Tip to Ground (if SLIC-P is used)
1	0010 0110		Active with Ring to Ground (if SLIC-P is used)
1	...		Reserved
1	0010 0111		Active High Resistive (if SLIC-E Vers. 1.2 is used, with C3 connected to $V_{DD}$ )
1	0010 1000		Active Low ( $V_{BATL}$ )
1	0010 1001		Active Test (ACT-T) (if SLIC-LCP is used)
1	0010 1010		Active Test In (ACT-TI) (if SLIC-LCP is used)
1	...		Reserved
1	0011 0000		Sleep Power Down Resistive on $V_{BATH}$ and $V_{BGND}$
1	...		Reserved

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**Command/Data Structure**
**Table 7 Coding Short Commands for Op. Modes with DCCTL extension**
**Coding of the CMD- & SUBCMD-Bits if Bit SC = 1 & Bit OM = 1 (cont'd)**  
**With DCCTL micro program extension<sup>1)</sup>**

OM	CMD [4:0]	SUBCMD [3:0]	Operating Mode Configuration Description <sup>2)</sup>
	MODE M3..M0	SUBMODE S3..S0	
1	0100 0000		Ground Start
1	0100 0001		Active Ground Start (ACTGS) (if SLIC-LCP is used)
1	0100 0100		Ground Start with fixed ring potential (HIT-2) (if SLIC-LCP is used)
1	...		Reserved
1	0101 0000 0101 0100		Ringing
1	0101 0001		Ringing with HIT
1	0101 0010		Ringing with HIR
1	0101 0101		Ringing on Ring with Tip to Ground (if SLIC-P is used)
1	0101 0110		Ringing on Tip with Ring to Ground (if SLIC-P is used)
1	0101 0111		Ring Trip Detection Test (RTT) (if SLIC-LCP is used)
1	...		Reserved
1	0110 0000		Active High with Metering
1	0110 0001		Active with Metering with HIT
1	0110 0010		Active with Metering with HIR
1	0110 0101		Active with Metering with Tip to Ground (if SLIC-P is used)
1	0110 0110		Active with Metering with Ring to Ground (if SLIC-P is used)
1	...		Reserved
1	0110 0100		Active Boost with Metering
1	...		Reserved
1	0110 1000		Active Low with Metering
1	...		Reserved

**Table 7 Coding Short Commands for Op. Modes with DCCTL extension**

**Coding of the CMD- & SUBCMD-Bits if Bit SC = 1 & Bit OM = 1 (cont'd)**  
**With DCCTL micro program extension<sup>1)</sup>**

<b>CMD [4:0]</b>		<b>SUBCMD [3:0]</b>	<b>Operating Mode Configuration Description<sup>2)</sup></b>
<b>OM</b>	<b>MODE M3..M0</b>	<b>SUBMODE S3..S0</b>	
1	0111 0000		Power Down Resistive on V <sub>BATH</sub> and V <sub>BGND</sub>
1	0111 0100		Power Down Resistive on V <sub>BATR</sub> and V <sub>BGND</sub> (if SLIC-P is used: PDRR)
1	...		Reserved
1	0111 0101		Power Down Active (PDNA) (if SLIC-LCP is used)
1	...		Reserved
1	1111 1111		Reserved

<sup>1)</sup> With the download of a micro program extension to the Analog Line Module (DCCTL) VINETIC® supports SLIC-E/-E2, SLIC-S/-S2, SLIC-P, GEMINAX-S/-S2, SLIC-LCP and GEMINAX-S MAX. For the supply of the micro program extension please contact your local Infineon sales.

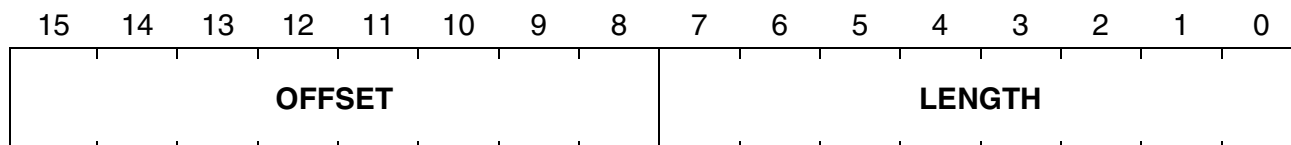
<sup>2)</sup> For an explanation of the different operating modes (including the SLIC modes) please refer to the *Preliminary User's Manual - System Reference*

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Command/Data Structure

#### 4.4 Second Command Word in Case of SOP, COP and IOP

The second command word in the command is necessary if the SC-bit of the first command word isn't set (SC = 0).



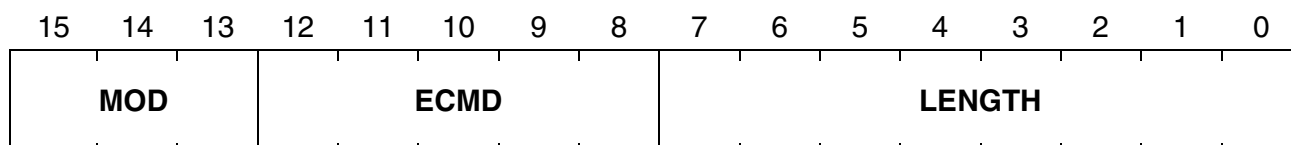
Field	Bits	Description
OFFSET	[15:8]	<b>Offset of the requested register.</b> The OFFSET field indicates the start offset of a specific number of consecutive registers to be accessed. The number of registers to be accessed is defined in the LENGTH field.
LENGTH	[7:0]	<b>Number of following data words</b> binary coded (in case of write commands) or number of data words to be read (in case of read commands) respectively. LENGTH[7:0] doesn't include the first and second command word.

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## 4.5 Second Command Word in Case of EOP

The second command word only exists if the SC-bit of the first command word isn't set (SC = 0).



Field	Bits	Description
MOD	[15:13]	<b>Selects the addressed module or indicates a resource command:</b> 000 Module PCM Interface (the CHAN field of the first command word contains the desired channel) 001 Module analog line Interface (the CHAN field of the first command word contains the desired channel) 010 Module Signaling (the CHAN field of the first command word contains the desired channel) 011 Module Coder Interface (the CHAN field of the first command word contains the desired channel) 100 Reserved 101 Control command (the CHAN field of the first command word is ignored) 110 Resource command (the CHAN field of the first command word contains the desired resource) 111 Test and Download (the CHAN field of the first command word is ignored)
ECMD	[12:8]	<b>EDSP command</b> for the addressed module/resource.
LENGTH	[7:0]	<b>Number of following data words</b> binary coded (see <i>Preliminary User's Manual - EDSP Firmware Description</i> ) (in case of write commands) or number of data words to be read (in case of read commands) respectively. LENGTH[7:0] does not include the first and second command word.

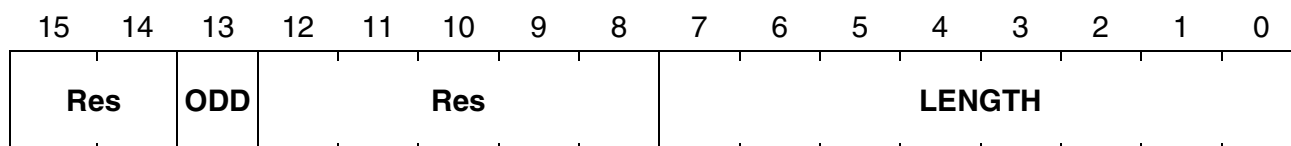


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## 4.6 Second Command Word in Case of EVT and VOP [M-V]

The second command word only exists if the SC-bit of the first command word is zero (SC = 0).

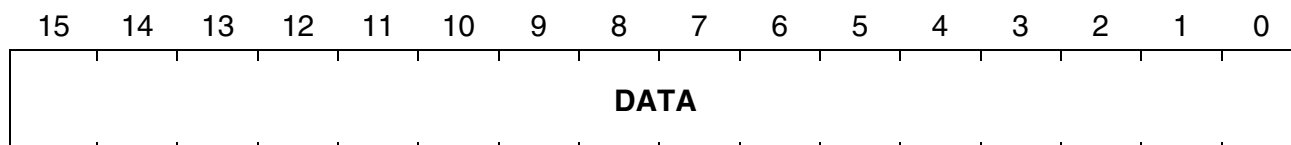
In fact the EVT and VOP command is always linked to a voice or event packet which is transferred via the packet mailbox to and from VINETIC®-x. That's why the two words ("first command word" and "second command word in case of EVT and VOP") can be seen as an additional 2 word header for voice or event packets.



Field	Bits	Description
<b>Res</b>	[15:14]	<b>Reserved</b> <i>Note: In downstream direction this bits should be set to 0. In upstream direction this bits will be set to 0 by VINETIC®-x.</i>
<b>ODD</b>	13	<b>Odd number of bytes.</b> This bit indicates if the LSB in the last data word is valid or not. 0 even number of byte, last significant byte in the last data word is valid 1 odd number off bytes, last significant byte in the last data word is not valid. In this case the controller can either remove the last byte or it can set the padding bit in the RTP header instead. <i>Note: In upstream direction the unused byte will always be set to 01<sub>H</sub>.</i>
<b>LENGTH</b>	[7:0]	<b>Number of following data words</b> binary coded (in case of write commands, downstream) or number of data words to be read (in case of read commands, upstream) respectively. LENGTH[7:0] doesn't include the first and second command word.

## 4.7 Data Words

Words following the first and second command words denote data (register values, command data, payload (voice and events) including RTP or AAL2 header, coefficients).



#### **4.8 Command Data Structure VINETIC®-2VIP and VINETIC®-2CPE.**

For the Version 1.4 devices with 2 analog channels, VINETIC®-2VIP and VINETIC®-2CPE, the command structure outlined in [Chapter 4.3](#) through [Chapter 4.7](#) has the following restrictions.

##### **Restrictions for commands/data structure in downstream direction:**

- The broadcast function is not supported in connection with packets, thus bit BC has to be set to 0 in packet commands.
- The broadcast function is not supported in connection with SOP, COP and IOP register access, thus bit BC has to be set to 0 in SOP, COP and IOP commands.
- The broadcast function is not supported in connection with Short Commands, thus bit BC has to be set to 0 in Short commands.

##### **Restrictions for commands/data structure in upstream direction:**

- The broadcast function is not supported in connection with packets, thus bit BC has to be set to 0 in packet commands.
- The broadcast function is not supported in connection with SOP, COP and IOP register access, thus bit BC has to be set to 0 in SOP, COP and IOP commands.
- The broadcast function may be used with channel oriented Short Commands (e.g rSR, rSRS, rl-SR, rl-SRS). The registers returned as response to those Short Commands will reflect the structure of a 4 channel device (see [Chapter 4.2.4 on Page 42](#)). All registers which are not supported by the 2 channel devices (analog channels C, D) will carry invalid data and have to be ignored by the host.

## 5 Mailbox Concept, Data Handling

The VINETIC®-x includes an interface controller (Programmable Host Interface - PHI) which handles the communication between the host and the VINETIC®-x internal units via a combination of HW and a SW state machine.

The VINETIC®-x programmable host interface handles:

- packet data (VOP, EVT commands [M-V-CPE]),
- command data (COP-, SOP-, IOP-, EOP- commands),
- short commands (SC bit of first command word is set) as well as
- direct interrupt register access (DIA) for SW-handshake with the RDYQ bit.

### 5.1 Downstream Direction (Host to VINETIC®-x)

*Note: Packet transfer (VOP, EVT) [M-V-CPE]*

Packets and commands sent by the host to the VINETIC®-x (or PHI respectively) are stored in buffers (mailboxes). Packets are stored in an in-buffer (packet in-box, one for all channels) and commands (read and write) are stored in another in-buffer (command in-box). Every 125 µs the VINETIC®-x internal EDSP will read one packet and one command from the packet and command in-box. COP, SOP and IOP commands will be distributed to the corresponding units (COP and SOP → Analog-Line-Module, IOP → PHI). VOP, EVT and EOP commands will be processed by the EDSP.

If the host wants to read command data, it has to send a read command (R/W bit of first command word is set). The EDSP retrieves the requested data and writes it to the command out-box and generates an interrupt.

*Note: Before the host sends a read command, it should check if there is enough space in the command out-box (this is done with the short command rOBXML). If there is not enough space available the VINETIC®-x will not process this read command as long as the host has not read the command out-box. All following commands (read and write) will be queued.*

Short commands (see [Table 5 on Page 50](#) and [Table 6 on Page 57](#)) are not written to a buffer but processed directly and with higher priority than packets and commands.

Before the host writes data to the VINETIC®-x, it has to make sure that there is enough free memory space in the desired packet- and/or command in-box. This is done by reading the FIBXMS (free in-box memory space) register via the short command rFIBXMS. As long as there is enough free memory space in the in-boxes (packets/commands) the host is allowed to send data.

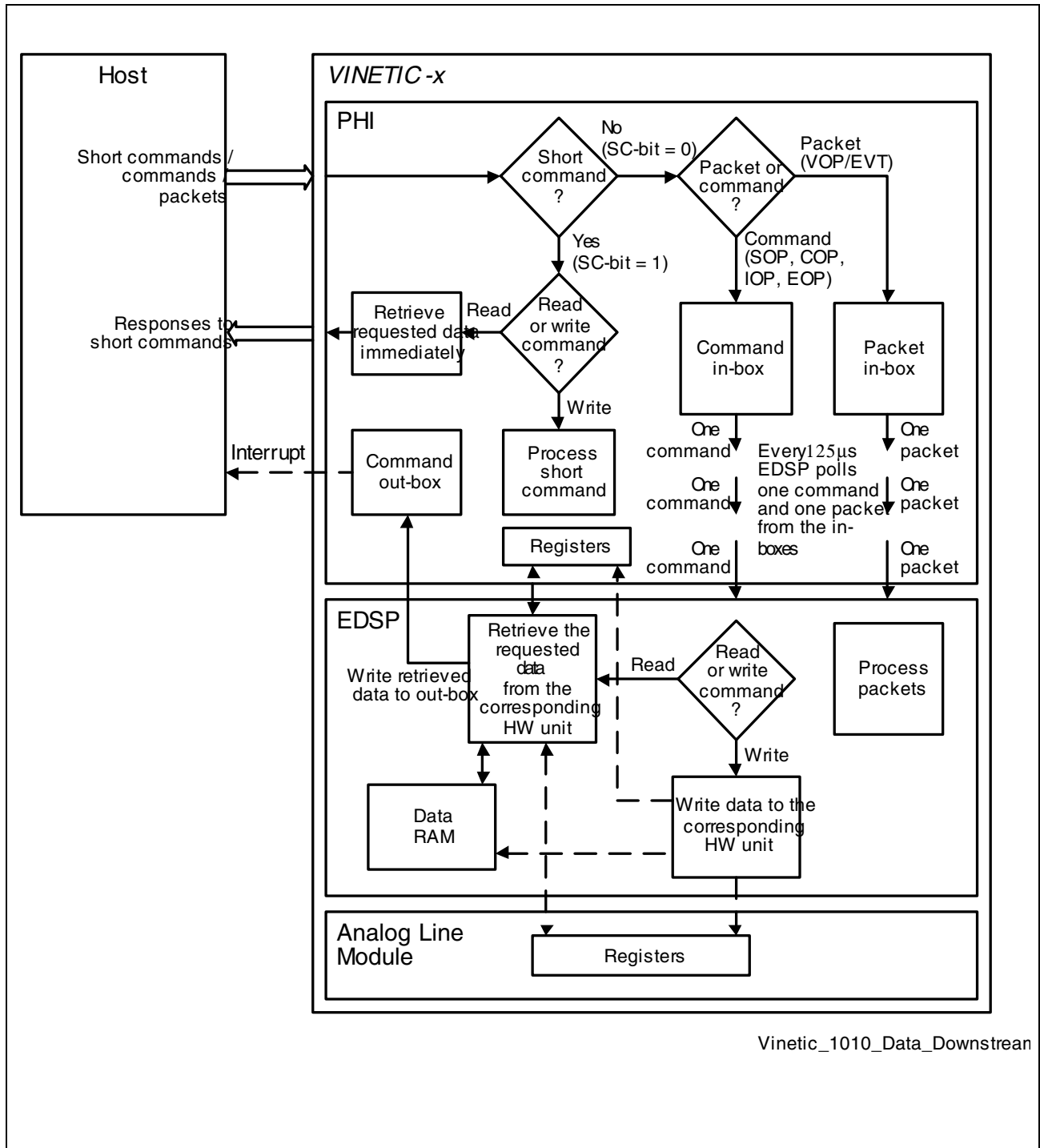
**Figure 9 on Page 68** gives an overview about the downstream transfer.

To optimize the data transfer during download and/or for packet transmission the size of the in-boxes (command/packet) can be changed with the short commands wMAXCBX ("Maximize command in-box size" → Command in-box size = 255 / Packet in-box size =

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31) and wMINCBX (“Minimize command in-box size” → Command in-box size = 31/ Packet in-box size = 255). Note that these commands may only be used before the wSTEDSP command.



**Figure 9 Data Transfer Downstream**

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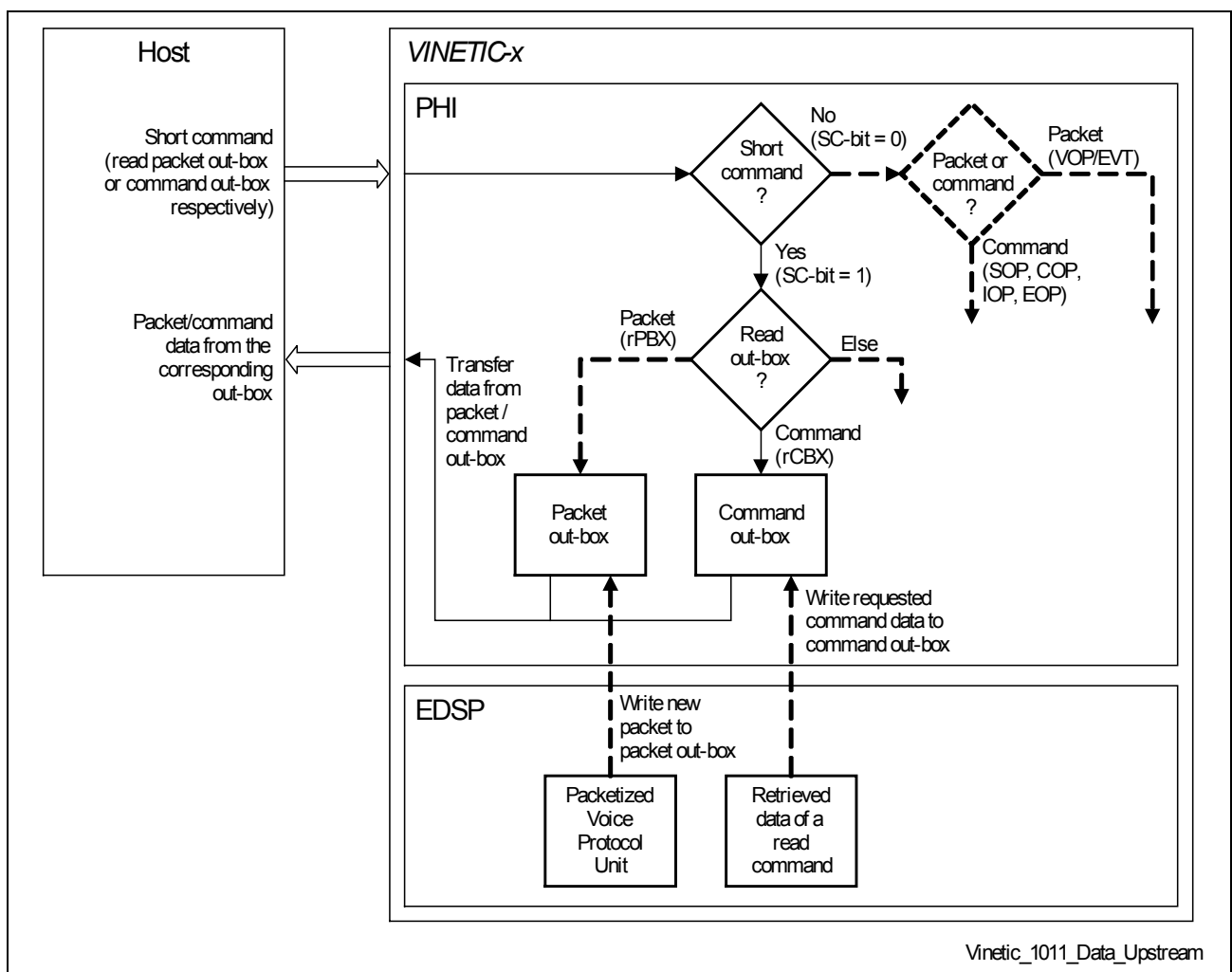
## 5.2 Upstream Direction (VINETIC®-x to Host)

*Note: Packet transfer (VOP, EVT) [M-V-CPE]*

In upstream direction packets or requested command data is transferred from the EDSP to internal out-buffers (packet out-box/command out-box) and the VINETIC®-x signals via status registers and interrupt that data is ready for reading. The answers to read commands are stored in the 31 word command out-box. Packet data for the host is stored in the 255 word packet out-box. The host can read the packet or command out-box via short commands (rPOBX → read packet out-box, rCOBX → read command out-box).

**Figure 10** gives an overview about the upstream transfer.

If the EDSP wants to send data (VOP or EVT operations) to the host, it checks the free memory space in the packet out-box before writing the data. If there is not enough memory in the packet out-box and the internal buffers within the EDSP software are full, the EDSP discards the data and sets the box-overflow flag in the Status Register for the EDSP (SRE2). Unlike as with the in-boxes the size of the out-boxes cannot be changed!



**Figure 10 Data Transfer Upstream**

### 5.3 Interrupt Mode / Polling Mode

The communication between host and VINETIC®-x can either be done via interrupt handling (maskable interrupt bits and an interrupt line) and/or by polling the status registers (host reads the VINETIC®-x status registers periodically).

The behavior of the VINETIC®-x in case of interrupt handling is described in [Chapter 3.6 on Page 28](#).

In case of polling mode the host deactivates those interrupt bits in the status registers, which should be polled, by setting the corresponding mask bits in the mask registers.

All bits of all status registers (except IR) can be masked. If a bit of a status register is masked, no interrupt will be generated, if the bit value changes. Furthermore the corresponding bit in the IR will not be set.

The following chapter shows the command sequences and flow charts to program the VINETIC®-x in case of interrupt and polling mode.

### 5.4 Data Transfer

#### 5.4.1 Packets (VOP)/Events (EVT) Downstream [M-V-CPE]

Whenever the host receives a packet/event from the net it can send it to the VINETIC®-x (if there is enough free memory space in the packet in-box).

Within the VINETIC®-x the Analog-Line-Module works with a constant sample rate and therefore it needs the packets for each channel in equal time intervals. Therefore the VINETIC®-x includes a jitter buffer (see also the *Preliminary User's Manual - EDSP Firmware Description*) to equalize the run time differences of the packets caused by the net.

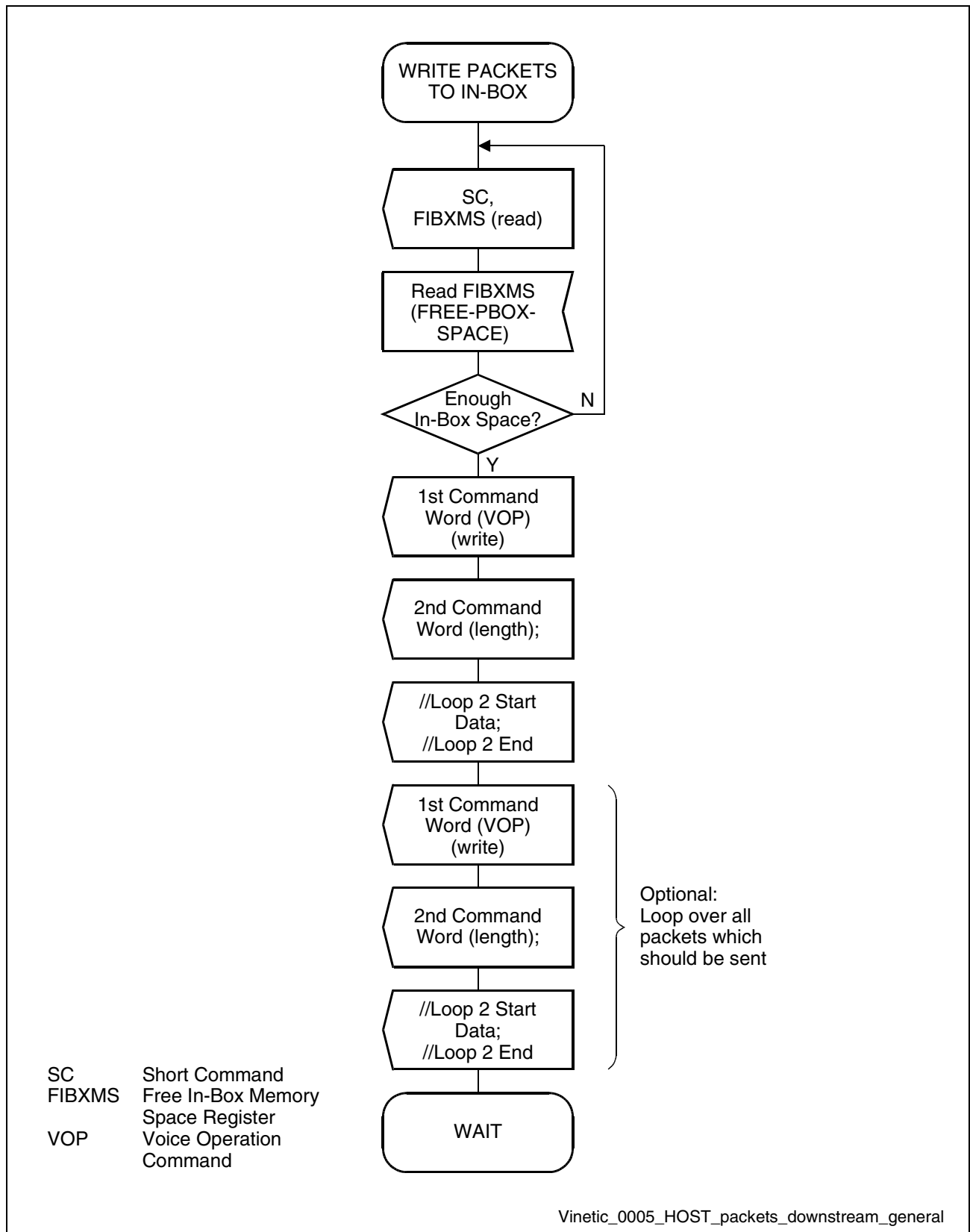
#### Polling Mode and Interrupt Mode

(See also [Figure 11](#))

1. Hosts sends the short command rFIBXMS<sup>1)</sup>  
→ Host reads FIBXMS (FREE-PBOX-SPACE[7:0])
2. If enough in-box-memory space is available, the host sends the packet(s). Each packet has to start with a VOP data packet.

*Note: The size of the packets must not exceed the free in-box-memory space. Otherwise the packets will be discarded and the PIBX-OF bit will be set in the BXS2.*

<sup>1)</sup> rFIBXMS: read Free In-BoX-Memory Space register



**Figure 11      Flow Chart Packets Downstream Procedure [M-V-CPE]**

### 5.4.2 Packets (VOP)/Events (EVT) Upstream [M-V-CPE]

After the VINETIC®-x has build a new packet it sets the MBX-EVT bit in the interrupt status register and the POBX-DATA bit in the Mailbox Status Register 2 (BXSR2). The host recognizes the request and reads the data from the packet out-box.

#### Polling Mode

(See also [Figure 12](#) and [Figure 13](#))

1. The host sends the short command rOBXML<sup>1)</sup>  
→ Host reads OBXML (PDATA-SIZE)
2. If PDATA-SIZE != 0 (data in packet out-box) the host sends the short command rPOBX<sup>2)</sup>  
→ Host reads the data

#### Interrupt Mode

(See also [Figure 12](#) and [Figure 13](#))

1. Host gets an interrupt and sends the short command rIR<sup>3)</sup>  
→ Host reads IR (MBX-EVT)
2. If the MBX-EVT bit is set, the host sends the short command rl-BXSR<sup>4)</sup>  
→ Host reads I-BXSR1 and I-BXSR2 (POBX-DATA in I-BXSR2)
3. If packets are ready for reading (bit POBX-DATA is set), the host sends the short command rOBXML<sup>2)</sup>  
→ Host reads OBXML (PDATA-SIZE)
4. Host sends the short command rPOBX<sup>3)</sup>  
→ Host reads as many words as indicated with PDATA-SIZE

#### Note:

1. *It may happen that more than one packet is stored in the out-box (especially in polling mode).*
2. *If the EDSP can't write a packet to the packet out-box, because of missing memory space in the packet out-box (host hasn't read the out-box timely), it discards the packet and sets the PVPU-OF flag in the Status Register SRE2.*

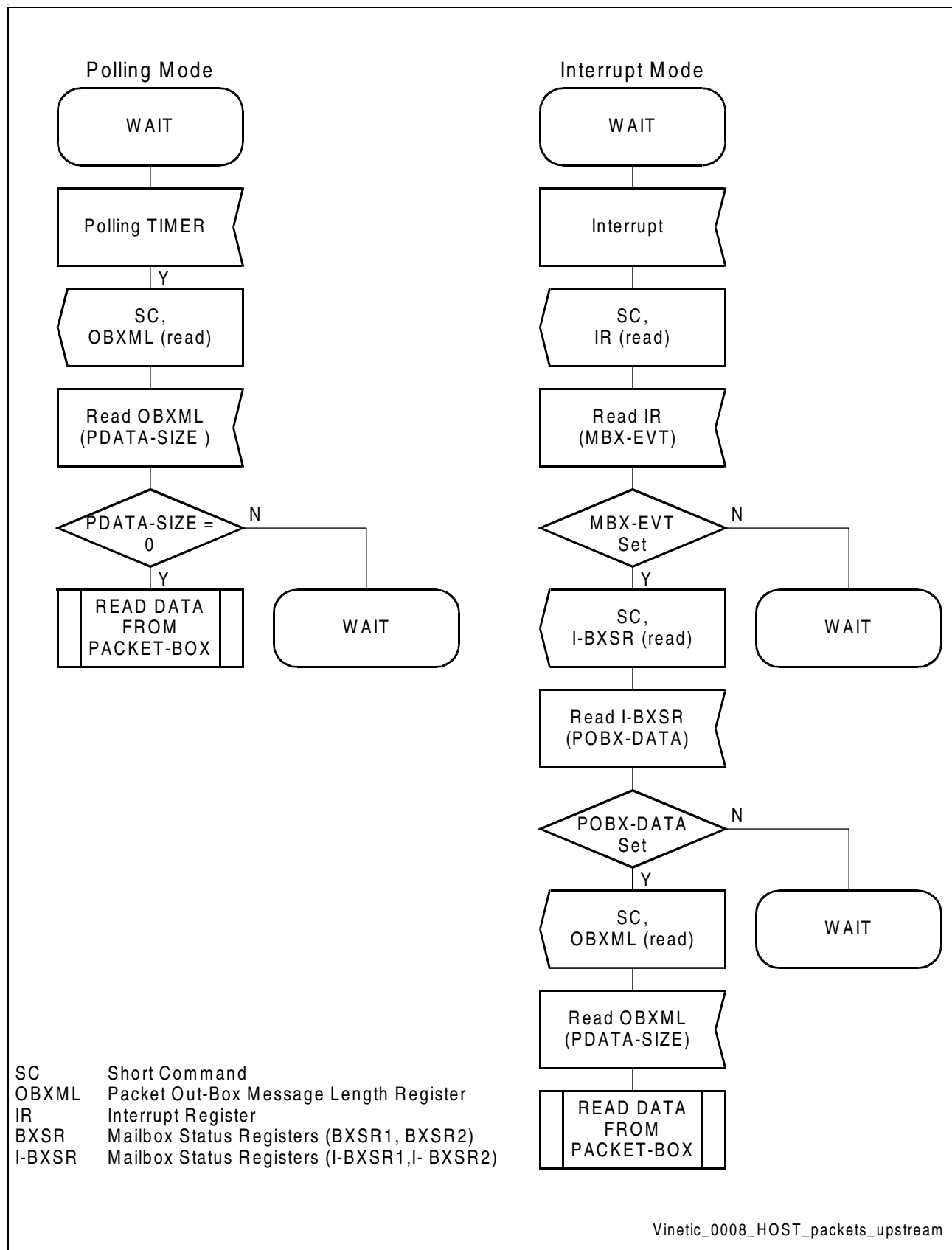
<sup>1)</sup> rOBXML: read Out-Box Message Length register

<sup>2)</sup> rPOBX: read Packet Out-BoX

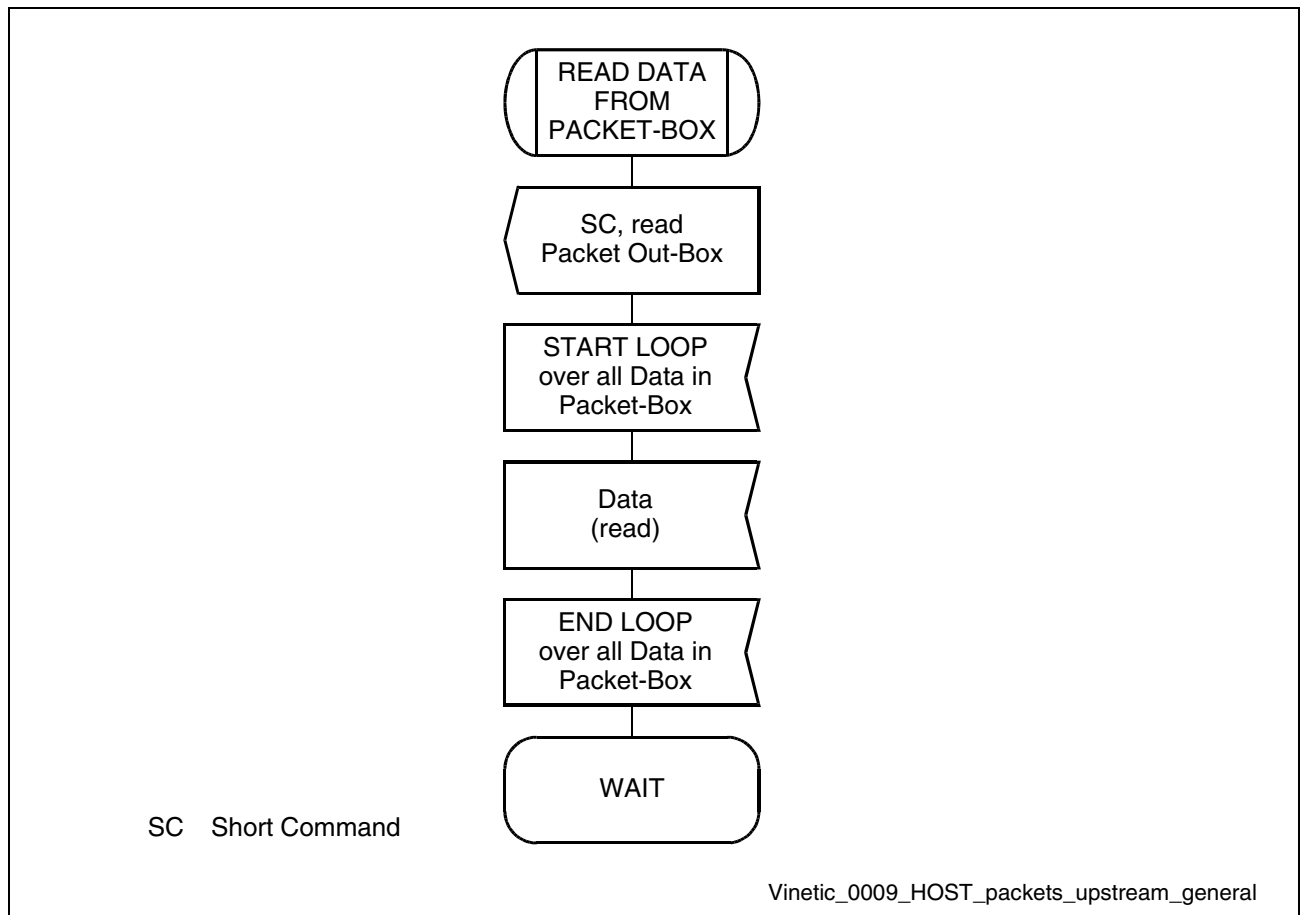
<sup>3)</sup> rIR: read Interrupt Register

<sup>4)</sup> rl-BXSR: read mailBoX Interrupt Status Register





**Figure 12 Flow Chart Packets Upstream**



**Figure 13 Flow Chart Packets Upstream General Procedure**

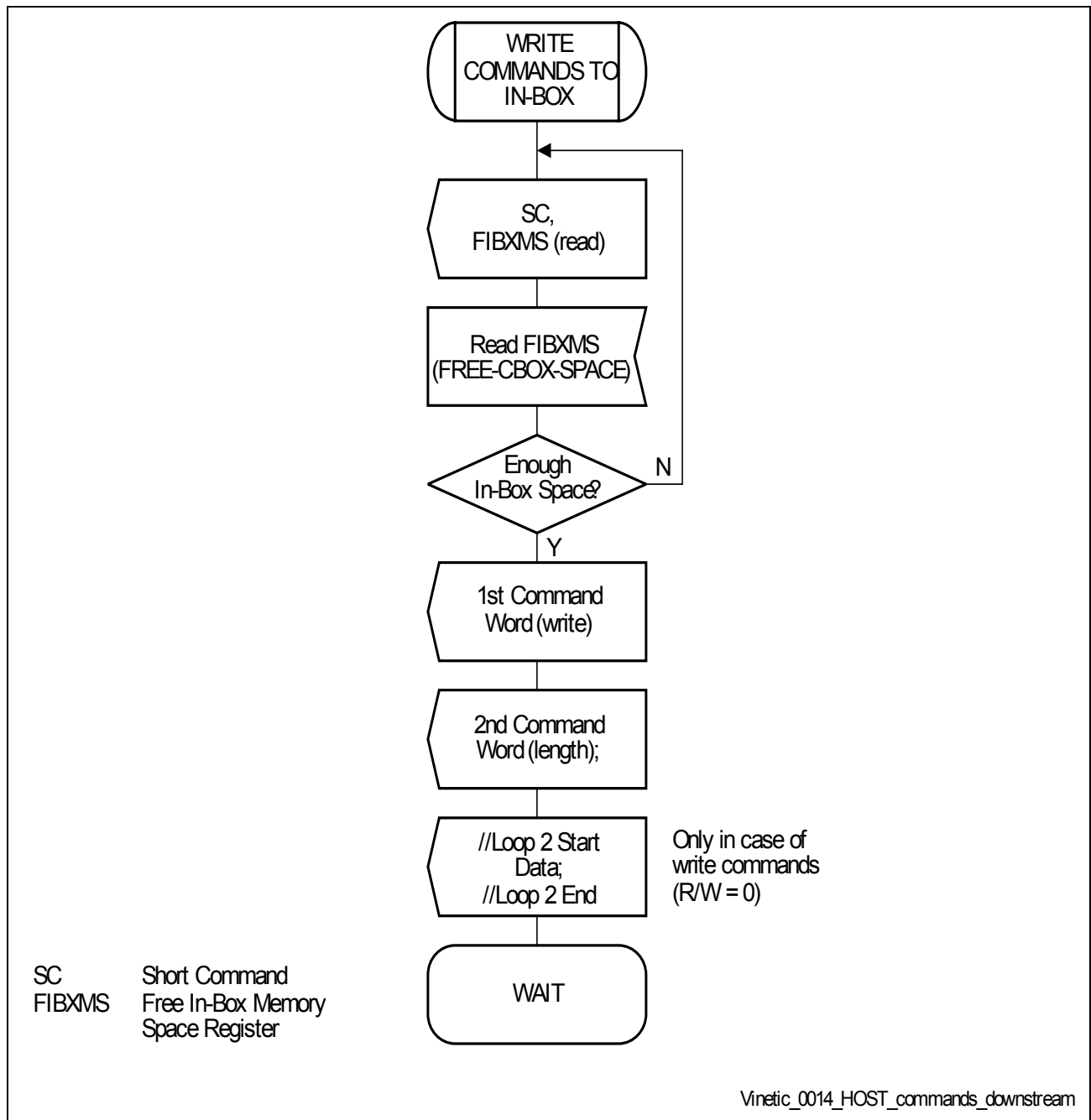
### 5.4.3 Command (SOP, COP, IOP, EOP) Write (Downstream)

(See also [Figure 14](#))

1. Host sends the short command rFIBXMS<sup>1)</sup>  
→ Host reads FIBXMS (FREE-CBOX-SPACE[7:0])
2. If enough in-box-memory space is available, the host sends the write command (COP, SOP, IOP, EOP)

*Note: The size of the command should not exceed the free command in-box-memory space. Otherwise all commands which exceed the free in-box memory space will be ignored and the CIBX-OF bit in register BXS2 will be set.*

<sup>1)</sup> rFIBXMS: read Free In-BoX-Memory Space register



**Figure 14      Flow Chart Commands (Read/Write) Downstream**

#### **5.4.4      Command (SOP, COP, IOP, EOP) Read (Upstream)**

##### **Polling Mode**

(See also [Figure 15](#) and [Figure 16](#))

1. Host sends the short command rFIBXMS  
→ Host reads FIBXMS (FREE-CBOX-SPACE[7:0])

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2. If enough in-box-memory space is available, the host sends the read command (SOP, COP, IOP, EOP)
3. As soon as the VINETIC®-x has prepared the requested data, the COBX-DATA bit in the BXS2 and indicates the number of words to read in CDATE-SIZE of register OBXML
4. The host polls the OBXML (CDATA-SIZE) register by sending the short command rOBXML<sup>1)</sup> as long as CDATE-SIZE != 0
5. Host sends the short command rCOBX<sup>2)</sup>  
→ Host reads the data

**Interrupt Mode**

(See also **Figure 15** and **Figure 16**)

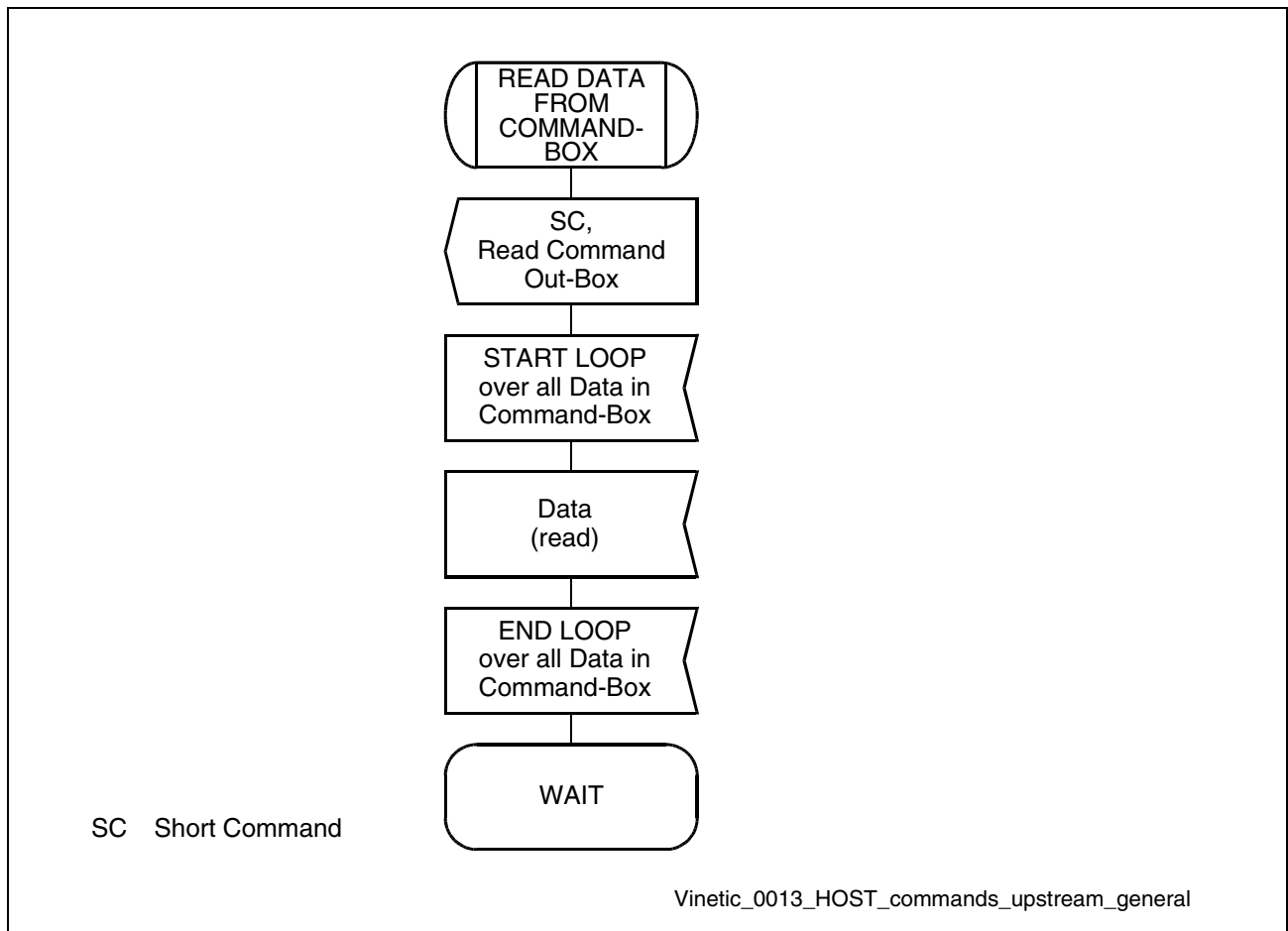
1. Host sends the short command rFIBXMS<sup>3)</sup>  
→ Host reads FIBXMS (FREE-CBOX-SPACE[7:0])
2. If enough in-box-memory space is available, the host sends the read command (SOP, COP, IOP, EOP)
3. As soon as the VINETIC®-x has prepared the requested data it sets the MBX-EVT bit in the IR and the COBX-DATA bit in the I-BXS2 and indicates the number of words to read in CDATE-SIZE of register OBXML
4. Host recognizes the interrupt and sends the short command rIR<sup>4)</sup>  
→ Host reads IR (MBX-EVT)
5. If the MBX-EVT bit is set, the host sends the short command rI-BXS<sup>5)</sup>  
→ Host reads I-BXS1 and I-BXS2 (COBX-DATA)
6. If the COBX-DATA bit is set, the host sends the short command rOBXML<sup>2)</sup>  
→ Host reads OBXML (CDATA-SIZE)
7. Host sends the short command rCOBX<sup>3)</sup>  
→ Host reads the data

*Note: Every 125 µs the EDSP reads one command from the command in-box. If the command is a read command (R/W = 1) the EDSP checks, if there is enough space in the command out-box. If not the EDSP will wait until there is enough space available. This means that all other command which are waiting in the in-box queue will not be processed.*

1) rOBXML: read Out-Box Message Length register  
 2) rCOBX: read Command Out-BoX  
 3) rFIBXMS: read Free In-BoX-Memory Space register  
 4) rIR: read Interrupt Status Register  
 5) rI-BXS: read mailBoX Interrupt Status Register

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**Figure 16 Flow Chart Commands Upstream General Procedure**

## 5.5 Examples for Command and Packet Transfer

For parallel interfaces it is necessary to signal additional information on the address lines (like continuing data transfer or end of data transfer respectively) to the VINETIC®-x. For detailed information see [Chapter 6.1.1 on Page 83](#). This signaling information is shown in the following tables in column “Address Lines”. For serial interfaces this column can be ignored.

### 5.5.1 Example for Packet Transfer Downstream [M-V-CPE]

**Table 8 Example for Packet Transfer Downstream**

No	Description	RD/ WR	Address Lines <sup>1)</sup>	Data Lines
1.	Host sends the short command rFIBXMS	Low	0010 (NWD)	11x00001 0000xxxx (short command)
	Host reads FIBXMS register (e.g. FREE-PBOX-SPACE[7:0] = 255)	High	0011 (EOM)	00000000 11111111 (FIBXMS)
2.	If enough in-box-memory space is available, the host sends the packet for channel three with a VOP data packet. (e.g. LENGTH = 4).	Low	0010 (NWD)	00x00100 xxxx0011 (first command word, VOP)
		Low	0010 (NWD)	xxxxxxxx 00000100 (second command word, LENGTH = 4)
		Low	0010 (NWD)	xxxxxxxx xxxxxxxx (data word)
		Low	0010 (NWD)	xxxxxxxx xxxxxxxx (data word)
		Low	0010 (NWD)	xxxxxxxx xxxxxxxx (data word)
		Low	0011 (EOM)	xxxxxxxx xxxxxxxx (last data word)

<sup>1)</sup> For detailed information see [Chapter 6.1.1 on Page 83](#). In case of a serial interface this column can be ignored.

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**5.5.2 Example for Packet Transfer Upstream [M-V-CPE]**

VINETIC®-x has transferred a packet to the packet out-box, sets the POBX-DATA (register BXSRI) and the MBX-EVT (register IR) and generates an interrupt (if not masked).

**Table 9 Example for Packet Transfer Upstream (Interrupt Mode)**

No	Description	RD/ WR	Address Lines <sup>1)</sup>	Data Lines
1.	Host gets an interrupt and sends the short command rIR	Low	0010 (NWD)	11x00000 0000xxxx (short command)
	Host reads IR and recognizes, that the MBX-EVT bit is set	High	0011 (EOM)	00000000 00000001 (IR)
2.	Host sends the short command rl-BXSRI	Low	0010 (NWD)	11x0000 1100xxxx (short command)
	Host reads l-BXSRI (e.g. no bits are set)	High	0010 (NWD)	00000000 00000000 (l-BXSRI)
	Host reads l-BXSRI2 (e.g. only bit POBX-DATA is set)	High	0011 (EOM)	00000000 00001000 (BXSRI2)
3.	Host sends the short command rOBXML	Low	0010 (NWD)	11x00001 0001xxxx (short command)
	Host reads OBXML (e.g. PDATA-SIZE = 5)	High	0011 (EOM)	00000000 00000101 (OBXML)
4.	Host sends the short command rPOBX  Host reads the first word of the packet out-box. (e.g. The VINETIC has sent a VOP data packet for channel one with LENGTH = 3)	Low	0010 (NWD)	11x00001 0010xxxx (short command)
		High	0010 (NWD)	10x00100 xxxx0001 (first command word, VOP)
		High	0010 (NWD)	xxxxxxxx 00000011 (second command word, LENGTH = 3)
		High	0010 (NWD)	xxxxxxxx xxxxxxxx (packet data)
		High	0010 (NWD)	xxxxxxxx xxxxxxxx (packet data)
		High	0011 (EOM)	xxxxxxxx xxxxxxxx (last packet data word)

<sup>1)</sup> For detailed information see [Chapter 6.1.1 on Page 83](#). In case of a serial interface this column can be ignored.



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**5.5.3 Example for a Write Command**
**Table 10 Example for a Write Command**

No	Description	RD/ WR	Address Lines <sup>1)</sup>	Data Lines
1.	Host sends the short command rFIBXMS	Low	0010 (NWD)	11x00001 0000xxxx (short command)
	Host reads FIBXMS register (e.g. FREE-CBOX-SPACE[7:0] = 31)	High	0011 (EOM)	00011111 xxxxxxxx (FIBXMS)
2.	If enough in-box-memory space is available, the host sends the write command (e.g. SOP command for channel 2; register BCR1, LENGTH = 1)	Low	0010 (NWD)	00000001 xxxx0010 (first command word, SOP)
		Low	0010 (NWD)	00000111 00000001 (second command word, OFFSET = 7, LENGTH = 1)
		Low	0011 (EOM)	xxxxxxxx xxxxxxxx (last data word, BCR1)

<sup>1)</sup> For detailed information see [Chapter 6.1.1 on Page 83](#). In case of a serial interface this column can be ignored.

**5.5.4 Example for a Read Command**
**Table 11 Example for a Read Command (Polling Mode)**

No	Description	RD/ WR	Address Lines <sup>1)</sup>	Data Lines
1.	Host sends the short command rFIBXMS	Low	0010 (NWD)	11x00001 0000xxxx (short command)
	Host reads FIBXMS register (e.g. FREE-CBOX-SPACE[7:0] = 20)	High	0011 (EOM)	00010100 xxxxxxxx (FIBXMS)
2.	If enough in-box-memory space is available, the host sends the read command (e.g. SOP for channel 3; register IOCTL1+IOCTL2, LENGTH = 2)	Low	0010 (NWD)	10000001 xxxx0011 (first command word, SOP)

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**Table 11 Example for a Read Command (Polling Mode) (cont'd)**

No	Description	RD/ WR	Address Lines <sup>1)</sup>	Data Lines
		Low	0011 (EOM)	00000101 00000010 (second command word, OFFSET = 5, LENGTH = 2)

As soon as the VINETIC®-x has prepared the requested data it sets the MBX-EVT bit in the IR and the COBX-DATA bit in the I-BXSR2 and indicates the number of words to read in CDATE-SIZE of register OBXML

3.	Host polls the OBXML by sending the short command rOBXML	Low	0010 (NWD)	11x00001 0001xxxx (short command)
	Host reads OBXML (e.g. CDATE-SIZE = 4)	High	0011 (EOM)	00000100 00000000 (OBXML)
4.	If the CDATE-SIZE != 0 the host reads the command out mailbox. (short command rCOBX)	Low	0010 (NWD)	11x00001 0011xxxx (short command)
		High	0010 (NWD)	10000001 xxxx0011 (first command word, SOP)
		High	0010 (NWD)	00000101 00000010 (second command word, OFFSET = 5, LENGTH = 2)
		High	0010 (NWD)	xxxxxxxx xxxxxxxx (IOCTL1)
		High	0011 (EOM)	xxxxxxxx xxxxxxxx (last data word, IOCTL2)

<sup>1)</sup> For detailed information see [Chapter 6.1.1 on Page 83](#). In case of a serial interface this column can be ignored.

## **6 Interface Description**

The VINETIC®-x supports different serial and parallel interface types:

- Intel 16-bit parallel interface,
- Motorola 16-bit parallel interface,
- Serial  $\mu$ C interface - SCI (Motorola SPI slave mode and DuSLIC® compatible),
- PCM,
- Intel 8-bit parallel interface,
- Motorola 8-bit parallel interface,

The described command/data/packet handling (see [Chapter 5 on Page 67](#)) is valid for all interface types.

All types of micro controller interfaces ( $\mu$ C-interfaces = host interfaces) are multiplexed to the same pins. Each host interface can be used in parallel with the PCM data interface. The preferred interface type can be selected by means of pin strapping with the pins IFSEL0, IFSEL1, IFSEL2 and IFSEL3 (for more details see *Preliminary Data Sheet*).

### **6.1 Parallel Interfaces**

#### **6.1.1 16-bit Parallel Interfaces**

Since parallel interfaces do not allow a continuous lock of the interface state machine like serial interfaces do, additional information about the nature of a data-word is necessary. For the parallel interface types this is performed by using the address lines to indicate the transmission end. For every word which should be transmitted (except the last data word) the host signals NWD (next word). For the last word which should be transmitted the host has to send EOM (end of message). This is valid for read and write access.

**Table 12** gives an overview about the address coding. VINETIC®-x latches in four address bits. In the demultiplexed interface mode the address information is taken from pins IFC0, IFC1, IFC2 and IFC3 (host processors that only put out even addresses on their address bus must be connected shifted, i.e. address lines A1 - A4 instead of A0 - A3 must be connected to the respective VINETIC®-x address pins).

In the multiplexed address mode the address information is taken from the pins IFAD0, IFAD1, IFAD2 and IFAD3. In this mode the EOM coding is changed in order to allow also the connection to processors that only put out even addresses.

**Table 12 VINETIC®-x Address Coding**

Demux Mode	Intel Mux Mode	Description
IFC3..IFC0	IFAD3..IFAD0	
0000	0000	Reserved
0001	0001	Reserved
0010	0010	NWD (Next Word): Indicates that the next word (data or a command word) is following (optional). This indication will not be checked by the PHI.
0011	0100	EOM (End Of Message): Indicates the last data or command word.
...	...	Reserved
1100	1100	DIA (Direct IR register Access): By applying this address and a read signalization on the control lines the Interrupt Register (IR) content (including the RDYQ bit) will be returned immediately without recovery time restriction (always accessible). This signaling is needed if SW handshake is used. (see <a href="#">“Direct Interrupt Register Access (DIA)” on Page 86</a> )
...	...	Reserved
1111	1111	Reserved

### 6.1.1.1 HW-Handshake (RDYQ PIN) and SW Handshake (RDYQ Bit)

As the commands of the VINETIC®-x have different command recovery times the VINETIC®-x supports HW and SW handshake for optimizing the data rate between host and VINETIC®-x. HW handshake is done via the RDYQ pin as described in *Preliminary Data Sheet*. SW handshake can be done via the RDYQ bit in the IR. The RDYQ bit reflects the status of the RDYQ pin. The RDYQ bit in the IR can be accessed directly via DIA address signaling (see also [Chapter 6.1.1.2](#)). This allows a data read of the IR within a single chip select access. By polling the RDYQ bit after each access the data transfer can be optimized. If the RDYQ bit is zero the VINETIC®-x is ready for the next command.

All other registers as well as the command in/out-boxes and packet in/out-box can not be addressed directly via DIA. For this the PHI handles the data transfer by auto address increment.

To enable performance computations the command processing times are listed in [Chapter 6.1.2](#). An example for the RDQ handshake is given in [Figure 17](#).

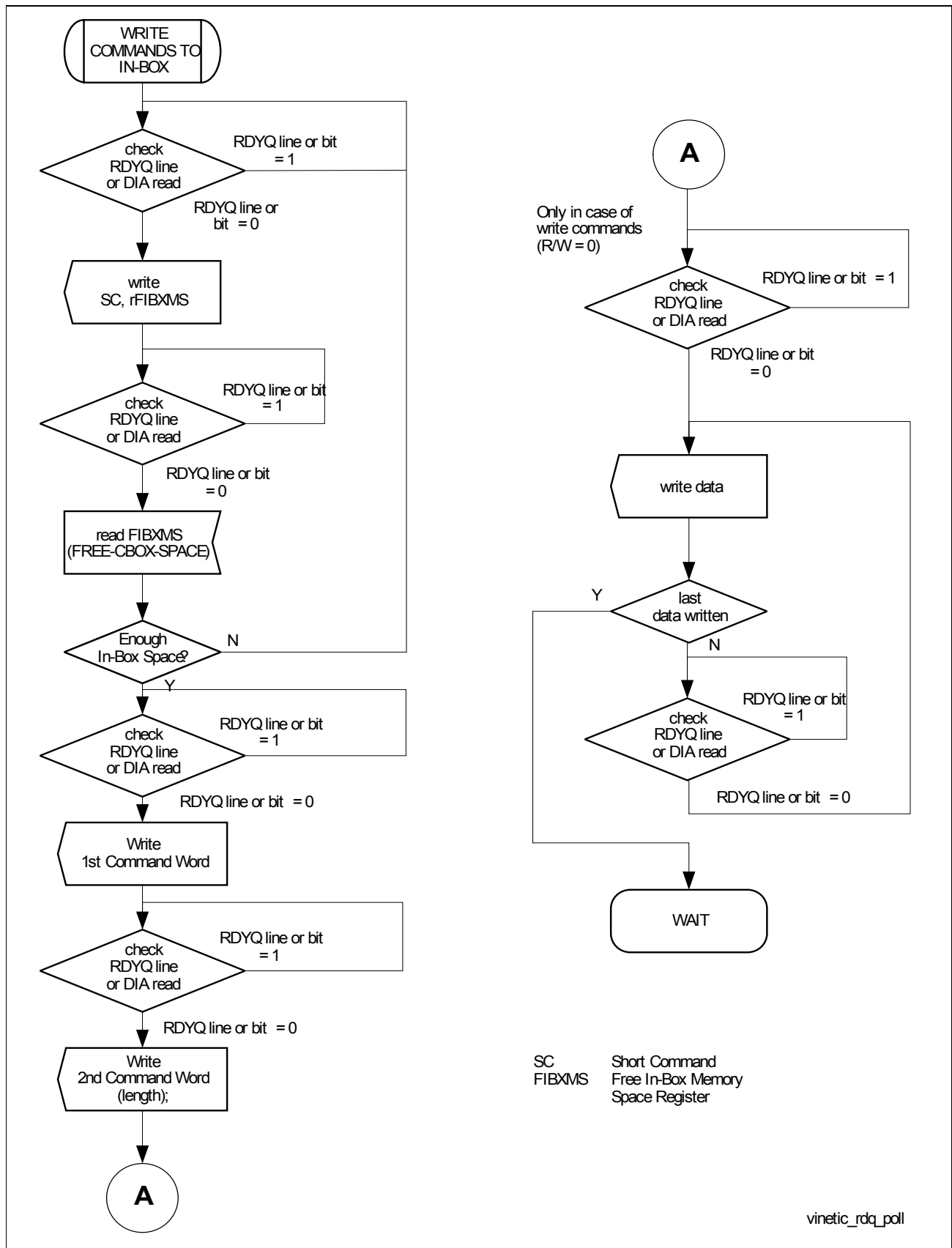


Figure 17 Example for Chip Access with Handshake

### 6.1.1.2 Direct Interrupt Register Access (DIA)

Beside a HW-handshake the VINETIC®-x also supports SW-handshake via the RDYQ bit, which resides in the Interrupt Register (IR). In order to poll the status of the RDYQ bit, IR has to be accessed via the address indication 1100 (DIA) at the address lines (see [Table 12](#)).

The RDYQ bit represents the current status of the RDYQ pin. Only when the RDYQ bit reflects a "0", VINETIC®-x is ready for the next access by the host. Accessing the RDYQ bit via DIA is only possible with 8-bit as well as 16 bit parallel host interfaces. DIA is not possible in case of a serial interface, in this case HW handshaking has to be used.

*Note: In case of an interrupt generated by the RESET bit in the IR, the interrupt is only cleared if the IR is accessed via the short command rIR, as the DIA access does not clear the RESET bit. Thus DIA should only be used for polling the RDYQ bit!*

[Table 13](#) shows the example for a direct access of the IR via DIA address signaling.

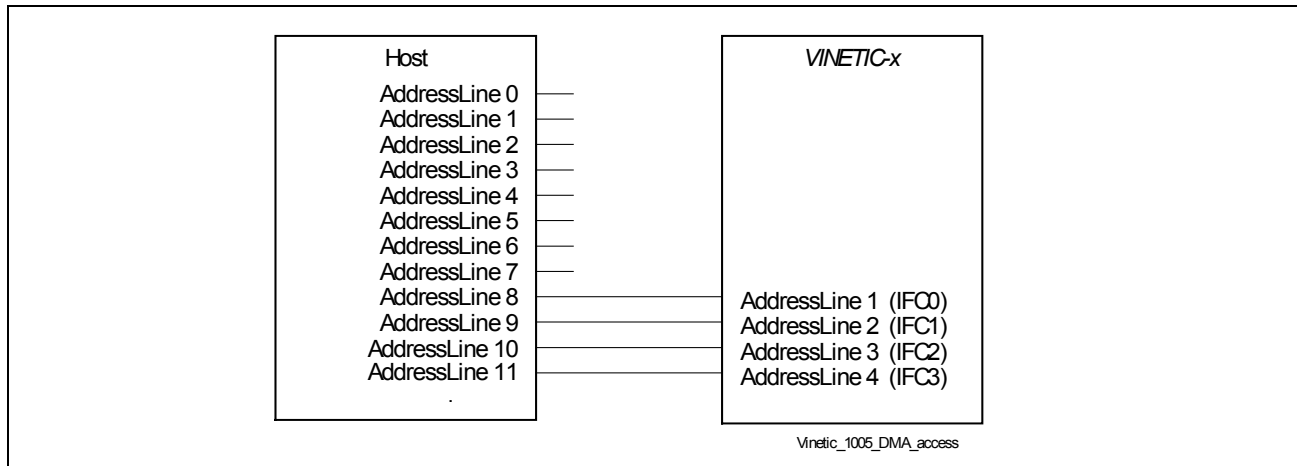
**Table 13 Example for a Direct IR Register Access**

No	Description	RD/ WR	Address Lines <sup>1)</sup>	Data Lines
1.	Host reads IR via DIA address signaling	High	1100 (DIA)	xxxxxxxx xxxxxxxx (IR)

<sup>1)</sup> For detailed information see [Chapter 6.1.1](#).

### 6.1.1.3 Using a Direct Memory Access (DMA)

It is possible to read/write data from/to the VINETIC®-x with one single DMA transfer. If the address lines of the host are connected to the address lines of the VINETIC®-x as shown in [Figure 18](#) and the host wants to transfer for example 67 words to the VINETIC®-x, it has to compute the start address by subtracting 1000011B (= 67) from 001100000001B (= 769) → 001010111110B (= 702). As only the highest four bits are connected to the VINETIC®-x the VINETIC®-x gets only the indication 0010 (= NWD) for all data except the last data word. With the last data word the address indication changes to 0011 (EOM) and the data transfer is finished. Of course also with DMA the host has to take care of the handshake via the RDYQ pin or via the RDYQ bit.



**Figure 18 Connecting Address Lines of Host and VINETIC®-x (Example)**

For a detailed description of the parallel host interfaces concerning diagrams and timing values please refer to the *Preliminary Data Sheet*.

### 6.1.2 8-bit Parallel Interfaces

The internal structure of VINETIC®-x is based on 16-bit registers. An 8-bit interface is supported also. The 8 bit data which is received via this interface is composed internally to 16 bit again. So always two 8-bit words form a complete command word or a complete data word.

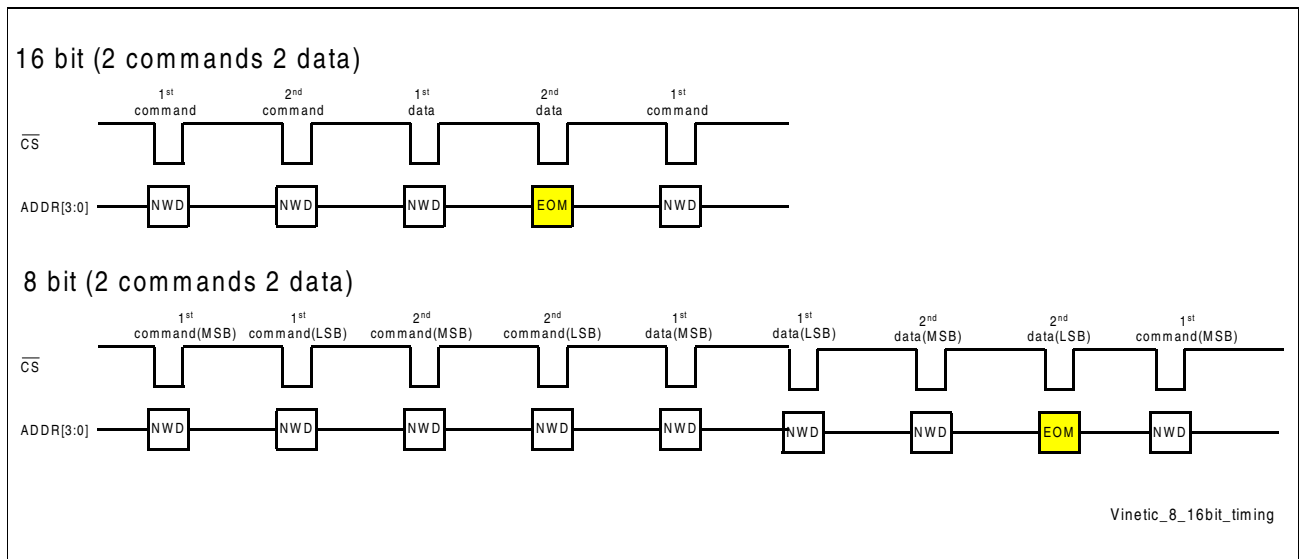
The principle differences for the chip access between 16-bit and 8-bit interfaces can be seen in **Figure 19**. The most significant byte (bits 15 to 8) of the 16-bit command is expected first, the least significant byte (bits 7 to 0) is expected as second part.

*Note: The 8-bit parallel interface implementation of VINETIC®-x V1.4 is in contrast to typical Intel 8-bit interface implementations. Future VINETIC®-x versions will have the sequence of most and least significant byte for 8-bit interface types changed (least significant byte first followed by most significant byte).*

A correct interpretation of the commands and data is only possible if an even number of 8-bit words are received. If no even number of accesses to VINETIC®-x occurs, a host error is signaled (bit HOST-ERR in BXS2) and the command is discarded.

If software handshake is used, the RDYQ bit in register IR must be checked by the host before the next 8 bit interface access.

With 8-bit parallel interfaces reading of RDYQ (bit 7 of IR register) is also possible by DIA access. In this case only the lower 8 bits of the IR register will be returned. To fetch the complete 16 bit IR register the short command rIR has to be used.



**Figure 19 8-Bit Versus 16-Bit Timing (only CSQ and ADDR shown)**

### 6.1.3 Data Transfer Timing, Command Recovery Times

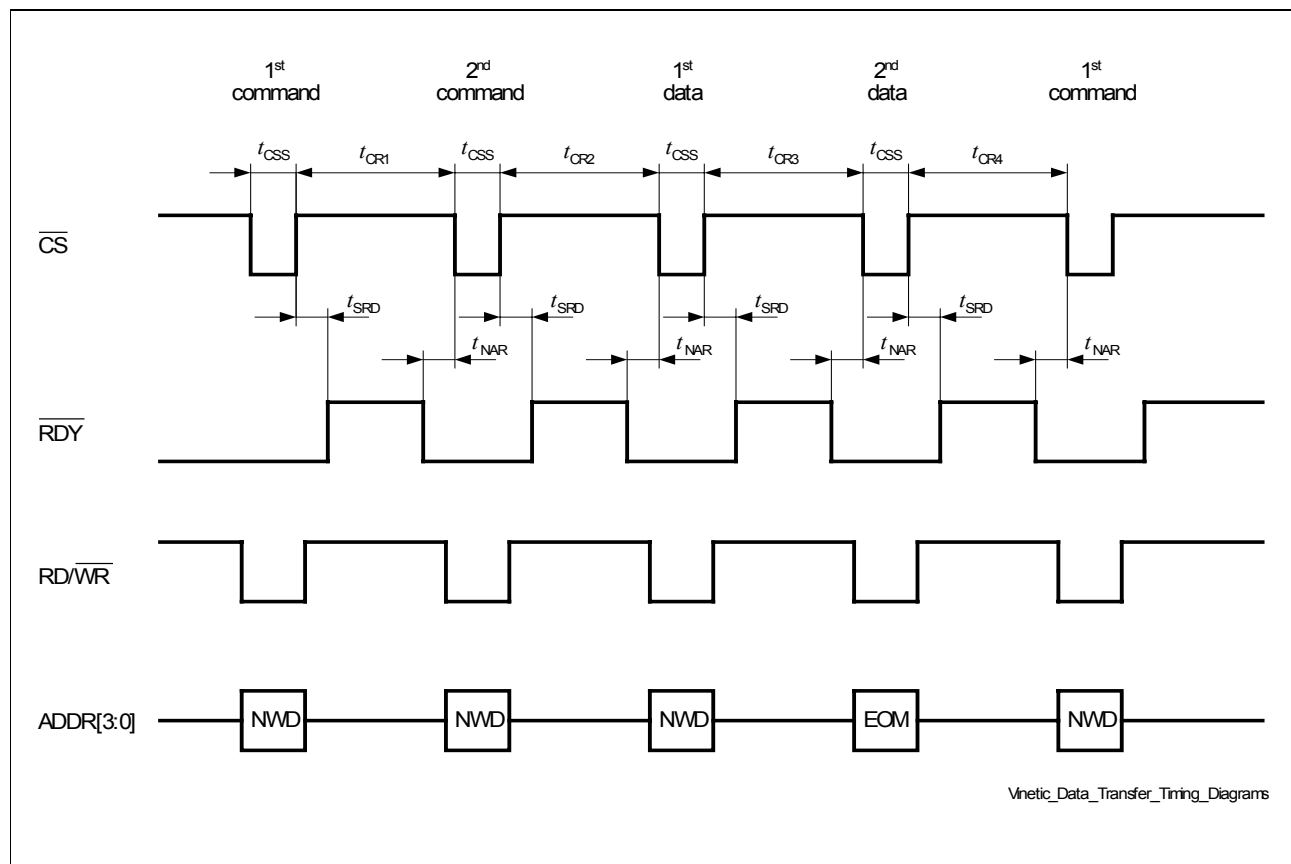
The following timing diagram depicts the command recovery times between commands, between command and data and between successive data accesses. The diagram refers to a Motorola interface but is transferable to all other types of parallel interfaces. The command recovery times for the 16-bit and the 8-bit interface types are the same.

For serial interfaces this command recovery times are not relevant. The timing for all interface types and signals is described in the *Preliminary Data Sheet*.

*Note: The EDSP reads only one command within 125  $\mu$ s from the command in mailbox. So the minimal logic delay between a read command and the actual possible read back of the data in the command out mailbox is > 125  $\mu$ s. With a read access via short commands (e.g. read ALM and EDSP status register) the response data is provided faster.*

*In the special case of DIA access to the IR register no command recovery time must be observed by the host.*




**Figure 20 Timing Diagrams for Data Transfer**
**Table 14 Timing Values for Data Transfer**

Parameter	Symbol	Limit Values without PCM		Limit Values with PCM		Unit
		Min.	Max.	Min.	Max.	
$\overline{CS}$ strobe pulse width	$t_{CSS}$	50	–	50	–	ns
1 <sup>st</sup> command ' 2 <sup>nd</sup> command	$t_{CR1}$	200	–	360	–	ns
Command ' 1 <sup>st</sup> data	$t_{CR2}$	670	–	1350	–	ns
Between two data accesses	$t_{CR3}$	410	–	780	–	ns
Last data/command ' next command	$t_{CR4}$	670	–	1350	–	ns
Strobe signal to $\overline{RDY}$ delay time	$t_{SRD}$		75		105	ns
Next access after interface ready	$t_{NAR}$	35	–	65	–	ns

## 6.2 Serial Interfaces

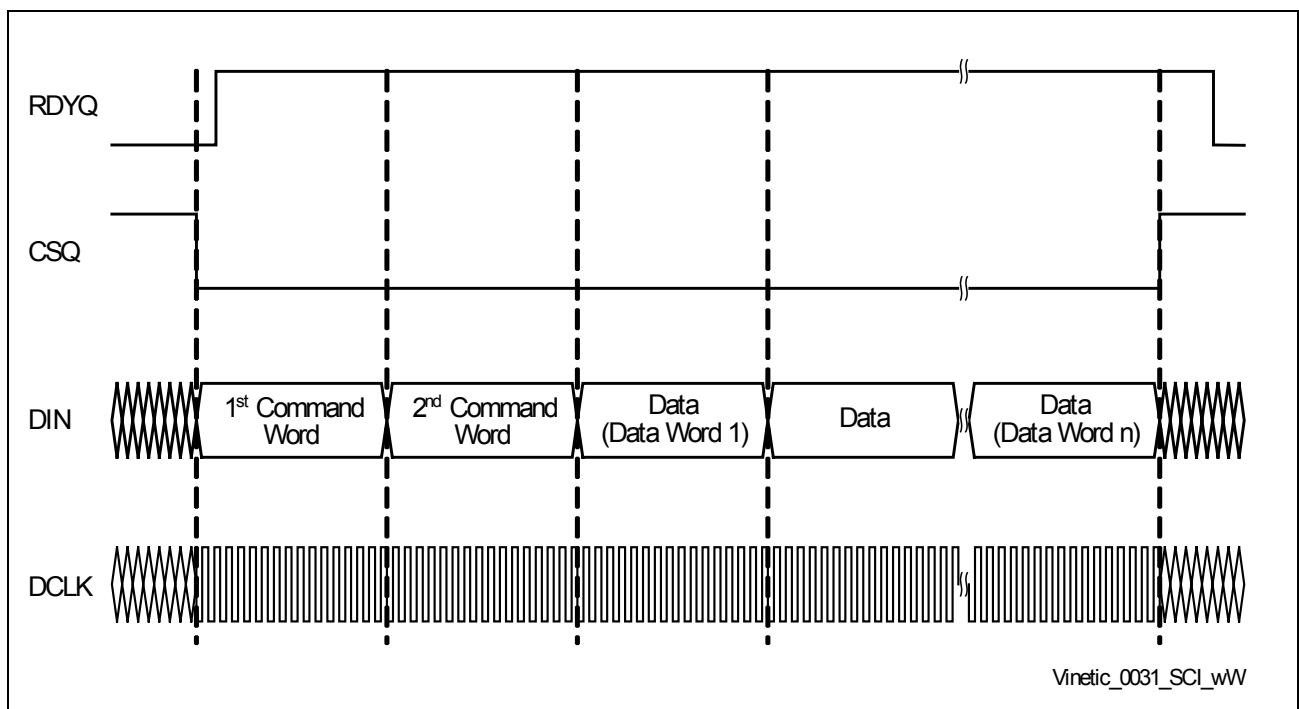
### 6.2.1 Serial $\mu$ C Interface

The VINETIC®-x micro controller serial interface (SCI) is electrically compatible with Infineon's DuSLIC® serial interface. The VINETIC® SCI also supports the slave mode of the SPI interface of the Motorola PowerQUICC™ family.

Using a serial interface the MSB (bit 15) of the command/data/packet-word is sent first.

**Figure 21** to **Figure 25** illustrate different accesses to the serial  $\mu$ C interface (the following command types and short commands are described in **Chapter 4**):

**Figure 21** shows a write access for SOP, COP, IOP, VOP, EVT and EOP commands (see **Table 4 on Page 49**), if the host wants to write data to the VINETIC®-x.



**Figure 21 Serial Control Interface Write-Command or Packet Write Access**

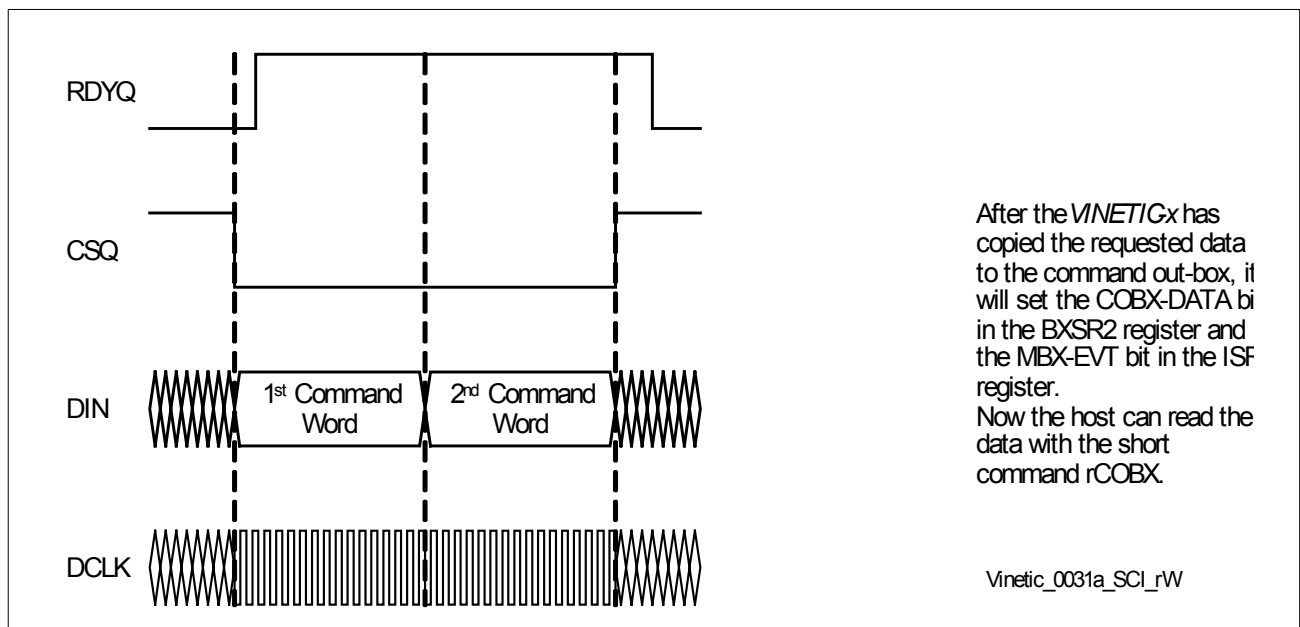
**Figure 22** illustrates the write access of the first and second command word for SOP, COP, IOP and EOP commands, if the host wants to read data from the VINETIC®-x. After the VINETIC®-x has prepared the requested data the host can read the data via the short command rPOBX or rCOBX (see also **Figure 25**). **Figure 23** shows the write access for short commands without data following (e.g. wMAXCBX, wMINCBX, wSTEDSP, wSWRST, wRESYNC...). A write access for short commands with data following (wLEMP, wLPMP) is illustrated in **Figure 24**. In **Figure 25** you can see a read access to the VINETIC®-x (rIR, rSR, rHWSR, rBXS, rSRGPIO, rPOBX, rCOBX...). In order to meet the requirements on command recovery time of the short command a "dump-word" (FFFF<sub>H</sub>) is filled in before the first data word. Data transfer starts with the first word following the "dump-word".

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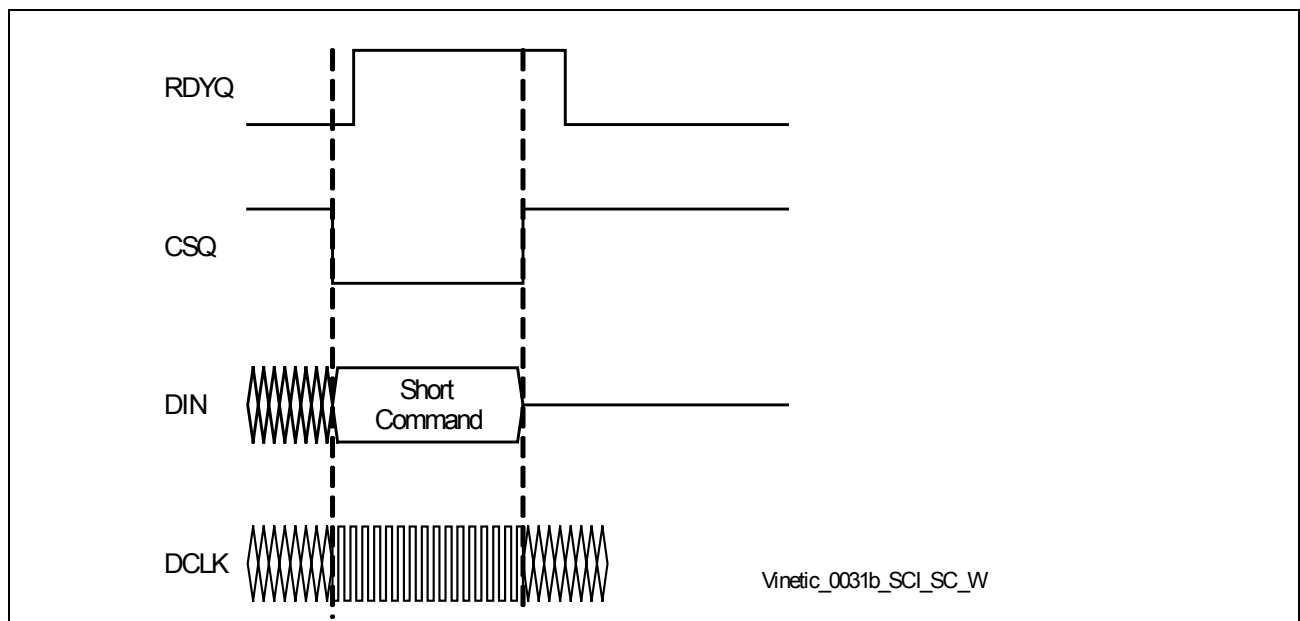
**Interface Description**

As the commands of the VINETIC®-x have different command recovery times the VINETIC®-x also supports HW handshake with the serial interface, similar to the parallel interface

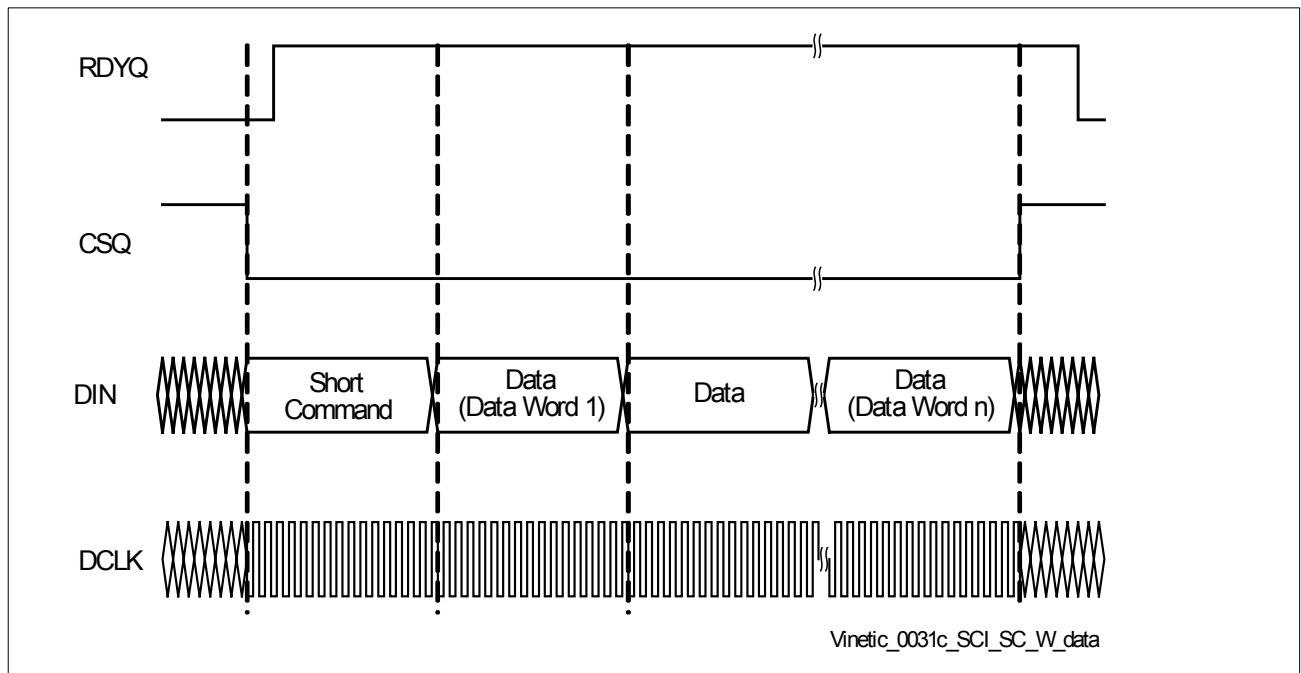
HW handshake is done via the RDYQ pin as described in *Preliminary Data Sheet*. The RDYQ bit reflects the status of the RDYQ pin. With the serial interface the RDYQ bit in the IR can only be read via short command “rIR”. If the RDYQ bit is zero, the VINETIC®-x is ready for the next command.



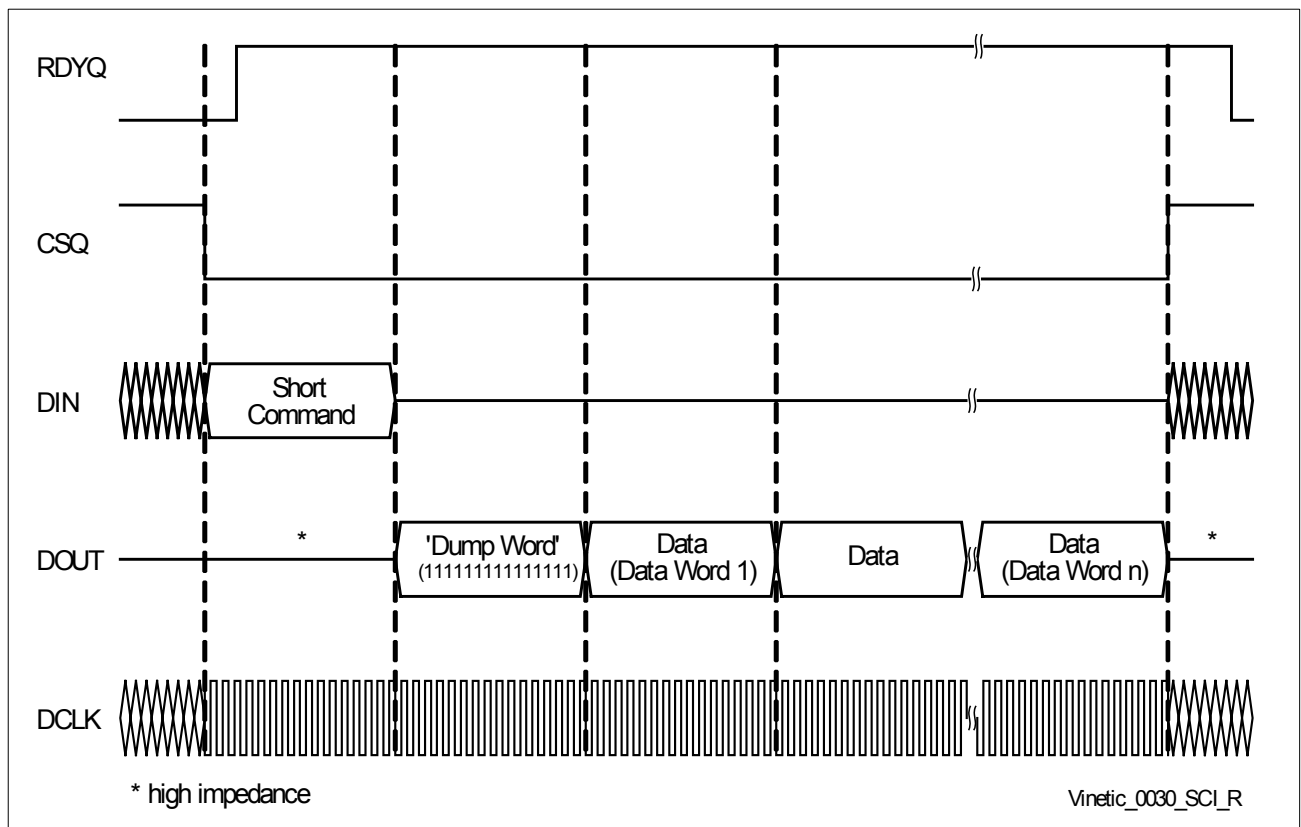
**Figure 22 Serial Control Interface Read-Command Write Access**



**Figure 23 Serial Control IF Short Command Write Access no Data Following**



**Figure 24 Serial Control IF Short Command Write Access with Data Following**



**Figure 25 Serial Control Interface Short Command Read Access**

### 6.2.2 PCM Interface

The serial PCM Interface is used to transfer A-Law or  $\mu$ -Law or ADPCM compressed voice data. The PCM Interface can also transfer linear data, in this case two consecutive PCM time slots are needed.

On all channels, bytes are serialized with the MSB first. As a default setting, the rising edge indicates the start of the bit, while the falling edge is used to buffer the contents of the received data on DR1 (DR2). If double clock rate is selected (PCLK clock rate is twice the data rate), the first rising edge indicates the start of a bit, while, by default, the second falling edge is used to buffer the contents of the data line DR1 (DR2).

The VINETIC®-x supports two<sup>1)</sup> PCM-highways. The data rate of the interface can vary from 256 kbit/s to 8192 kbit/s for each highway. A frame may consist of up to 128 time slots of 8 bits each. The time slot and PCM highway assignment for each VINETIC®-x channel can be programmed. Receive and transmit time slots can also be programmed individually (see *Preliminary User's Manual - EDSP Firmware Description*).

**Table 15** gives examples for possible PCM Interface settings. Other frequencies between 512 kHz and 8 MHz are also possible, and can be calculated by the formula  $f_{PCLK}[\text{kHz}] = 512 \cdot n$  kHz for  $n = 1 \dots 16$ . The number of possible time slots for a given clock rate ( $f_{PCLK}$ ) is calculated with the formulas:

- $f_{PCLK}/64$  for single Clock and,
- $f_{PCLK}/128$  for double clock.

**Table 15 VINETIC®-x PCM Interface Configuration**

<b>Clock Rate PCLK</b> [kHz]	<b>Single/Double</b> <b>Clock</b> [1/2]	<b>Time Slots</b> [per highway]	<b>Data Rate</b> [kbit/s per highway]
512	2	4	256
512	1	8	512
1024	2	8	512
1024	1	16	1024
2048	2	16	1024
2048	1	32	2048
4096	2	32	2048
4096	1	64	4096
8192	2	64	4096
8192	1	128	8192

<sup>1)</sup> VINETIC®-2CPE provides only one PCM highway

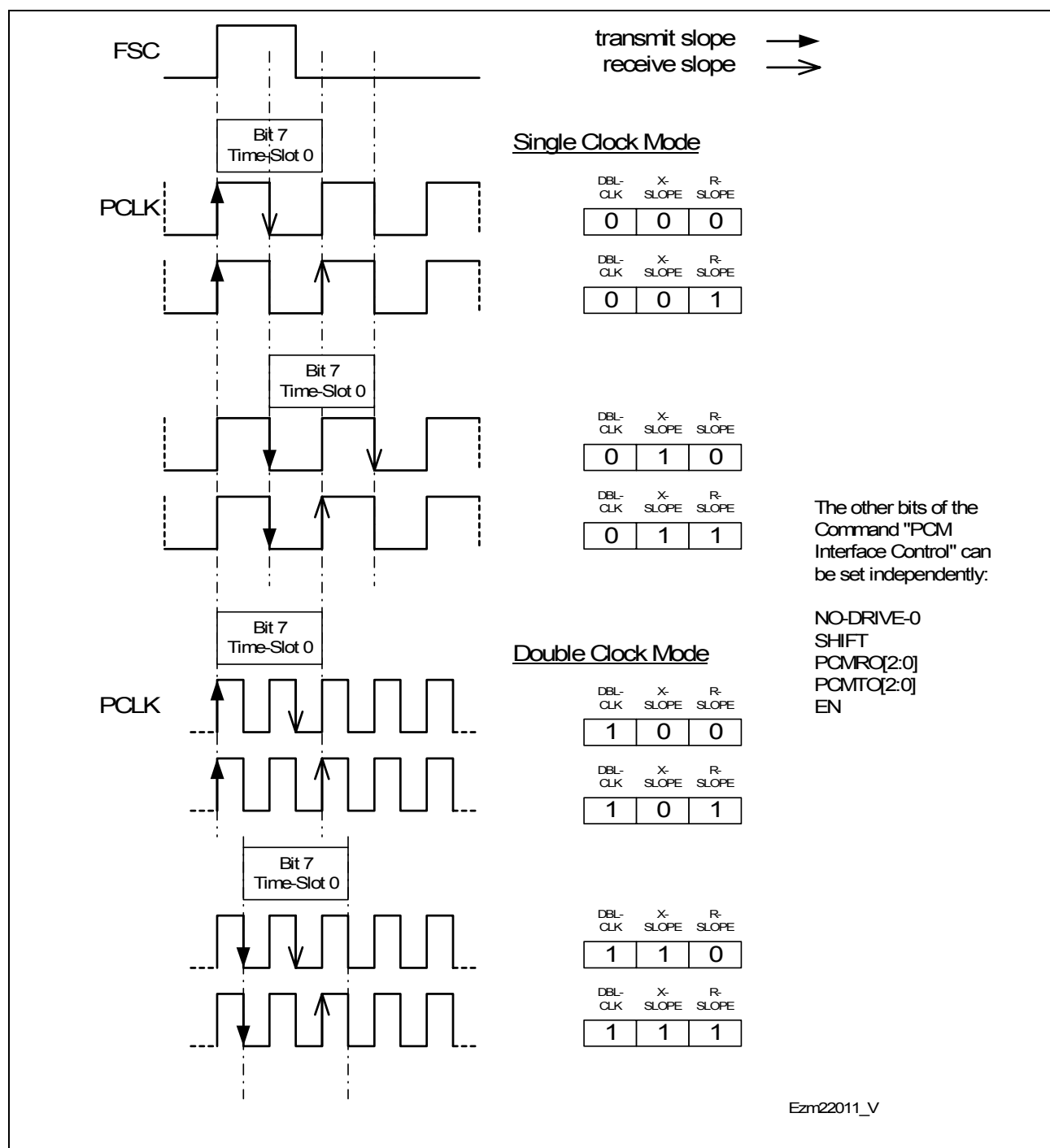


Figure 26 Setting the Slopes with the Command "PCM Interface Control"

## 7 Register Description

This chapter provides an overview and a detailed description of the registers that are necessary to configure and operate the VINETIC®-x devices. VINETIC®-x provides four types of registers which are grouped by the type of access command used to read or write the register content:

- Registers accessed by SOP command
- Registers accessed by COP command
- Registers accessed by IOP Command
- Registers accessed with Short commands

The register description format is explained in [“Register Description Format” on Page 251](#).

### Registers Accessed by SOP Commands

With SOP commands the registers of the Analog Line Modules (ALM) can be configured. All registers are channel-specific (Allocation C). The command syntax is described in [Chapter 4.4 on Page 63](#). A registers overview is given in [Table 16 on Page 96](#).

### Registers Accessed by COP Commands

All CRAM coefficients can be computed with the VINETICOS tool, which enables an easy generation of the required coefficients. After generation, all coefficients can be downloaded to the CRAM via COP (Coefficient OPeration) commands. A registers overview is given in [Table 24 on Page 157](#). All Coefficient RAM locations in [Table 24 on Page 157](#) marked with *“Coefficient will be set via Coefficient RAM download”* have to be computed with VINETICOS all other register locations can be set individually by the host.

### Registers Accessed by IOP Commands

With IOP commands the registers of the PHI can be accessed. “Mask” registers are used to suppress interrupt indications. “Common” registers and “Other” PHI related registers are used to configure device specific settings.

Depending on their functions, the registers can have the Allocation C (channel specific, four registers), R (Resource specific, eight registers) or D (Device specific, one register). A registers overview is given in [Table 16 on Page 96](#)

### Registers Accessed with Short Commands

With short commands the “Status-”, “Operating Mode-” and “Handshake-” registers of the PHI can be accessed. Since short commands are not handled via the command mailbox and consist only of the first command word (see [Chapter 4.1.4 on Page 38](#)), a fast access to important chip informations is achieved. A summary of all provided short

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**Register Description**

commands is given in [Table 5 on Page 50](#). The response to the Short commands is detailed in [Chapter 4.2.4 on Page 42](#).

Depending on their functions, the registers can have the Allocation C (channel specific), R (Resource specific) or D (Device specific). For registers overview see [Table 16 on Page 96](#)

**Notes:**

1. The command syntax for SOP, COP and IOP command is described in [Chapter 4.4 on Page 63](#). Depending on the values of the OFFSET-field and LENGTH-field in the command, either one single register (OFFSET = register address, LENGTH = 1) or multiple registers (LENGTH > 1) can be written or read.  
With SOP, COP and IOP Commands the BC bit (broadcast) is supported by the write access (R/W=0) only. No broadcast read access is supported with those commands.
2. With Short Commands the BC bit (broadcast) is only supported with the read access (R/W=1). No broadcast write access is supported with short commands.
3. Register access to addresses/offsets which are not assigned has to be avoided in any case! Multi register access which read or write unassigned offsets are prohibited, those accesses may cause unpredictable behavior of the device.

## 7.1 Register Overview

**Table 16 VINETIC®-x Registers Accessed with SOP-, IOP- and Short Commands**

Register Short Name	Register Long Name	Offset or Short Cmd.	Description see
<b>Registers Accessed with SOP Commands</b>			
DCCHKR	DCCTL-PRAM Checksum Register	00 <sub>H</sub>	<a href="#">Page 101</a>
DSCHKR	DSP-PRAM Checksum Register	01 <sub>H</sub>	<a href="#">Page 102</a>
CCR	Common Configuration Register	02 <sub>H</sub>	<a href="#">Page 103</a>
LMRES	Level Metering Result	03 <sub>H</sub>	<a href="#">Page 104</a>
CCHKR	CRAM Checksum Register	04 <sub>H</sub>	<a href="#">Page 105</a>
IOCTL1	I/O Control Register 1	05 <sub>H</sub>	<a href="#">Page 106</a>
IOCTL2	I/O Control Register2	06 <sub>H</sub>	<a href="#">Page 110</a>
BCR1	Basic Configuration Register 1	07 <sub>H</sub>	<a href="#">Page 113</a>
BCR2	Basic Configuration Register 2	08 <sub>H</sub>	<a href="#">Page 120</a>
DSCR	DTMF Sender Configuration Register	09 <sub>H</sub>	<a href="#">Page 124</a>



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**Register Description**
**Table 16 VINETIC®-x Registers Accessed with SOP-, IOP- and Short Commands (cont'd)**

<b>Register Short Name</b>	<b>Register Long Name</b>	<b>Offset or Short Cmd.</b>	<b>Description see</b>
LMCR	Level Metering Configuration Register	0A <sub>H</sub>	<a href="#">Page 127</a>
RTR	Ring Configuration Register	0B <sub>H</sub>	<a href="#">Page 130</a>
OFR	DC Offset Register	0C <sub>H</sub>	<a href="#">Page 134</a>
AUTOMOD	Automatic Mode Register	0D <sub>H</sub>	<a href="#">Page 135</a>
TSTR1	Test Register 1	0E <sub>H</sub>	<a href="#">Page 138</a>
TSTR2	Test Register 2	0F <sub>H</sub>	<a href="#">Page 141</a>
TSTR3	Test Register 3	10 <sub>H</sub>	<a href="#">Page 144</a>
AUTOMET CONF	Auto Metering Configuration Register	1A <sub>H</sub>	<a href="#">Page 146</a>
AUTORING CONF1	Auto Ring Cadence 1 Configuration Register	1B <sub>H</sub>	<a href="#">Page 149</a>
AUTORING CONF2	Auto Ring Cadence 2 Configuration Register	1C <sub>H</sub>	<a href="#">Page 150</a>
AUTORING CONF3	Auto Ring Cadence 3 Configuration Register	1D <sub>H</sub>	<a href="#">Page 151</a>
AUTORING CONF4	Auto Ring Cadence 3 Configuration Register	1E <sub>H</sub>	<a href="#">Page 152</a>
AUTORING CONF5	Auto Ring Cadence 5 Configuration Register	1F <sub>H</sub>	<a href="#">Page 153</a>

**Registers Accessed with IOP Command- Mask Registers**

MR-SRE1	Mask Register for Status Register for EDSP Interrupts 1 (rising edge) [M-V-CPE]	00 <sub>H</sub>	<a href="#">Page 160</a>
MR-SRE2	Mask Register for Status Register for EDSP Interrupts 2 (rising edge) [M-V-CPE]	01 <sub>H</sub>	<a href="#">Page 163</a>
MR-SRS1	Mask Register for Status Register for Analog-Line-Module Interrupts 1 (rising edge)	02 <sub>H</sub>	<a href="#">Page 165</a>

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**Register Description**
**Table 16 VINETIC®-x Registers Accessed with SOP-, IOP- and Short Commands (cont'd)**

<b>Register Short Name</b>	<b>Register Long Name</b>	<b>Offset or Short Cmd.</b>	<b>Description see</b>
MR-SRS2	Mask Register for Status Register for Analog-Line-Module Interrupts 2 (rising edge)	03 <sub>H</sub>	<a href="#">Page 167</a>
MR-HWSR1	Mask Register for Hardware Status Register 1 (rising edge)	12 <sub>H</sub>	<a href="#">Page 168</a>
MR-HWSR2	Mask Register for Hardware Status Register 2 (rising edge)	13 <sub>H</sub>	<a href="#">Page 169</a>
MR-BXSR1	Mask Register for Mailbox Status Register 1 (rising edge) [M-V-CPE]	16 <sub>H</sub>	<a href="#">Page 170</a>
MR-BXSR2	Mask Register for Mailbox Status Register 2 (rising edge)	17 <sub>H</sub>	<a href="#">Page 171</a>
MR-SRGPIO	Mask Register for Status Register for GPIO Interrupts (rising edge)	1A <sub>H</sub>	<a href="#">Page 172</a>
MF-SRE1	Mask Register for Status Register for EDSP Interrupts 1 (falling edge) [M-V-CPE]	60 <sub>H</sub>	<a href="#">Page 173</a>
MF-SRE2	Mask Register for Status Register for EDSP Interrupts 2 (falling edge) [M-V-CPE]	61 <sub>H</sub>	<a href="#">Page 175</a>
MF-SRS1	Mask Register for Status Register for Analog-Line-Module Interrupts 1 (falling edge)	62 <sub>H</sub>	<a href="#">Page 177</a>
MF-SRS2	Mask Register for Status Register for Analog-Line-Module Interrupts 2 (falling edge)	63 <sub>H</sub>	<a href="#">Page 179</a>
MF-HWSR1	Mask Register for Hardware Status Register 1 (falling edge)	72 <sub>H</sub>	<a href="#">Page 180</a>
MF-HWSR2	Mask Register for Hardware Status Register 2 (falling edge)	73 <sub>H</sub>	<a href="#">Page 181</a>
MF-BXSR1	Mask Register for Mailbox Status Register 1 [M-V-CPE]	76 <sub>H</sub>	<a href="#">Page 182</a>
MF-BXSR2	Mask Register for Mailbox Status Register 2 (falling edge)	77 <sub>H</sub>	<a href="#">Page 183</a>

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**Register Description**
**Table 16 VINETIC®-x Registers Accessed with SOP-, IOP- and Short Commands (cont'd)**

<b>Register Short Name</b>	<b>Register Long Name</b>	<b>Offset or Short Cmd.</b>	<b>Description see</b>
MF-SRGPIO	Mask Register for Status Register for GPIO Interrupts (falling edge)	7A <sub>H</sub>	<a href="#">Page 184</a>

**Registers Accessed with IOP Commands - Common Register**

OPMOD-SRC	Operating Mode Status Register Source	20 <sub>H</sub>	<a href="#">Page 186</a>
OPMOD-CUR	Operating Mode Status Register Current	21 <sub>H</sub>	<a href="#">Page 187</a>
REVISION	Revision Number (read-only)	40 <sub>H</sub>	<a href="#">Page 188</a>
CHIPID1	Chip Identification 1 (read-only)	41 <sub>H</sub>	<a href="#">Page 189</a>
CHIPID2	Chip Identification 2 (read-only)	42 <sub>H</sub>	<a href="#">Page 189</a>
CHIPID3	Chip Identification 3 (read-only)	43 <sub>H</sub>	<a href="#">Page 189</a>
GCONF	Global Configuration Register	44 <sub>H</sub>	<a href="#">Page 190</a>
EDSPFUSE	EDSP Fuse Register	45 <sub>H</sub>	<a href="#">Page 192</a>
PLLCTRL	PLL Control Register	46 <sub>H</sub>	<a href="#">Page 192</a>

**Registers Accessed with IOP Command - Other PHI Related Registers**

GCR1	GPIO Configuration Register 1	47 <sub>H</sub>	<a href="#">Page 193</a>
GCR2	GPIO Configuration Register 2	48 <sub>H</sub>	<a href="#">Page 195</a>
PHICKR	PHI PRAM Checksum Register	49 <sub>H</sub>	<a href="#">Page 198</a>

**Status Registers accessed with Short Commands**

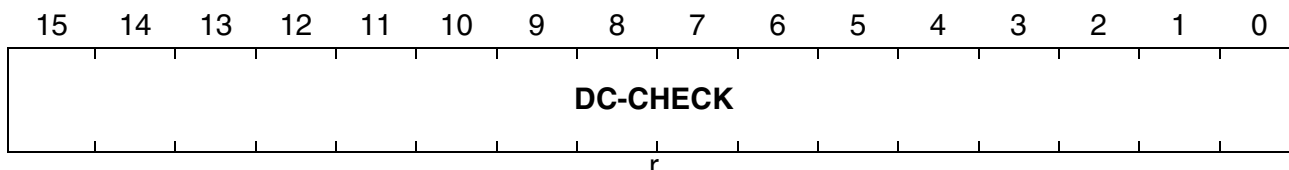
IR	Interrupt Register	rIR	<a href="#">Page 199</a>
SRE1	Status Register for EDSP 1	rSR	<a href="#">Page 204</a>
SRE2	Status Register for EDSP 2	rSR	<a href="#">Page 209</a>
SRS1	Status Register for Analog-Line-Module 1	rSR, rSRS	<a href="#">Page 214</a>
SRS2	Status Register for Analog-Line-Module 2	rSR, rSRS	<a href="#">Page 217</a>
HWSR1	Hardware Status Register 1	rHWSR	<a href="#">Page 219</a>
HWSR2	Hardware Status Register 2	rHWSR	<a href="#">Page 221</a>
BXSR1	Mailbox Status Register 1	rBXSR	<a href="#">Page 223</a>
BXSR2	Mailbox Status Register 2	rBXSR	<a href="#">Page 224</a>
SRGPIO	Status Register for GPIO	rSRGPIO	<a href="#">Page 226</a>

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**Register Description**

**Table 16      VINETIC®-x Registers Accessed with SOP-, IOP- and Short Commands (cont'd)**

<b>Register Short Name</b>	<b>Register Long Name</b>	<b>Offset or Short Cmd.</b>	<b>Description see</b>
I-SRE1	Interrupt Status Register for EDSP 1	rl-SR	<a href="#">Page 228</a>
I-SRE2	Interrupt Status Register for EDSP 2	rl-SR	<a href="#">Page 230</a>
I-SRS1	Interrupt Status Register for Analog-Line-Module 1	rl-SR, rl-SRS	<a href="#">Page 233</a>
I-SRS2	Interrupt Status Register for Analog-Line-Module 2	rl-SR, rl-SRS	<a href="#">Page 235</a>
I-HWSR1	Hardware Interrupt Status Register 1	rl-HWSR	<a href="#">Page 236</a>
I-HWSR2	Hardware Interrupt Status Register 2	rl-HWSR	<a href="#">Page 237</a>
I-BXSR1	Mailbox Interrupt Status Register 1	rl-BXSR	<a href="#">Page 238</a>
I-BXSR2	Mailbox Interrupt Status Register 2	rl-BXSR	<a href="#">Page 239</a>
I-SRGPIO	Interrupt Status Register for GPIO	rl-SRGPIO	<a href="#">Page 240</a>
<b>Registers Accessed with Short Commands - Handshake Registers</b>			
FIBXMS	Free In-Box-Memory Space Register	rFIBXMS	<a href="#">Page 241</a>
OBXML	Out-Box Message Length Register	rOBXML	<a href="#">Page 242</a>

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**7.2 Register Accessed with SOP Commands (ALM)<sup>1)</sup>**
**DCCHKR (Allocation M)**
**DCCTL-PRAM Checksum Register (00<sub>H</sub>)** **Reset Value: 0000<sub>H</sub>**


Field	Bits	Type	Description
DC-CHECK	[15:0]	r	DCCTL-PRAM checksum

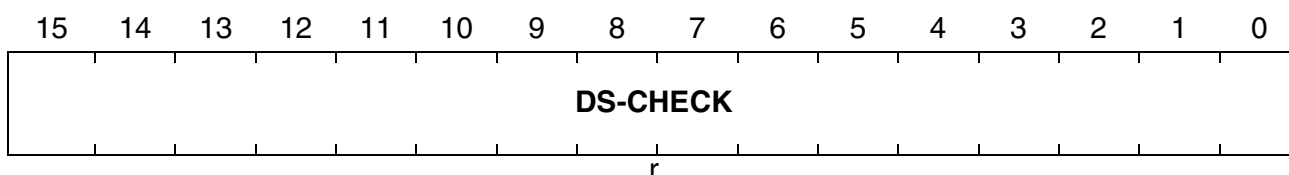
As an option, the DCCTL micro program extensions can be downloaded to a program RAM. To verify the download and to check the RAM during operation a checksum for the DCCTL software is calculated.

Immediately after a DCCTL download, the checksum can be verified with the command EOP-Command "CRC FPI" (command description see *Preliminary User's Manual - EDSP Firmware Description*). The checksum in SOP register DCCHKR is only available if the download has been enabled for a specific channel (BCR1:PRAM-DCC = 1). After enabling the download, reading of register DCCHKR offers a convenient way to check if the DCCTL program RAM has been corrupted.

The checksum is generated in hardware by a 16-bit MISR. The used polynomial is:  $x^{16}+x^5+x^3+x^2+1$ . The internal reference checksum is calculated once after download. During normal operation the checksum is calculated continuously and checked against the reference checksum. If a mismatch is detected an interrupt is generated (status bit CS-FAIL-DCCTRL in SRS2). The DCCTRL checksum generation takes up to 2 ms.

*Note: A detailed description of the download procedure and checksum calculation for the EDSP, PHI, DCCTL DSP and Coefficient RAM is available on request in form of an application note. Please note that the checksum algorithms are different for CRC FPI and register DCCHKR*

<sup>1)</sup> For VINETIC®-x Version 1.4 devices all SOP registers are set to 0000<sub>H</sub> after a reset, and do not coincide with the default values documented in this User's Manual. Therefore after any reset (hard or soft reset) the SOP registers need to be re initialized to their default values or the values required for the application.

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**DSCHKR (Allocation M)**
**DSP-PRAM Checksum Register**
**(01<sub>H</sub>)**
**Reset Value: 0000<sub>H</sub>**


Field	Bits	Type	Description
DS-CHECK	[15:0]	r	DSP-PRAM Checksum

As an option, parts of the Analog Line Module DSP Software can be downloaded to a Program RAM. To verify the download and to check the RAM during operation a checksum for the DSP software is calculated.

The checksum is calculated in hardware by a 16-bit MISR. The used polynomial is:  $x^{16}+x^5+x^3+x^2+1$ . The internal reference checksum is calculated once after download. During normal operation the checksum is calculated continuously and checked against the reference checksum. If a mismatch is detected an interrupt is generated (status bit CS-FAIL-DSP in SRS2). The DSP checksum generation takes up to 0.5 ms.

The algorithm of the checksum generation is:

```

For (ram_adr=0; ram_adr < max; ram_adr++) {
  ram_dat = ram[ram_adr];
  if (csum[15:0] & 0x8000)
    csum = csum<<1 XOR ram_dat XOR 0x002D;
  else
    csum = csum<<1 XOR ram_dat;
}

```

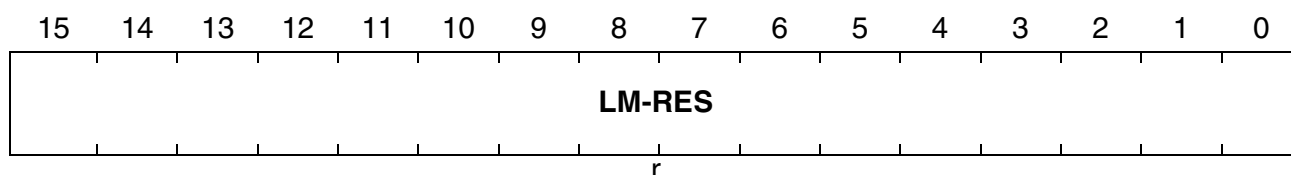
Note: For detailed documentation of the ALM DSP download and checksum see [“Download of DCCTL Program Code \(optional\)” on Page 27](#).

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**CCR (Allocation M)**
**Common Configuration Register**
**(02<sub>H</sub>)**
**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
rw							
7	6	5	4	3	2	1	0
0	0	JUMP-DC	JUMP-AC3	JUMP-AC2	JUMP-AC1	PD-CVCM	PD-CBIAS
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
JUMP-DC	5	(rw)	<b>Jump on DC</b> For internal use only. Must be set to 0 <sup>1)</sup> .
JUMP-AC3	4	(rw)	<b>Jump on AC3</b> For internal use only. Must be set to 0 <sup>1)</sup> .
JUMP-AC2	3	(rw)	<b>Jump on AC2</b> For internal use only. Must be set to 0 <sup>1)</sup> .
JUMP-AC1	2	(rw)	<b>Jump on AC1</b> For internal use. Must be set to 0 <sup>1)</sup> .
PD-CVCM	1	rw	<b>Power Down of VCM and VREF Buffer</b> (inside the central biasing). This bit has no effect unless the TEST-EN bit in register BCR1 is set to 1. 0 VCM and VREF buffer active 1 VCM and VREF buffer power down
PD-CBIAS	0	rw	<b>Central Biasing Power Down</b> This bit has no effect unless the TEST-EN bit in register BCR1 is set to 1. 0 Central biasing active 1 Central biasing power down

<sup>1)</sup> If a patch for the ALM-DSP is supplied and downloaded, the corresponding JUMP bit has to be set to 1.

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**LMRES (Allocation C)**
**Level Metering Result**
**(03<sub>H</sub>)**
**Reset Value: 0000<sub>H</sub>**


Field	Bits	Type	Description
<b>LM-RES</b>	[15:0]	r	<b>LM Result</b> Selected by the LM-SEL bits in the LMCR register

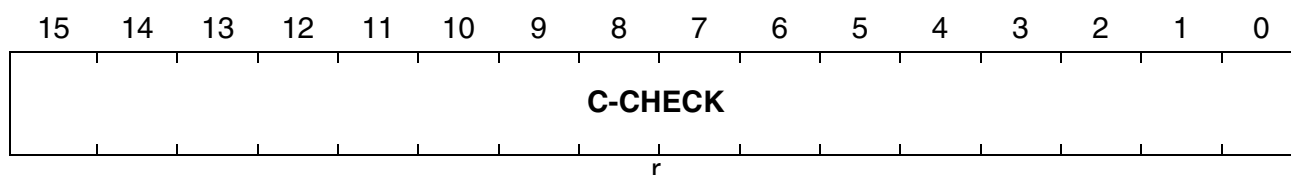
The result of any measurement can be read via this register. It gives a 16-bit value coded in two's complements. For the interpretation of the result and the level meter settings refer to the document *Preliminary User's Manual - System Reference*.

**Table 17      Level Metering Result Value Range**

Negative Value Range		Positive Value Range	
<b>– Full-scale</b>			<b>+ Full-scale</b>
8000 <sub>H</sub>	FFFF <sub>H</sub>	0000 <sub>H</sub>	7FFF <sub>H</sub>
–32768	–1	0	+32767

*Note: Timing Requirements: To ensure the correct function with level metering, consecutive SOP commands for the ALM modules must be sent by the host with time gaps of  $\geq 2$  ms.*



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**CCHKR (Allocation C)**
**CRAM Checksum Register**
**(04<sub>H</sub>)**
**Reset Value: 0000<sub>H</sub>**


Field	Bits	Type	Description
C-CHECK	[15:0]	r	<b>CRAM checksum</b> The value is MSB-LSB reversed. E.g. if the CRAM checksum is 1234 <sub>H</sub> the value returned in <b>C-CHECK</b> is 2C48 <sub>H</sub>

The coefficients that determine the AC and DC behavior are stored in a RAM. To ensure the consistency during operation a checksum for the CRAM is calculated.

The checksum is calculated in hardware by a 16-bit MISR. The used polynomial is:  $x^{16}+x^5+x^3+x^2+1$ . The internal reference checksum is calculated once after download. During normal operation the checksum is calculated continuously and checked against the reference checksum. If a mismatch is detected an interrupt is generated (status bit CS-FAIL-CRAM in SRS2). The CRAM checksum generation takes up to 2 ms.

The algorithm of the checksum generation is:

```

For (ram_adr=0; ram_adr < max; ram_adr++) {
  ram_dat = ram[ram_adr];
  if (csum[15:0] & 0x8000)
    csum = csum<<1 XOR ram_dat XOR 0x002D;
  else
    csum = csum<<1 XOR ram_dat;
}
  
```

*Note: For the correct behavior the following steps must be executed.*

- 1.) download of CRAM coefficients of both ALM channels.
- 2.) switch to CRAM coefficients (CRAM-EN in register BCR2)
- 3.) dummy download (at least one access to CRAM). After this, the correct reference checksum will be calculated.

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**IOCTL1 (Allocation C)**
**I/O Control Register 1**
**(05<sub>H</sub>)**
**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
0	0	0	INEN-IO4	INEN-IO3	INEN-IO2	INEN-IO1	INEN-IO0

rw

7	6	5	4	3	2	1	0
0	0	0	OEN-IO4	OEN-IO3	OEN-IO2	OEN-IO1	OEN-IO0

rw

Field	Bits	Type	Description
INEN-IO4	12	rw	<b>Input Enable IO4</b> Enables digital input for programmable I/O pin IO4 with analog functionality. 0 Input pin IO4 is disabled. 1 Input pin IO4 is enabled.
INEN-IO3	11	rw	<b>Input Enable Schmitt-Trigger IO3</b> Enables digital input for programmable I/O pin IO3 with analog functionality. 0 Input pin IO3 is disabled. 1 Input pin IO3 is enabled.
INEN-IO2	10	rw	<b>Input Enable Schmitt-Trigger IO2</b> Enables digital input for programmable I/O pin IO2 with analog functionality. 0 Input pin IO2 is disabled. 1 Input pin IO2 is enabled.
INEN-IO1	9	rw	<b>Input Enable Schmitt-Trigger IO1</b> Enables digital input for programmable I/O pin IO1. 0 Input pin IO1 is disabled. 1 Input pin IO1 is enabled.
INEN-IO0	8	rw	<b>Input Enable Schmitt-Trigger IO0</b> Enables digital input for programmable I/O pin IO0. 0 Input pin IO0 is disabled. 1 Input pin IO0 is enabled.

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Field	Bits	Type	Description
<b>OEN-IO4</b>	4	rw	<b>Output Driver IO4</b> Enables output driver of the IO4 pin. 0 The output driver of the IO4 pin is disabled. 1 The output driver of the IO4 pin is enabled.
<b>OEN-IO3</b>	3	rw	<b>Output Driver IO3</b> Enables output driver of the IO3 pin. 0 The output driver of the IO3 pin is disabled. 1 The output driver of the IO3 pin is enabled.
<b>OEN-IO2</b>	2	rw	<b>Output Driver IO2</b> Enables output driver of the IO2 pin. 0 The output driver of the IO2 pin is disabled. 1 The output driver of the IO2 pin is enabled.
<b>OEN-IO1</b>	1	rw	<b>Output Driver IO1</b> Enables output driver of the IO1 pin. If external ringing is selected (bit REXT-EN in register RTR set to 1), pin IO1 cannot be controlled by the user but is utilized by the VINETIC®-x to control the ring relay. 0 The output driver of the IO1 pin is disabled. 1 The output driver of the IO1 pin is enabled.
<b>OEN-IO0</b>	0	rw	<b>Output Driver IO0</b> Enables output driver of the IO0 pin. If SLIC-P is selected (see bits SEL-SLIC [3:0] in register BCR1), pin IO0 cannot be controlled by the user but is utilized by the VINETIC®-x to control the C3 input of SLIC-P. Exception: In case of extremely low power applications without current limitation (bits SEL-SLIC [3:0] in register BCR1 = 0011 or 0111) the IO0 pin is not controlled by the VINETIC®-x. 0 The output driver of the IO0 pin is disabled. 1 The output driver of the IO0 pin is enabled.

**Note:**

1. If input and output of the same IO pin are enabled, the actual output value will be reflected in the corresponding bit of SRS1.  
 Digital inputs which are disabled will return a "1" in the Status Register.
2. If IO3, IO4 or IO2 are utilized as analog input for line testing, the corresponding IO must not be configured as digital input nor as digital output (INEN-IOx=0,

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*OEN\_IOx=0). The settings in register IOCTL1 only configure the digital function of the pin.*

Without a download of a micro program extension to the Analog Line Module (DCCTL) VINETIC® supports SLIC-E/-E2, SLIC-S/-S2, SLIC-P and GEMINAX-S/S2.

With a download of a micro program extension to the Analog Line Module (DCCTL) VINETIC® supports SLIC-E/-E2, SLIC-S/-S2, SLIC-P, GEMINAX-S/-S2, SLIC-LCP and GEMINAX-S MAX.

**Table 18 Usage of IO Pins for SLIC Control, Line Testing and Ringing**

**Proposed Usage of VINETIC® IOs**

SLIC	IO0	IO1	IO2	IO3	IO4
SLIC-E/-E2 SLIC-S/-S2	—	Ring relay	Ring current sense	Line test	Line test
SLIC-P	C3	Ring relay	Ring current sense	Line test	Line test
SLIC-P (power sensitive)	—	Ring relay	Ring current sense	Line test	Line test
SLIC-LCP	LCAS	C3	Line test	Line test	Line test

**Automatic Control from DCCTL**

**Standard with no External Ringing (REXT-EN=0) and no IOs used for Line Testing**

SLIC	IO0	IO1	IO2	IO3	IO4
SLIC-E/-E2 SLIC-S/-S2	—	—	—	—	—
SLIC-P	C3	—	—	—	—

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**Table 18 Usage of IO Pins for SLIC Control, Line Testing and Ringing (cont'd)**
**Proposed Usage of VINETIC® IOs**

SLIC	IO0	IO1	IO2	IO3	IO4
------	-----	-----	-----	-----	-----

**Automatic Control from DCCTL**

**External Ringing with relays (REXT-EN=1, LCAS-EN=0) and no IOs used for Line Testing**

SLIC	IO0	IO1	IO2	IO3	IO4
SLIC-E/-E2 SLIC-S/-S2	–	Ring relay	Ring current sense	–	–
SLIC-P (power sensitive)	–	Ring relay	Ring current sense	–	–
SLIC-LCP	–	C3	–	–	–

**Automatic Control from DCCTL**

**External Ringing with LCAS (REXT-EN=1, LCAS-EN=1)**

SLIC	IO0	IO1	IO2	IO3	IO4
SLIC-LCP	LCAS	C3	Ring current sense	–	–

**Table 19 Usage of VINETIC GPIO Pins**

GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO6	GPIO7
				HOOKA <sup>1)</sup>	HOOKB <sup>1)</sup>	HOOKC <sup>1)</sup>	HOOKD <sup>1)</sup>

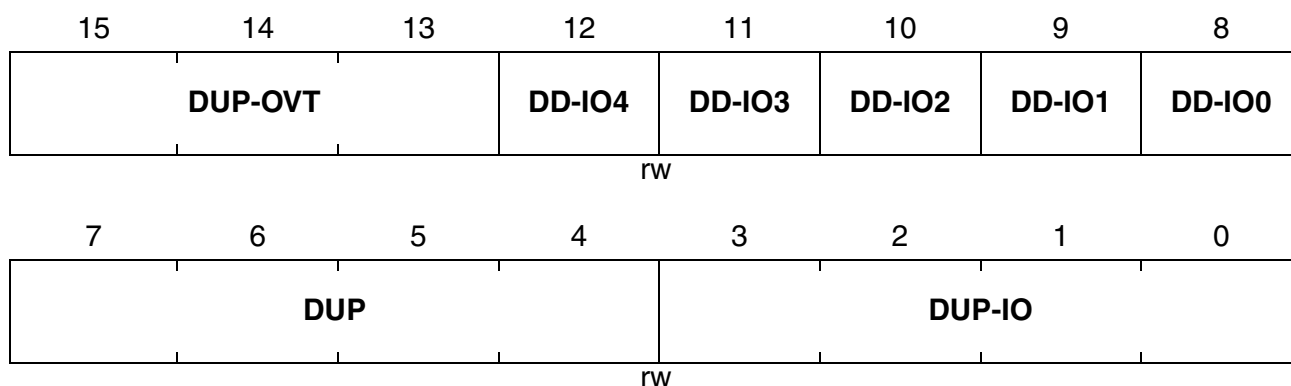
<sup>1)</sup> HOOKx-EN=1 (x= A,B,C,D) in register GCONF.

HOOKx-EN bits are implemented for signaling of hook indication of the channel specific HOOK bit (SRS1[13]) on the GPIO pins GPIO[4:7]. In this case exactly the filtered HOOK information is mirrored to the GPIO pins. The maximum delay between hook detection and the signaling on the GPIO pins is 750 µs.

**SLIC-LCP**

If SLIC-LCP is selected, the IO1 pin is reserved to control C3 pin of the SLIC-LCP. SLIC-LCP supports external ringing only (REXT-EN=1). VINETIC®-x supports the control of LCAS devices (LCAS-EN=1) or relay (LCAS-EN=0) for switching the ring generator to the Ring/Trip wires.

- LCAS-EN=1:  
IO0 is reserved for additional control of the LCAS device (break before make option).
- LCAS-EN=0:  
The ring relay can be controlled automatically by the SLIC-LCP relay driver pin RD.

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**IOCTL2 (Allocation C)**
**I/O Control Register 2**
**(06<sub>H</sub>)**
**Reset Value: 0094<sub>H</sub>**


Field	Bits	Type	Description
<b>DUP-OVT</b>	[15:13]	rw	<b>Data Upstream Persistence Counter End Value</b> Restricts the rate of interrupts generated by the OTEMP bit in the status register for Analog-Line-Module Interrupts 2 (SRS2). The interval is programmable from 1 ms to 57 ms in steps of 8 ms. DUP-OVT      Interval [ms] 000            1 (default) 001            9 010            17 011            25 100            33 101            41 110            49 111            57
<b>DD-IO4</b>	12	rw	<b>Output Value IO4</b> Value for the programmable I/O pin IO4 if programmed as an output pin. 0      Pin IO4 is driving a logic 0. 1      Pin IO4 is driving a logic 1.
<b>DD-IO3</b>	11	rw	<b>Output Value IO3</b> Value for the programmable I/O pin IO3 if programmed as an output pin. 0      Pin IO3 is driving a logic 0. 1      Pin IO3 is driving a logic 1.

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Field	Bits	Type	Description																																																			
DD-IO2	10	rw	<b>Output Value IO2</b> Value for the programmable I/O pin IO2 if programmed as an output pin. 0 Pin IO2 is driving a logic 0. 1 Pin IO2 is driving a logic 1.																																																			
DD-IO1	9	rw	<b>Output Value IO1</b> Value for the programmable I/O pin IO1 if programmed as an output pin. If external ringing is selected (bit REXT-EN in register RTR set to 1), pin IO1 cannot be controlled by the user but is utilized by the VINETIC®-x to control the ring relay. 0 Pin IO1 is driving a logic 0. (Ring pause) 1 Pin IO1 is driving a logic 1. (Ring burst)																																																			
DD-IO0	8	rw	<b>Output Value IO0</b> Value for the programmable I/O pin IO0 if programmed as an output pin. 0 Pin IO0 is driving a logic 0. 1 Pin IO0 is driving a logic 1.																																																			
DUP	[7:4]	rw	<b>Data Upstream Persistence Counter End Value</b> Restricts the rate of interrupts generated by the HOOK bit in the status register SRS1. The interval is programmable.  <table><tr><th>DUP</th><th>HOOK Act [ms]</th><th>HOOK PD [ms]</th></tr><tr><td>0000</td><td>1</td><td>2</td></tr><tr><td>0001</td><td>2</td><td>4</td></tr><tr><td>0010</td><td>3</td><td>6</td></tr><tr><td>0011</td><td>4</td><td>8</td></tr><tr><td>0100</td><td>5</td><td>10</td></tr><tr><td>0101</td><td>6</td><td>12</td></tr><tr><td>0110</td><td>7</td><td>14</td></tr><tr><td>0111</td><td>8</td><td>16</td></tr><tr><td>1000</td><td>9</td><td>18</td></tr><tr><td>1001</td><td>10 (default)</td><td>20</td></tr><tr><td>1010</td><td>11</td><td>22</td></tr><tr><td>1011</td><td>12</td><td>24</td></tr><tr><td>1100</td><td>13</td><td>26</td></tr><tr><td>1101</td><td>14</td><td>28</td></tr><tr><td>1110</td><td>15</td><td>30</td></tr><tr><td>1111</td><td>16</td><td>32</td></tr></table>	DUP	HOOK Act [ms]	HOOK PD [ms]	0000	1	2	0001	2	4	0010	3	6	0011	4	8	0100	5	10	0101	6	12	0110	7	14	0111	8	16	1000	9	18	1001	10 (default)	20	1010	11	22	1011	12	24	1100	13	26	1101	14	28	1110	15	30	1111	16	32
DUP	HOOK Act [ms]	HOOK PD [ms]																																																				
0000	1	2																																																				
0001	2	4																																																				
0010	3	6																																																				
0011	4	8																																																				
0100	5	10																																																				
0101	6	12																																																				
0110	7	14																																																				
0111	8	16																																																				
1000	9	18																																																				
1001	10 (default)	20																																																				
1010	11	22																																																				
1011	12	24																																																				
1100	13	26																																																				
1101	14	28																																																				
1110	15	30																																																				
1111	16	32																																																				

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Field	Bits	Type	Description
<b>DUP-IO</b>	[3:0]	rw	<b>Data Upstream Persistence Counter End Value</b> Valid for the I/O pins when used as digital input pins and the bits ICON and VTRLIM in register SRS2. The interval is programmable: <div> DUP-IO      Interval [ms] <div> 0000      0.5 0001      4.5 0010      8.5 0011      12.5 0100      16.5 (default) 0101      20.5 0110      24.5 0111      28.5 1000      32.5 1001      36.5 1010      40.5 1011      44.5 1100      48.5 1101      52.5 1110      56.5 1111      60.5 </div> </div>



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**BCR1 (Allocation C)**
**Basic Configuration Register 1**
**(07<sub>H</sub>)**
**Reset Value: 2000<sub>H</sub>**

15	14	13	12	11	10	9	8
DUP-GNDK				LMAC64	PRAM-DCC	HIM-RES	HIM-AN
rw							
7	6	5	4	3	2	1	0
LMABS-EN	DC-HOLD	EN-IK	TEST-EN	SEL-SLIC			
rw							

Field	Bits	Type	Description
DUP-GNDK	[15:12]	rw	<b>Data Upstream Persistence Counter Groundkey End Value</b>
			Restricts the rate of interrupts generated by the GNDK bit in the status register SRS1.The interval is programmable.
			DUP-GNDK      GNDK      GNDK
			[ms] $f_{\min,ACsup}[\text{Hz}]^{1)}$
			0000            4            125.0000
			0001            8            62.5000
			0010            12 (default)    41.6667
			0011            16            31.2500
			0100            20            25.0000
			0101            24            20.8333
			0110            28            17.8571
			0111            32            15.6250
			1000            36            13.8889
			1001            40            12.5000
			1010            44            11.3636
			1011            48            10.4167
			1100            52            9.6154
			1101            56            8.9286
			1110            60            8.3333
1111            64            7.8125			

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Field	Bits	Type	Description
<b>LMAC64</b>	11	rw	<b>Auxiliary gain in the AC levelmeter</b> Enables gain of 64 before squarer (or rectifier) in the AC levelmeter 0 No auxiliary gain (gain = 1) 1 auxiliary gain enabled, with gain factor of 64
<b>PRAM-DCC</b>	10	rw	<b>Configuration Bit for DCCTL</b> 0 Run program from PROM 1 Run program from PRAM
<b>HIM-RES</b>	9	rw	<b>High Impedance Reserved</b> Reserved for future use.
<b>HIM-AN</b>	8	rw	<b>High Impedance in the Analog Impedance Matching Loop</b> The value of this bit must correspond to the selection done in the VINETICOS tool when calculating the coefficients. The total impedance of the VINETIC®-x is synthesized as a combination of three different loops (one analog and two digital loops). 0 Standard (low) impedance in analog impedance matching loop. 1 High impedance in analog impedance matching loop.
<b>LMABS-EN</b>	7	rw	<b>Rectifier or Squarer Selection for the AC Levelmeter</b> Enables rectifier or squarer for AC levelmeter 0 Squarer enabled (rectifier disabled) 1 Rectifier enabled (squarer disabled) <i>Note: This selection will only have effect for the AC Levelmeter if the bit LM-RECT is set to "1".</i>
<b>DC-HOLD</b>	6	rw	<b>DC Hold</b> Actual DC output value hold. The value after the summation point of the last DSP filter stage of the DC regulation and the PCM2DC input will be frozen (see <a href="#">Figure 27</a> ). 0 Normal operation 1 DC output value hold

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Field	Bits	Type	Description
<b>EN-IK</b>	5	rw	<p><b>Enable Enhanced DC Regulation</b></p> <p>The enhanced DC regulation provides a constant off-hook current independent from the loop resistance.</p> <p>0      Enhanced regulation disabled</p> <p>1      Enhanced regulation enabled</p> <p><i>Note: For detailed description of the Enhanced DC Regulation see Preliminary User's Manual - System Reference.</i></p>
<b>TEST-EN</b>	4	rw	<p><b>Test Enable</b></p> <p>Activates the VINETIC®-x test features controlled by test register TSTR1, TSTR2 and TSTR3.</p> <p>0      VINETIC®-x test features are disabled.</p> <p>1      VINETIC®-x test features are enabled.</p> <p>The test register bits can be programmed before the TEST-EN bit is set to 1.</p> <p><i>Note: The switching of the TEST-EN bit may change the absolute AC level in transmit and receive, depending on the current value of the TTX-EN bit in register BCR2. The effects on the level are summed in <a href="#">Table 20 on Page 118</a></i></p>

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Field	Bits	Type	Description
<b>SEL-SLIC</b>	[3:0]	rw	<p><b>SLIC Type Selection without Download of Micro Program Extension to Analog Line Module (DCCTL)</b></p> <p>Dependent on the SLIC types used, the appropriate predefined mode table has to be selected. The following devices are supported without a download of a micro program extension to the Analog Line Module (DCCTL).</p> <p>0000 SLIC-S/SLIC-S2 selected.</p> <p>0001 SLIC-E/SLIC-E2 Version 1.1 or SLIC-E/SLIC-E2 Version 1.2 with C3 open or connected to GND or TSLIC-E Version 1.1/Version 1.2 selected.</p> <p>0010 SLIC-P selected.</p> <p>0011 SLIC-P selected for extremely power sensitive applications using external ringing. In this case the C3 pin of the SLIC-P can be connected to GND.</p> <p>0100 SLIC-E/SLIC-E2 Version 1.2 with C3 connected to VDD or TSLIC-E0 Version 1.2 selected.</p> <p>0101 GEMINAX S/S2</p> <p>0110 SLIC-P with current limitation (60 mA) selected.</p> <p>0111 –1111 Reserved for future use.</p>

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Field	Bits	Type	Description
<b>SEL-SLIC</b>	[3:0]	rw	<b>SLIC Type Selection with download of micro program extension to Analog Line Module (DCCTL)</b> The following devices are supported with a download of a micro program extension to the Analog Line Module (DCCTL). 0000 SLIC-S/SLIC-S2 selected. 0001 SLIC-E/SLIC-E2 Version 1.1 or SLIC-E/SLIC-E2 Version 1.2 with C3 open or connected to GND or TSLIC-E Version 1.1/Version 1.2 selected. 0010 reserved. 0011 reserved. 0100 SLIC-E/SLIC-E2 Version 1.2 with C3 connected to VDD or TSLIC-E0 Version 1.2 selected. 0101 GEMINAX S/S2 0110–0111 reserved 1000 SLIC-LCP selected 1001 SLIC-LCP with current limitation selected 1010 GEMINAX-S MAX selected 1011 GEMINAX-S MAX with current limitation selected 1010 –1111 Reserved for future use.

<sup>1)</sup> Minimum frequency for AC suppression.

**For SLIC-P Two Selections are Possible**

- The standard SLIC-P selection automatically uses the IO0 pin of the VINETIC®-x to control the C3 pin of the SLIC-P. By using pin C3 as well as the pins C1 and C2, all possible operating modes of the SLIC-P can be selected.
- For extremely power sensitive applications using external ringing with SLIC-P SEL-SLIC[3:0] = 0011 should be chosen. In this case, internal unbalanced ringing is not needed and therefore there is no need to switch the C3 pin of the SLIC-P to 'High'. The C3 pin of the SLIC-P must be connected to GND and the IO0 pin of the VINETIC®-x is programmable by the user.

There is no need for a high battery voltage for ringing either. This mode uses  $V_{BATR}$  for the on-hook voltage (e.g. –48 V) in Power Down Resistive (PDR) mode and the other battery supply voltages (e.g.  $V_{BATH} = -24$  V and  $V_{BATL} = -18$  V) can be used for the off-hook state. This will help to save power because the lowest possible battery voltage can be selected.

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The flags TTX-EN (see [Page 113](#)), AC-XGAIN (see [Page 141](#)) and AC-RGAIN (see [Page 141](#)) should be considered as static. After setting TEST-EN to 1, the relative receive and transmit level may deviate from the programmed level. [Table 20](#) shows the dependencies.

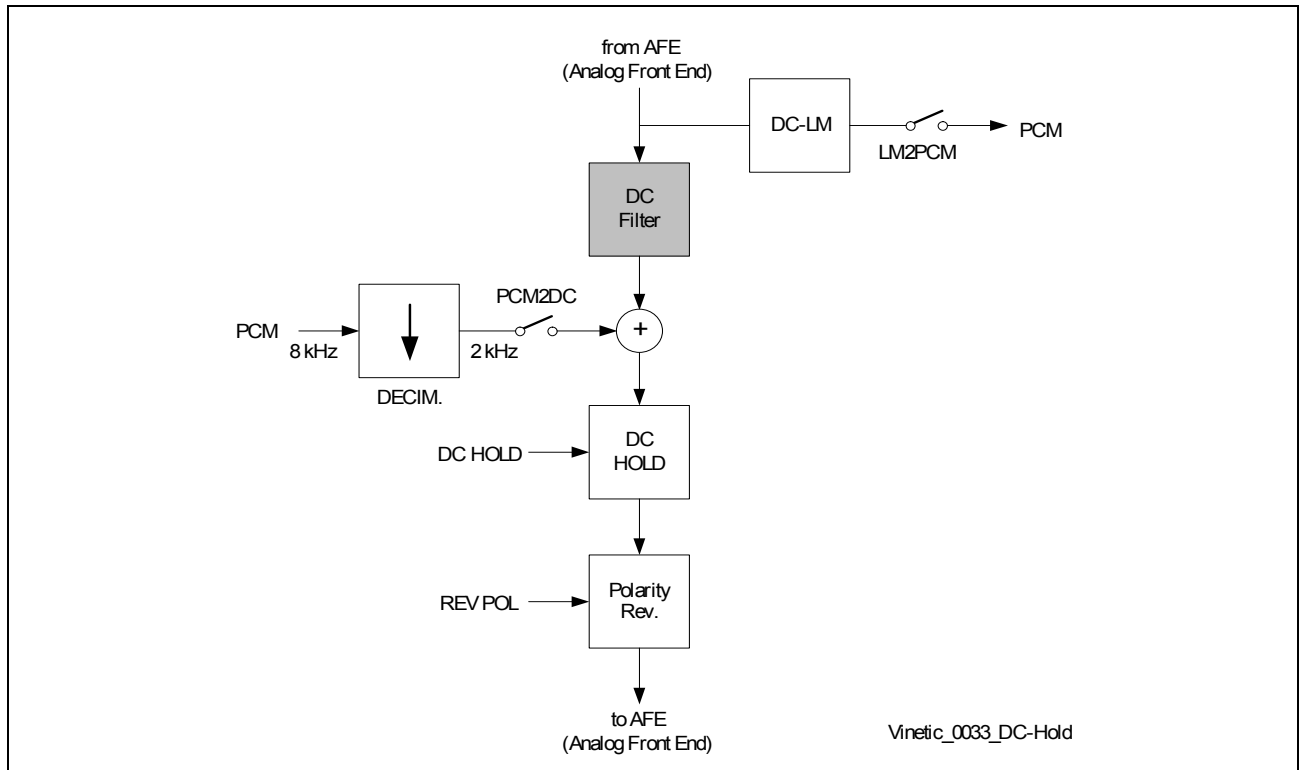
**Table 20 Level Changes Depending on TTX-EN, AC-XGAIN and AC-RGAIN**

TTX-EN	AC-XGAIN	AC-RGAIN	Deviation Transmit [dB]	Deviation Receive [dB]	Remark
0	0	0	-6.85	+6.85	
1	0	0	0	0	
0	1	1	0	0	Default
1	1	1	+6.85	-6.85	
0	0	1	-6.85	0	1)
1	0	1	0	-6.85	1)
0	1	0	0	+6.85	1)
1	1	0	+6.85	0	1)

1) Test condition in receive: high ohmic load between tip and ring.

Test condition in transmit: the input signal is applied directly between the pins ITx and VCMITx, after disconnecting the SLIC. Alternatively, the test circuit in Figure 32 of the data sheet can be used.

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**Figure 27 DC Hold**

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**BCR2 (Allocation C)**
**Basic Configuration Register 2**
**(08<sub>H</sub>)**
**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
LPRX-CR	CRAM-EN	SOFT-DIS	TTX-EN	TTX-12K	REV-POL	AC-SHORT-EN	0
rw							
7	6	5	4	3	2	1	0
TH-DIS	IM-DIS	AX-DIS	AR-DIS	FRX-DIS	FRR-DIS	HPX-DIS	HPR-DIS
rw							

Field	Bits	Type	Description
LPRX-CR	15	rw	<b>LPR/LPX Filter CRAM Coefficients</b> Selects CRAM coefficients for the filter characteristic of the LPR/LPX filters. These coefficients may be enabled in case of a modem transmission to improve the modem performance. 0 Coefficients from ROM are used. 1 Coefficients from CRAM are used.
CRAM-EN	14	rw	<b>CRAM Enable</b> Enables all coefficients in CRAM except those controlled by LPRX-CR and PTG. 0 Coefficients from ROM are used. 1 Coefficients from CRAM are used. <i>Note: LPRX-CR of register BCR2 and PTG of register DSCR are independent of the value of CRAM-EN.</i>
SOFT-DIS	13	rw	<b>Soft Polarity Reversal/ Soft TTX Burst switching Disable</b> Disables soft switching for polarity reversal or soft TTX bursts switching (to minimize noise on DC feeding). 0 soft polarity reversal / soft TTX burst switching. 1 hard polarity reversal / hard TTX burst switching.



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Field	Bits	Type	Description
<b>TTX-EN</b>	12	rw	<p><b>TTX Enable</b>            Configuration of the metering signal either by burst or reversed polarity.</p> <p>0 TTX bursts are disabled. Any “active with metering” mode will generate the metering signal with polarity reversal.</p> <p>1 TTX bursts are enabled. Any “active with metering” mode will generate the metering signal with TTX bursts (12/16 kHz).</p> <p><i>Note: The activation and deactivation of metering with either TTX or reverse polarity is performed by a operating mode change from active mode to active with metering mode or vice versa (see <a href="#">Table 6 on Page 57</a> ).</i></p> <p><i>Metering pulses (TTX bursts or polarity reversal) may also be generated by the auto-metering function.</i></p> <p><i>Frequency (12/16 kHz) and amplitude of the TTX bursts are set via CRAM coefficients.</i></p>
<b>TTX-12K</b>	11	rw	<p><b>TTX 12 kHz</b>            Selection of TTX frequency.</p> <p>0 16 kHz TTX signals selected.</p> <p>1 12 kHz TTX signals selected.</p>
<b>REV-POL</b>	10	rw	<p><b>Reverse Polarity</b>            Reverses the polarity of DC feeding.</p> <p>0 Normal polarity.</p> <p>1 Reverse polarity.</p> <p><i>Note: This bit will be combined with the operating mode “active with metering” by an exclusive-or function in case TTX-EN = 0</i></p>
<b>AC-SHORT-EN</b>	9	rw	<p><b>AC Short Enable</b>            Enables temporarily lower input impedance at input pin ITAC.</p> <p>During soft reversal the input pin ITAC will temporarily be set to a lower input impedance for faster discharging the external capacitor.</p> <p>0 Input impedance of the ITAC pin is standard (high impedance).</p> <p>1 Input impedance of the ITAC pin is lowered.</p>

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Field	Bits	Type	Description
<b>TH-DIS</b>	7	rw	<b>TH Filter Disable</b> Disables the transhybrid filter 0 TH filter is enabled. 1 TH filter is disabled ( $H_{TH} = 0$ ).
<b>IM-DIS</b>	6	rw	<b>IM Filter Disable</b> Disables the impedance-matching filter in the codec DSP. 0 IM filter is enabled. 1 IM filter is disabled ( $H_{IM} = 0$ ).
<b>AX-DIS</b>	5	rw	<b>AX Filter Disable</b> Disables the attenuation filter in transmit direction (AX) in the codec DSP. 0 AX filter is enabled. 1 AX filter is disabled ( $H_{AX} = 1$ ).
<b>AR-DIS</b>	4	rw	<b>AR Filter Disable</b> Disables the attenuation filter in receive direction in the codec DSP. 0 AR filter is enabled. 1 AR filter is disabled ( $H_{AR} = 1$ ).
<b>FRX-DIS</b>	3	rw	<b>FRX Filter Disable</b> Disables the frequency-response filter in transmit direction (FRX) in the codec DSP. 0 FRX filter is enabled. The coefficients of the CRAM will be used. 1 Default coefficients will be used <i>Note: This bit will be ignored if CRAM-EN = 0. In this case the default coefficients will be used</i>
<b>FRR-DIS</b>	2	rw	<b>FRR Filter Disable</b> Disables the frequency-response filter in receive direction (FRR) in the codec DSP 0 FRR filter is enabled. 1 FRR filter is disabled ( $H_{FRR} = 1$ ).
<b>HPX-DIS</b>	1	rw	<b>HPX Filter Disable</b> Disables the high-pass filter in transmit direction. 0 High-pass filter is enabled. 1 High-pass filter is disabled ( $H_{HPX} = 1$ ).

Field	Bits	Type	Description
<b>HPR-DIS</b>	0	rw	<b>HPR Filter Disable</b> Disables the high-pass filter in receive direction. 0      High-pass filter is enabled. 1      High-pass filter is disabled ( $H_{\text{HPR}} = 1$ ).



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**DSCR (Allocation C)**
**DTMF Sender Configuration Register (09<sub>H</sub>)**
**Reset Value: 0000<sub>H</sub>**

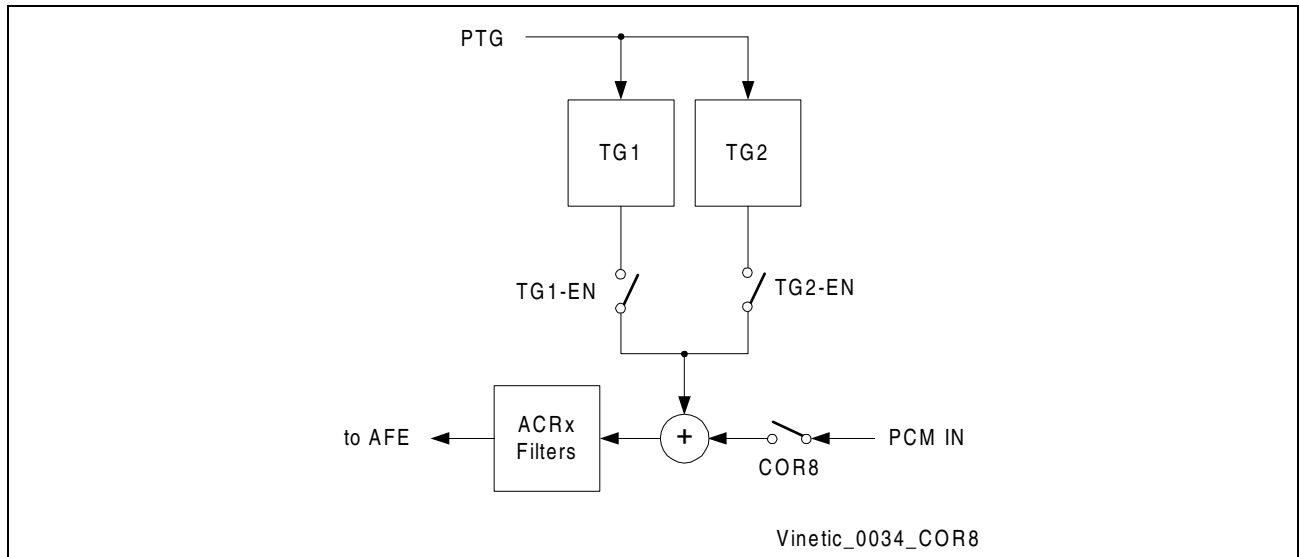
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
rw							
7	6	5	4	3	2	1	0
DG-KEY				COR8	PTG	TG2-EN	TG1-EN
rw							

Field	Bits	Type	Description																																																																				
DG-KEY	[7:4]	rw	<b>DTMF Key Selection</b> Selects one of sixteen DTMF keys. The tones are generated by the two tone generators. The key will be generated if TG1-EN and TG2-EN are 1. <i>Note: These two DTMF generators are additional tone generators and work independently of the tone generators of the EDSP.</i>																																																																				
			<table> <tr> <th>DG-KEY</th><th>DIGIT</th><th><math>f_{LOW}</math> [Hz]</th><th><math>f_{HIGH}</math> [Hz]</th></tr> <tr><td>0000</td><td>0</td><td>941</td><td>1336</td></tr> <tr><td>0001</td><td>1</td><td>697</td><td>1209</td></tr> <tr><td>0010</td><td>2</td><td>697</td><td>1336</td></tr> <tr><td>0011</td><td>3</td><td>697</td><td>1477</td></tr> <tr><td>0100</td><td>4</td><td>770</td><td>1209</td></tr> <tr><td>0101</td><td>5</td><td>770</td><td>1336</td></tr> <tr><td>0110</td><td>6</td><td>770</td><td>1477</td></tr> <tr><td>0111</td><td>7</td><td>852</td><td>1209</td></tr> <tr><td>1000</td><td>8</td><td>852</td><td>1336</td></tr> <tr><td>1001</td><td>9</td><td>852</td><td>1477</td></tr> <tr><td>1010</td><td>*</td><td>941</td><td>1209</td></tr> <tr><td>1011</td><td>#</td><td>941</td><td>1477</td></tr> <tr><td>1100</td><td>A</td><td>697</td><td>1633</td></tr> <tr><td>1101</td><td>B</td><td>770</td><td>1633</td></tr> <tr><td>1110</td><td>C</td><td>852</td><td>1633</td></tr> <tr><td>1111</td><td>D</td><td>941</td><td>1633</td></tr> </table>	DG-KEY	DIGIT	$f_{LOW}$ [Hz]	$f_{HIGH}$ [Hz]	0000	0	941	1336	0001	1	697	1209	0010	2	697	1336	0011	3	697	1477	0100	4	770	1209	0101	5	770	1336	0110	6	770	1477	0111	7	852	1209	1000	8	852	1336	1001	9	852	1477	1010	*	941	1209	1011	#	941	1477	1100	A	697	1633	1101	B	770	1633	1110	C	852	1633	1111	D	941	1633
DG-KEY	DIGIT	$f_{LOW}$ [Hz]	$f_{HIGH}$ [Hz]																																																																				
0000	0	941	1336																																																																				
0001	1	697	1209																																																																				
0010	2	697	1336																																																																				
0011	3	697	1477																																																																				
0100	4	770	1209																																																																				
0101	5	770	1336																																																																				
0110	6	770	1477																																																																				
0111	7	852	1209																																																																				
1000	8	852	1336																																																																				
1001	9	852	1477																																																																				
1010	*	941	1209																																																																				
1011	#	941	1477																																																																				
1100	A	697	1633																																																																				
1101	B	770	1633																																																																				
1110	C	852	1633																																																																				
1111	D	941	1633																																																																				

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Field	Bits	Type	Description
<b>COR8</b>	3	rw	<b>Cut Off Receive 8 kHz</b> Cuts off the receive path at 8 kHz before the tone generator summation point (see <a href="#">Figure 29</a> ). Allows sending of tone generator signals with no overlaid voice. 0      Cut off receive path disabled. 1      Cut off receive path enabled.
<b>PTG</b>	2	rw	<b>Programmable Tone Generator Coefficients</b> Programmable coefficients for tone generators will be used. 0      Standard DG-Key Frequencies 1      CRAM coefficients. In this case the frequencies of both TG1 and TG2 are programmable, and the appropriate CRAM coefficients can be calculated with the VINETICOS. <i>Note: For VINETIC®-x Version 1.4 devices in order to achieve a faultless function of the PTG bit, a DCCTL download is required.</i>
<b>TG2-EN</b>	1	rw	<b>Tone Generator 2 Enable</b> Enables tone generator two. 0      Tone generator is disabled. 1      Tone generator is enabled.
<b>TG1-EN</b>	0	rw	<b>Tone Generator 1 Enable</b> Enables tone generator one. 0      Tone generator is disabled. 1      Tone generator is enabled.

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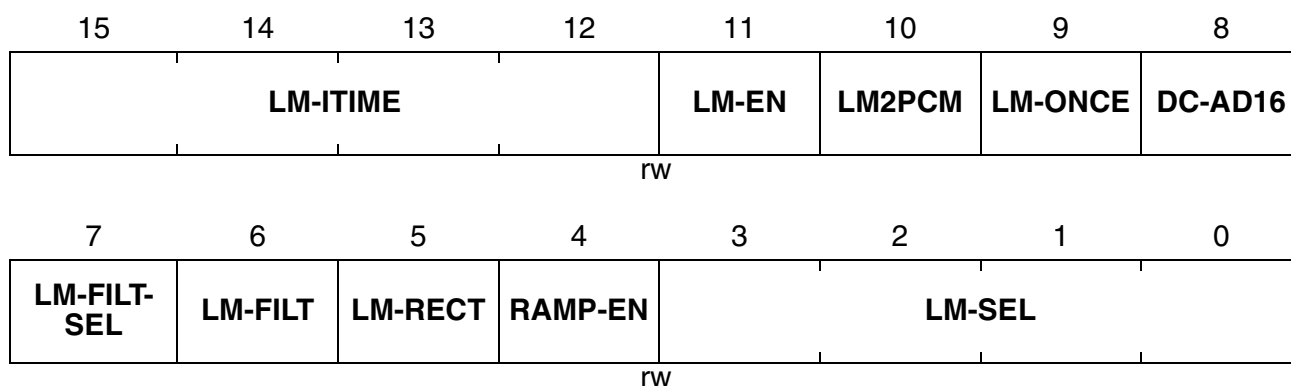
**Figure 29 Cut Off Receive 8 kHz**

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# LMCR (Allocation C)

## Level Metering Configuration Register(0A<sub>H</sub>)

Reset Value: 0200<sub>H</sub>



Field	Bits	Type	Description
LM-ITIME	[15:12]	rw	<b>Level Metering Integration Time</b> Integration time for AC Level Metering.  <i>Note: For the DC level metering, the integration time is given by the period of the programmed ring frequency, even if no ring signal is applied to the line.</i>
			LM-ITIME            Value [ms]
			0000                16
			0001                32
			0010                48
			0011                64
			0100                80
			0101                96
			0110                112
			0111                128
			1000                144
			1001                160
			1010                176
			1011                192
			1100                208
			1101                224
			1110                240
			1111                256

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Field	Bits	Type	Description
<b>LM-EN</b>	11	rw	<b>Level Metering Enable</b> Enables level metering with integration of the source signal. A positive transition of this bit starts a measurement accordingly to the mode defined with the LM-ONCE bit. 0 The source is not integrated and can be monitored by the LM register or the PCM interface. 1 Level metering with integrator.
<b>LM2PCM</b>	10	rw	<b>Level Meter to PCM</b> Level metering source/result feeding is transferred to the PCM interface (see <a href="#">Figure 27</a> ). (depending on LM-EN bit) 0 Normal Operation. 1 Level metering source /result is fed to PCM interface.
<b>LM-ONCE</b>	9	rw	<b>Level Meter Once</b> Selects level metering execution mode. 0 Level metering is executed continuously. 1 Level metering is executed only once. <i>Note: To start the level meter again, the LM-EN bit must be set back to 0 and then to 1.</i>
<b>DC-AD16</b>	8	rw	<b>DC AD Path 16</b> Additional digital amplification in the DC AD path for level metering. 0 Additional gain factor 16 disabled. 1 Additional gain factor 16 enabled.
<b>LM-FILT-SEL</b>	7	rw	<b>Level Metering Filter Selection</b> Selects a notch filter or a band-pass filter for the AC level metering. 0 Notch filter selected. 1 Band-pass filter selected.
<b>LM-FILT</b>	6	rw	<b>Level Metering Filter</b> Enables a programmable band-pass or notch filter for the AC level metering. 0 Normal operation (no filtering). 1 Band-pass/notch filter enabled.
<b>LM-RECT</b>	5	rw	<b>Level Metering Rectifier</b> Enables rectifier in DC level meter. 0 Rectifier disabled. 1 Rectifier enabled.



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Field	Bits	Type	Description
<b>RAMP-EN</b>	4	rw	<b>Ramp Enable</b> Enables ramp generator. The ramp generator works together with the RING-OFFSET bits in RTR and the LM-EN bit to create different voltage slopes in the DC-Path. 0 Ramp generator disabled. 1 Ramp generator enabled.
<b>LM-SEL</b>	[3:0]	rw	<b>Level Metering Select</b> Selection of the source for the level metering. 0000 AC level metering in transmit 0001 Real part of TTX (TTX <sub>REAL</sub> ) 0010 Imaginary part of TTX (TTX <sub>IMG</sub> ) 0011 Voltage on IO3 – IO2 0100 DC out voltage on DCN-DCP 0101 DC current on IT (DC level metering) 0110 AC level metering in receive 0111 AC level metering in receive and transmit 1000 Voltage on IO4 – IO2 1001 DC current on IL 1100 Voltage on IO3 1011 Voltage on IO4 1010 Voltage on IO2 1101 $V_{DD}$ 1110 Offset of DC-Prefi (short circuit on DC-Prefi input) 1111 Voltage on IO4 – IO3

**Note:**

1. *Timing Requirements: To ensure the correct function with level metering, consecutive SOP commands for the ALM modules must be sent by the host with time gaps of  $\geq 2$  ms.*
2. *For VINETIC®-x V1.4 devices a DCCTL download is required in order achieve faultless working of the level metering function.*

**CONFIDENTIAL**
**RTR (Allocation C)**
**Ring Configuration Register**
**(0B<sub>H</sub>)**
**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	LCAS-EN

rw

7	6	5	4	3	2	1	0
RTR-EXTS	RTR-SEL	RTR-FAST	PCM2DC	RING-OFFSET		ASYNC H-R	REXT-EN

rw

Field	Bits	Type	Description
LCAS-EN	8	rw	<b>LCAS Enable</b> Enables control of Line Access Switch when using SLIC-LCP 0 Control of an external ring relay by IO1x. IO1x is switched to 1 during Ringing mode. 1 Control of an LCAS device by IO0x and IO1x. IO1 is switched to 1 during ring burst. With a mode change from Ringing mode to another mode IO0 is switched to 0 for about 30 ms. <i>Note: This bit is only available after download of a specific DCCTL micro program extension.</i>
RTR-EXTS	7	rw	<b>External Ringburst Sense</b> Select source for ring trip detection. 0 ITx pin is used as source for ring current sensing. 1 Depending on the SLIC used the IO pin defined in <a href="#">Table 18 on Page 108</a> will be used for ring current sensing during a ringburst (typically IO2) In all other operating modes the ITx pin will be used. The switching between ITx and IO2x (and the ring trip threshold) is synchronized with the switching of the ring relays.

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Field	Bits	Type	Description
<b>RTR-SEL</b>	6	rw	<b>Ring Trip Select</b> Standard Ring Trip method selection with integration over one ringing period 0 Ring Trip with a DC offset is selected. 1 AC Ring Trip is selected. Recommended for short lines only. During Ring Burst RO2 is active in all other modes the ring offset set in the RTR register (RING-OFFSET) is activated. The setting of the ring offset is handled automatically and synchronously with the ring signal.
<b>RTR-FAST</b>	5	rw	<b>Ring Trip Fast</b> Selection of the detection method. 0 Standard Ring Trip method (see RTR-SEL) selected 1 Fast Ring Trip method selected. Fast detection of off-hook indication (without integration over one ringing period). The HOOK bit in the SRS1 register will be set as soon as a programmable current threshold is exceeded. Always asynchronous mode switching independent of ASYNCH-R bit  <i>Note: With the fast ring trip detection method the channel is switched automatically to Active High independent of the ringing mode selected.</i>
<b>PCM2DC</b>	4	rw	<b>PCM to DC</b> PCM voice channel data added to the DC-output. This function can be used to transfer a ring signal or an offset from the PCM voice channel to the line through a summation point in the DC characteristic (test feature). After the summation point the DC-HOLD and polarity reversal functions have been implemented (s. <a href="#">Figure 27</a> ). 0 Normal operation. 1 PCM voice channel data is added to DC output.
<b>RING-OFFSET</b>	[3:2]	rw	<b>Ring Offset Selection</b> Selection of the Ring Offset source as depicted in <a href="#">Table 21</a> .

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Field	Bits	Type	Description
<b>ASYNCH-R</b>	1	rw	<b>Asynchronous External Ringing</b> Enables asynchronous mode switching for internal or external ringing. 0 Mode switching, synchronous with zero crossing. 1 Asynchronous mode switching.
<b>REXT-EN</b>	0	rw	<b>External Ring Enable</b> Enables the use of an external ring signal generator. Synchronization is done via the RSYNC pin and the Ring Burst Enable signal is transferred via the IO1 pin. 0 External ringing is disabled. 1 External ringing enabled.

**Table 21 Interpretation of Ring Offset Bits**

<b>RNG-OFFSET</b>	<b>Ring Offset Voltage in Given Mode</b>		
	<b>Active ACTH/ACTL</b>	<b>Active Ring ACTR</b>	<b>Ring Pause Ringing</b>
0 0	Voltage given by DC regulation	Voltage given by DC regulation	Ring Offset RO1 Hook Threshold Ring
0 1	Ring Offset RO1/2 (no DC regulation)	Ring Offset RO1 (no DC regulation)	Ring Offset RO1 Hook Threshold Ring
1 0	Ring Offset RO2/2 (no DC regulation)	Ring Offset RO2 (no DC regulation)	Ring Offset RO2 Hook Message Waiting
1 1	Ring Offset RO3/2 (no DC regulation)	Ring Offset RO3 (no DC regulation)	Ring Offset RO3 Hook Message Waiting

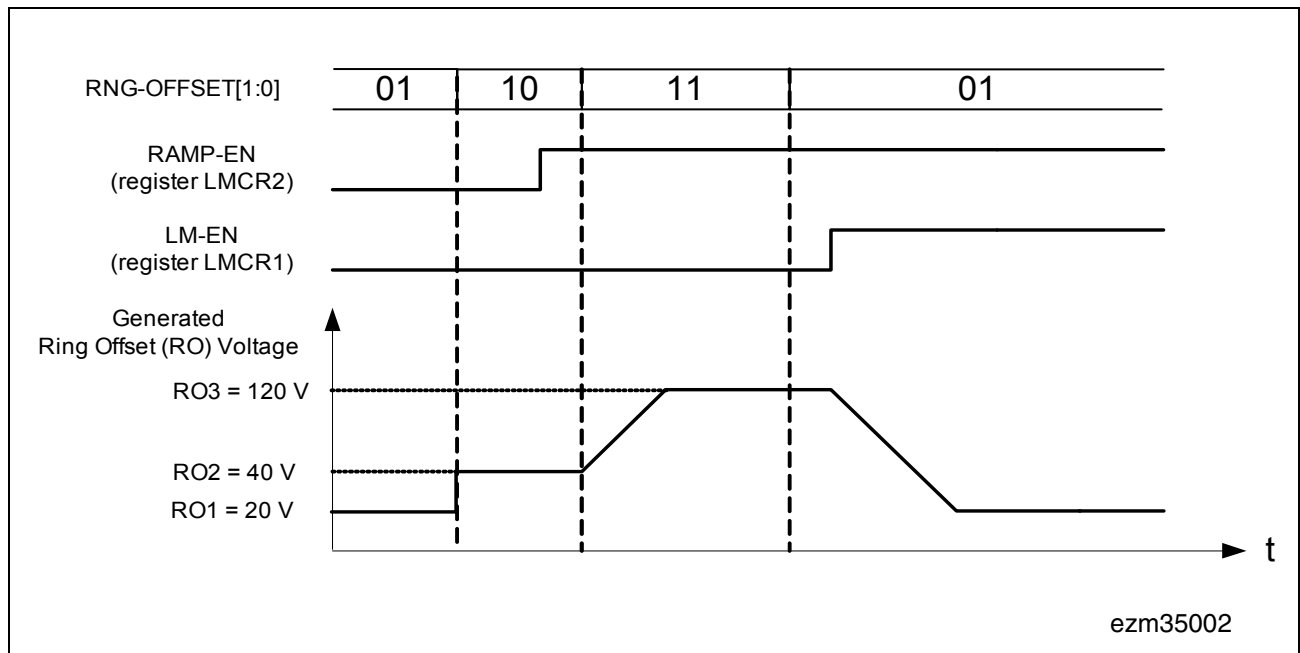
By setting the RAMP-EN bit (register LMCR) to 1, the ramp generator is started by setting LM-EN (register LMCR) from 0 to 1 (see [Figure 30](#)).

Exception: Transition of RNG-OFFSET from 10 to 11 or 11 to 10 where the ramp generator is started automatically.

For Ring Offset RO1, the usual “Hook Threshold Ring” is used. Using Ring Offset RO2 or RO3 in any ringing mode (Ringing and Ring Pause) also changes the hook thresholds. In this case the “Hook Message Waiting” threshold is used automatically.

When using the Ring Offsets RO2 and RO3 for Message Waiting, an additional lamp current is expected. In this case, the Hook Message Waiting threshold should be programmed higher than the Hook Threshold Ring.

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**Figure 30 Example for Switching Between Different Ring Offset Voltages**

The three programmable Ring Offsets are typically used for the following purposes:

**Table 22 Typical Usage for the three Ring Offsets**

Ring Offset Voltage	Application
Ring Offset RO1	Ringing
Ring Offset RO2	Low voltage for message waiting lamp
Ring Offset RO3	High voltage for message waiting lamp

Besides the typical usage described in [Table 22](#), the Ring Offsets RO1, RO2, and RO3 can also be used for the generation of different custom waveforms (see [Figure 30](#)).

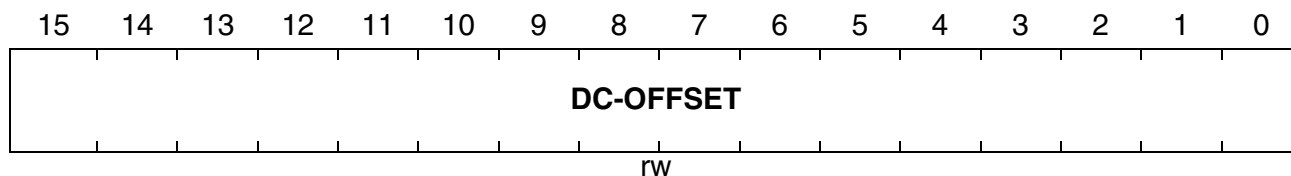
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**OFR (Allocation C)**

**DC Offset Register**

**(0C<sub>H</sub>)**

**Reset Value: 0000<sub>H</sub>**



Field	Bits	Type	Description
<b>DC-OFFSET</b>	[15:0]	rw	<b>DC Offset</b> The value of this register is added to the input of the DC loop to compensate for a given offset of the current sensors in the SLIC-E/-E2/-P. For computation of the DC-offset please refer to chapter "Current Offset Compensation" in the <i>Preliminary User's Manual - System Reference</i> <i>Note: For additional information on offset compensation an Application Note is available.</i>

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**AUTOMOD (Allocation C)**
**Automatic Mode Register**
**(0D<sub>H</sub>)**
**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0

rw

7	6	5	4	3	2	1	0
0	0	AUTO-RING-EN	AUTO-MET-START	AUTO-MET-EN	AUTO-OFFH	AUTO-BAT	PDOT-DIS

rw

Field	Bits	Type	Description
<b>AUTO-RING-EN</b>	5	rw	<b>Auto Ring Function Enable</b> 0 Auto Ring Function disable 1 Auto Ring Function enable
<b>AUTO-MET-START</b>	4	rw	<b>Auto Metering Start</b> 0 Don't care This bit will be reset to 0 by the VINETIC®-x 1 Start Auto Metering <i>Note: With the transition from 0 → 1 the auto metering is started. This bit will be reset to 0 right after the start of the auto metering pulse. While the auto metering function is active a change of the AUTO-MET-START bit, initiated from the host, will be ignored by the VINETIC®-x.</i>
<b>AUTO-MET-EN</b>	3	rw	<b>Auto Metering Enable</b> 0 Auto Metering disable 1 Auto Metering enable

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Field	Bits	Type	Description
<b>AUTO-OFFH</b>	2	rw	<p><b>Automatic Off-Hook Detection</b></p> <p>0     automatic off-hook detection disabled</p> <p>1     automatic off-hook detection enabled</p> <p>If AUTO-OFFH=1 VINETIC®-x will perform the following transitions:</p> <ul style="list-style-type: none"> <li>• In case an off-hook is detected VINETIC®-x will automatically switch from the current mode to Active Mode as listed below: PDRH, PDRR → Active High Ringing (Active High) → Active High Ringing (Active Boost) → Active High Ring Pause (Active High) → Active High Ring Pause (Active Boost) → Active High If off-hook can not be verified (off-hook indication was too short) the chip set will be set back to the mode programmed by the host. This is likely the ring burst or the ring pause mode. An off-hook detection during ringing will switch off the ring generator.</li> <li>• In case an on-hook is detected: VINETIC®-x will automatically switch to the mode programmed by the host. (Active → host mode)</li> </ul>
<b>AUTO-BAT</b>	1	rw	<p><b>Automatic Mode Battery Switching</b></p> <p>Automatic battery mode switching for power management. Change from <math>V_{BATH} \rightarrow V_{BATL}</math>.</p> <p>0     Automatic mode not activated</p> <p>1     Automatic mode activated</p> <p><i>Note: Checking for <math>V_{BATH}/V_{BATL}</math> is only executed once after a off-hook is detected.</i></p> <p><i>In a later state, even when the programmed threshold is exceeded, no transition <math>V_{BATH} \rightarrow V_{BATL}</math> is conducted.</i></p> <p><i>The voltage threshold for the Tip Ring voltage is set in CRAM (calculated with VINETICOS DC Control Parameter 2/4: Tip-Ring Voltage Threshold).</i></p>



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Field	Bits	Type	Description
<b>PDOT-DIS</b>	0	rw	<p><b>Power Down Overtemperature Disable</b> Disables power down mode in case of overtemperature. <i>Note: If overtemperature is detected the VINETIC®-x indicates this by setting the OTEMP bit in the SRS2 register.</i></p>
			<p>0 When overtemperature is detected, the SLIC is automatically switched into Power Down High Impedance mode (PDH). This is the safe operation mode for the SLIC in case of overtemperature. To leave the automatically activated PDH mode, the VINETIC®-x must be switched to PDH mode and then to the mode as desired by the host.</p> <p>1 When overtemperature is detected, the SLIC is not automatically switched into Power Down High Impedance mode. But in any case, the output current of the SLIC buffers is limited to a value that keeps the SLIC temperature below the upper temperature limit.</p>

**CONFIDENTIAL**
**TSTR1 (Allocation C)**
**Test Register 1**
**(0E<sub>H</sub>)**
**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
<b>PD-AC-PR</b>	<b>PD-AC-PO</b>	<b>PD-AC-AD</b>	<b>PD-AC-DA</b>	<b>PD-DC-PR</b>	<b>PD-DC-AD</b>	<b>PD-DC-DA</b>	<b>PD-DCBUF</b>
rw							
7	6	5	4	3	2	1	0
<b>PD-ACDITH</b>	<b>PD-DCREF</b>	<b>PD-GNKC</b>	<b>PD-OFHC</b>	<b>PD-OVTC</b>	<b>PD-ACREF</b>	<b>PD-IREF</b>	<b>PD-HVI</b>
rw							

This register has no effect unless the TEST-EN bit in register BCR1 is set to 1.

Field	Bits	Type	Description
<b>PD-AC-PR</b>	15	rw	<b>AC-PREFI Power Down</b> (don't use, reserved!) 0 Normal operation 1 Power Down mode
<b>PD-AC-PO</b>	14	rw	<b>AC-POFI Power Down</b> (don't use, reserved!) 0 Normal operation 1 Power Down mode
<b>PD-AC-AD</b>	13	rw	<b>AC-ADC Power Down</b> (don't use, reserved!) 0 Normal operation 1 Power Down mode, transmit path is inactive.
<b>PD-AC-DA</b>	12	rw	<b>AC-DAC Power Down</b> (don't use, reserved!) 0 Normal operation 1 Power Down mode, receive path is inactive.
<b>PD-DC-PR</b>	11	rw	<b>DC-PREFI Power Down</b> (don't use, reserved!) 0 Normal operation 1 Power Down mode

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Field	Bits	Type	Description
<b>PD-DC-AD</b>	10	rw	<b>DC-ADC Power Down</b> (don't use, reserved!) 0 Normal operation 1 Power Down mode, transmit path is inactive.
<b>PD-DC-DA</b>	9	rw	<b>DC-DAC Power Down</b> (don't use, reserved!) 0 Normal operation 1 Power Down mode, receive path is inactive.
<b>PD-DCBUF</b>	8	rw	<b>DC-BUFFER Power Down</b> (don't use, reserved!) 0 Normal operation 1 Power Down mode
<b>PD-ACDITH</b>	7	rw	<b>AC ADC Dither Power Down</b> (don't use, reserved!) 0 Normal operation 1 Power Down mode
<b>PD-DCREF</b>	6	rw	<b>DC Loop Reference Power Down</b> (don't use, reserved!) 0 Normal operation 1 Power Down mode
<b>PD-GNKC</b>	5	rw	<b>Ground Key Comparator (GNKC) Power Down</b> (don't use, reserved!) 0 Normal operation 1 Power Down mode
<b>PD-OFHC</b>	4	rw	<b>Off-Hook Comparator (OFHC) Power Down</b> (don't use, reserved!) 0 Normal operation 1 Power Down mode
<b>PD-OVTC</b>	3	rw	<b>Overtemperature Comparator (OVTC) Power Down</b> (don't use, reserved!) 0 Normal operation 1 Power Down mode
<b>PD-ACREF</b>	2	rw	<b>AC Loop Reference Power Down</b> (don't use, reserved!) 0 Normal operation 1 Power Down mode

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Field	Bits	Type	Description
<b>PD-IREF</b>	1	rw	<b>Channel Bias Current Block Power Down</b> (don't use, reserved!) 0      Normal operation 1      Power Down mode
<b>PD-HVI</b>	0	rw	<b>HV Interface Power Down</b> (don't use, reserved!) (to SLIC) 0      Normal operation 1      Power Down mode

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**TSTR2 (Allocation C)**
**Test Register 2**
**(0F<sub>H</sub>)**
**Reset Value: 00C0<sub>H</sub>**

15	14	13	12	11	10	9	8
0	AC-ALB-PP	AC-ALB-16M	AC-DLB-16M	AC-DLB-128K	AC-DLB-32K	AC-DLB-8K	AC-SHORT
rw							
7	6	5	4	3	2	1	0
AC-RGAIN	AC-XGAIN	LOW-PERF		OPIM-AN	OPIM-HW	COR-64	COX-16
rw							

This register has no effect unless the TEST-EN bit in register BCR1 is set to 1.

Field	Bits	Type	Description
<b>AC-ALB-PP</b>	14	rw	<b>AC Analog Loop-Back Prefi Pofi</b> AC analog loop-back via prefi-pofi filters. <i>Note: Also the bit PD-AC-DA in register TSTR1 has to be set. Otherwise the output of the AC DAC will be low-impedance.</i> 0 Normal operation 1 Analog loop-back for the AC path via prefi-pofi filters.
<b>AC-ALB-16M</b>	13	rw	<b>AC Analog Loop 16 MHz</b> AC analog loop via a 16 MHz bitstream. 0 Normal operation 1 The output of the ADC is interpolated and looped back to the input of the DAC.
<b>AC-DLB-16M</b>	12	rw	<b>AC Digital Loop 16 MHz</b> AC digital loop back. The data from the PCM interface are looped back before the DAC. 0 Normal operation 1 Digital loop closed

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Field	Bits	Type	Description
<b>AC-DLB-128K</b>	11	rw	<b>AC Digital Loop-Back 128 kHz</b> The signal from the PCM interface is digitally looped back. This full digital loop is closed in the ALM-DSP's 128 kHz domain. 0     Normal operation 1     Digital loop closed
<b>AC-DLB-32K</b>	10	rw	<b>AC Digital Loop-Back 32 kHz</b> The signal from the PCM interface is digitally looped back. This full digital loop is closed in the ALM-DSP's 32 kHz domain. 0     Normal operation 1     Digital loop closed
<b>AC-DLB-8K</b>	9	rw	<b>AC Digital Loop-Back 8 kHz</b> The signal from the PCM interface is digitally looped back. This full digital loop is closed in the ALM-DSP's 8 kHz. 0     Normal operation 1     Digital loop closed
<b>AC-SHORT</b>	8	rw	<b>AC Short</b> The input pin ITAC will be set to a lower input impedance. 0     Input impedance of the ITAC pin is standard. 1     Input impedance of the ITAC pin is lowered.
<b>AC-RGAIN</b>	7	rw	<b>AC Receive Gain</b> Analog gain in receive direction. 0     No additional analog gain in receive direction. 1     Additional 6.85 dB analog attenuation in receive direction.
<b>AC-XGAIN</b>	6	rw	<b>AC Transmit Gain</b> Analog gain in transmit direction. 0     No additional analog gain in transmit direction. 1     Additional 6.85 dB analog amplification in transmit direction.

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Field	Bits	Type	Description
<b>LOW-PERF</b>	[5:4]	rw	<b>Low Performance Mode</b> (don't use, reserved!) Reduction of the analog clock of the HW-filters. This leads to a lower power consumption (for lifeline support). In this low performance modes the VINETIC®-x will not fulfill the specifications any more. 00 Normal mode 01 8 MHz mode (low performance) 10 4 MHz mode (low performance) 11 reserved
<b>OPIM-AN</b>	3	rw	<b>Open Impedance Loop through Analog Part</b> Open impedance matching loop through the analog part. 0 Normal operation 1 Loop opened
<b>OPIM-HW</b>	2	rw	<b>Open Impedance Loop through Hardware Filters</b> Open digital impedance matching loop through the hardware filters. 0 Normal operation 1 Loop opened
<b>COR-64</b>	1	rw	<b>Cut Off Receive 64 kHz</b> Cut off the AC receive path at 64 kHz. 0 Normal operation 1 Receive path is cut off (open).
<b>COX-16</b>	0	rw	<b>Cut Off Transmit 16 kHz</b> Cut off the AC transmit path at 16 kHz. (The TH filters can be tested without the influence of the analog part.) 0 Normal operation 1 Transmit path is cut off.

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**TSTR3 (Allocation C)**
**Test Register 3**
**(10<sub>H</sub>)**
**Reset Value: 0000**

15	14	13	12	11	10	9	8
<b>DC-ALB-PP</b>	<b>DC-ALB-1M</b>	<b>DC-DLB-1M</b>	<b>DC-POFI-HI</b>	<b>0</b>	<b>DCC-DIS</b>	<b>DC-LP2-DIS</b>	<b>DC-LP1-DIS</b>
rw							
7	6	5	4	3	2	1	0
<b>ATST-RES5</b>	<b>ATST-RES4</b>	<b>ATST-RES3</b>	<b>ATST-RES2</b>	<b>ATST-RES1</b>	<b>ATST-RES0</b>	<b>NO-DITH-AC</b>	<b>NO-AUTO-DITH-AC</b>
rw							

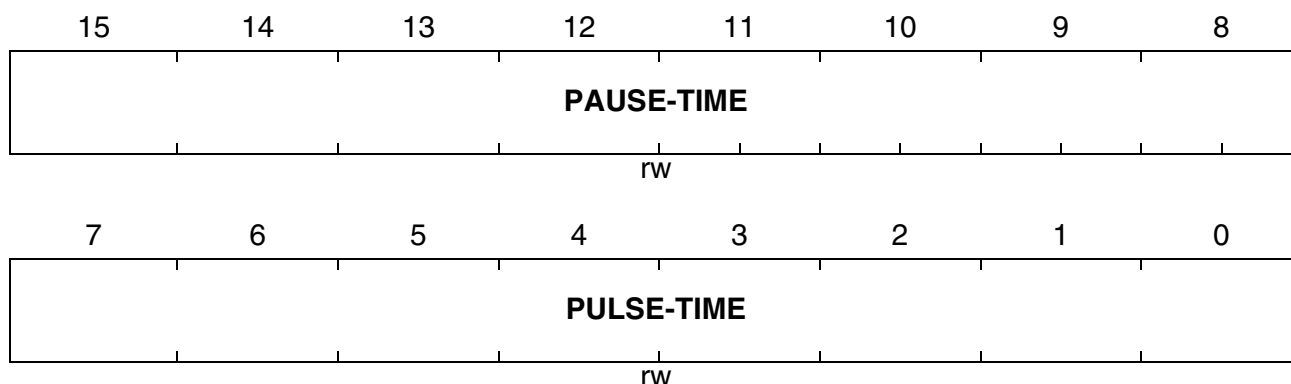
This register has no effect unless the TEST-EN bit in register BCR1 is set to 1.

Field	Bits	Type	Description
<b>DC-ALB-PP</b>	15	rw	<b>DC Analog Loop-Back Prefi Pofi</b> (don't use, reserved!) DC analog loop-back via prefi-pofi filters. 0 Normal operation 1 Analog loop-back for the DC path via prefi-pofi filters selected.
<b>DC-ALB-1M</b>	14	rw	<b>DC Analog Loop 1 MHz</b> (don't use, reserved!) DC analog loop via a 1-MHz bitstream 0 Normal operation 1 The output of the 1 MHz DC ADC is interpolated and connected to the input of the 4 MHz DC DAC for testing purposes.
<b>DC-DLB-1M</b>	13	rw	<b>DC Digital Loop 1 MHz</b> (don't use, reserved!) DC digital loop via a 1-MHz bitstream. 0 Normal operation 1 The input of the DC DAC is decimated and looped back to the output of the DC ADC.
<b>DC-POFI-HI</b>	12	rw	<b>DC Pofi High Value</b> Higher value for the DC post filter cut-off frequency. 0 Cut-off frequency is set to 100 Hz (normal operation). 1 Cut-off frequency is set to 300 Hz.



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Field	Bits	Type	Description
<b>DCC-DIS</b>	10	rw	<b>DC Characteristic Disable</b> Disables DC characteristic 0 Normal operation 1 DC characteristic is disabled
<b>DC-LP2-DIS</b>	9	rw	<b>DC Low Pass 2 Disable</b> (don't use, reserved!) Disables low pass 2 (LP2) of DC characteristic 0 Normal operation 1 LP2 of the DC characteristic is disabled (bypassed)
<b>DC-LP1-DIS</b>	8	rw	<b>DC Low Pass 1 Disable</b> (don't use, reserved!) Disables low pass 1 (LP1) of DC characteristic 0 Normal operation 1 LP1 of the DC characteristic is disabled (bypassed)
<b>ATST-RES5</b>	7	rw	<b>Analog Test Reserved 5</b> reserved for future use
<b>ATST-RES4</b>	6	rw	<b>Analog Test Reserved 4</b> reserved for future use
<b>ATST-RES3</b>	5	rw	<b>Analog Test Reserved 3</b> reserved for future use
<b>ATST-RES2</b>	4	rw	<b>Analog Test Reserved 2</b> reserved for future use
<b>ATST-RES1</b>	3	rw	<b>Analog Test Reserved 1</b> reserved for future use
<b>ATST-RES0</b>	2	rw	<b>Analog Test Reserved 0</b> reserved for future use
<b>NO-DITH-AC</b>	1	rw	<b>No AC Dithering</b> (don't use, reserved!) Disables dithering of the AC ADC 0 Normal operation 1 Dithering of the AC ADC is disabled
<b>NO-AUTO-DITH-AC</b>	0	rw	<b>No Auto AC Dithering</b> (don't use, reserved!) Disables automatic dithering of the AC ADC 0 Normal operation: Automatic dithering enabled 1 Automatic dithering disabled

**CONFIDENTIAL**
**AUTOMETCONF (Allocation C)**
**Auto Metering**
**Configuration Register**
**(1A<sub>H</sub>)**
**Reset Value: xxxx<sub>H</sub>**


Field	Bits	Type	Description
<b>PAUSE-TIME</b>	[15:8]	rw	<b>Auto Metering Pause Time</b> Duration of metering pause for auto metering (AUTO-MET-EN = 1).
			00 <sub>H</sub> 0.5 ms metering pause duration
			01 <sub>H</sub> 4.5 ms metering pause duration
			·
			·            0.5 + n*4 ms metering pause duration for n = 0..255
			·
			FF <sub>H</sub> 1020.5 ms metering pause duration
<b>PULSE-TIME</b>	[7:0]	rw	<b>Auto Metering Pulse Time</b> Metering pulse time for auto metering (AUTO-MET-EN = 1).
			00 <sub>H</sub> 8 ms metering pulse duration
			01 <sub>H</sub> 16 ms metering pulse duration
			·
			·            8 + n*8 ms metering pulse duration for n = 0..255
			·
			FF <sub>H</sub> 2048 ms metering pulse duration

*Note: In order that VINETIC®-x will support this register a download of a DCCTL micro program extension is necessary.*

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### Auto Metering

Auto Metering generates one metering pulse and indicates the completion of this pulse by an interrupt to the host. **Figure 31** and **Figure 32** show a timing diagram of metering pulses, generated by the auto metering function, with the corresponding control and status bits. The function is implemented in the Analog-Line-Module of VINETIC®-x, thus the control from the host is done by SOP commands. Status monitoring is achieved via the first status registers of the Analog-Line-Module **SRS1 (Allocation C)**.

The following registers are relevant for programming the auto metering function:

- **“AUTOMOD (Allocation C)” on Page 135** with  
**AUTO-MET-EN** (Enable/Disable auto metering)  
**AUTO-MET-START** (Start auto metering)
- **“AUTOMETCONF (Allocation C)” on Page 146**  
**PAUSE-TIME** (Pause time for auto metering)  
**PULSE-TIME** (Pulse time for auto metering)
- **“SRS1 (Allocation C)” on Page 214**  
**AUTO-MET-DONE** (Auto metering done status bit, indication via Interrupt)
- **“I-SRS1 (Allocation C)” on Page 233**  
**AUTO-MET-DONE** (Auto metering done interrupt status)
- **“MR-SRS1 (Allocation C)” on Page 165 & “MF-SRS1 (Allocation C)” on Page 177**  
**M-AUTO-MET-DONE** (Interrupt mask bits for auto metering done)
- **“BCR2 (Allocation C)” on Page 120**  
**TTX-EN** (TTX Enable)

The Auto Metering Function works with both metering methods, metering by TTX bursts and metering by polarity reversal.

When **AUTO-MET-EN** is set to 1, the auto metering function is enabled and the standard metering modes (Active High with Metering, Active Low with Metering) are deactivated.

When **AUTO-MET-START** is set to 1 and the VINETIC®-x is in Active mode (High or Low) one metering pulse is started with the duration set in the **PULSE-TIME** field. The metering pulse is succeeded by a metering pause phase. The duration of this pause is defined in the **PAUSE-TIME** field. With the introduction of **PAUSE-TIME** it is possible to generate an interrupt at the estimated end of the TTX slope, as VINETIC®-x does not provide status information of the actual end of the TTX slope.

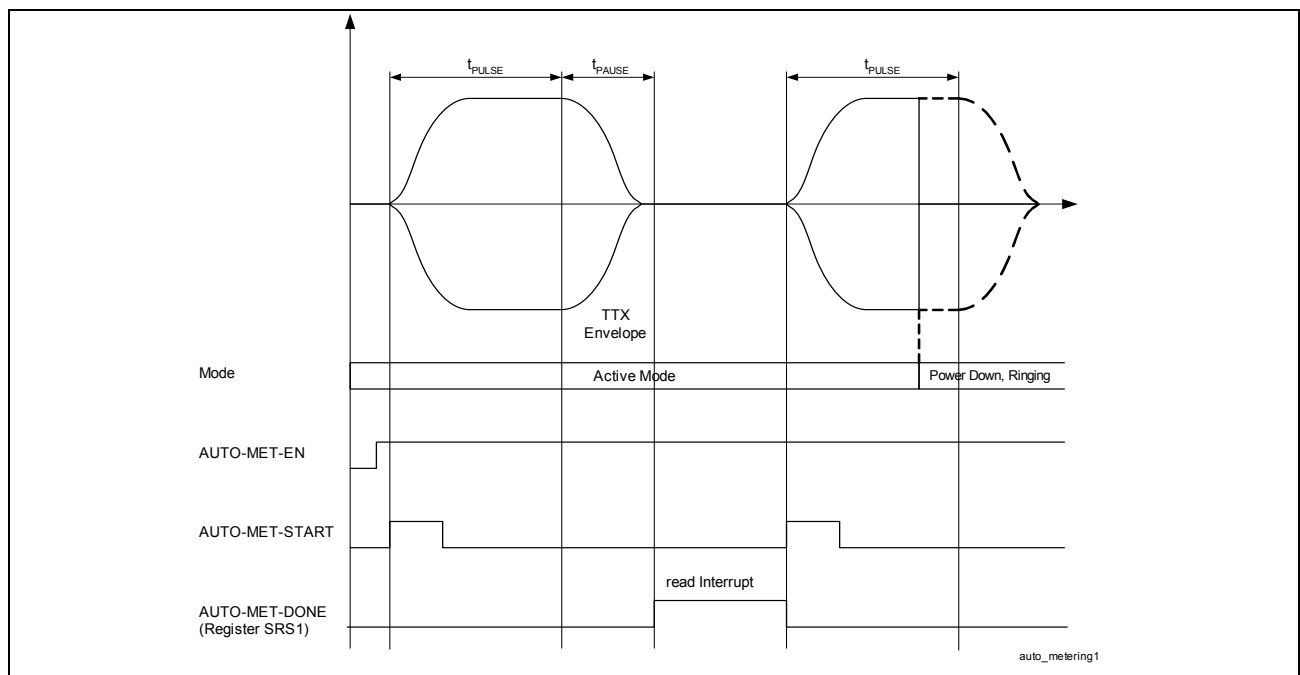
The end of the pause phase is indicated by the interrupt status bit **AUTO-MET-DONE**. After this bit is set a new metering pulse can be triggered by the host.

- The metering pulse generated by the auto metering function will be stopped with:
- A mode change of VINETIC®-x to another mode as Active mode. In this case the metering pulse is immediately cut off as shown in **Figure 31**.
- Setting of the **AUTO-MET-EN** bit to 0 by the host during the pulse- or pause-phase. In this case a soft cut of the metering pulse takes place as shown in **Figure 32**

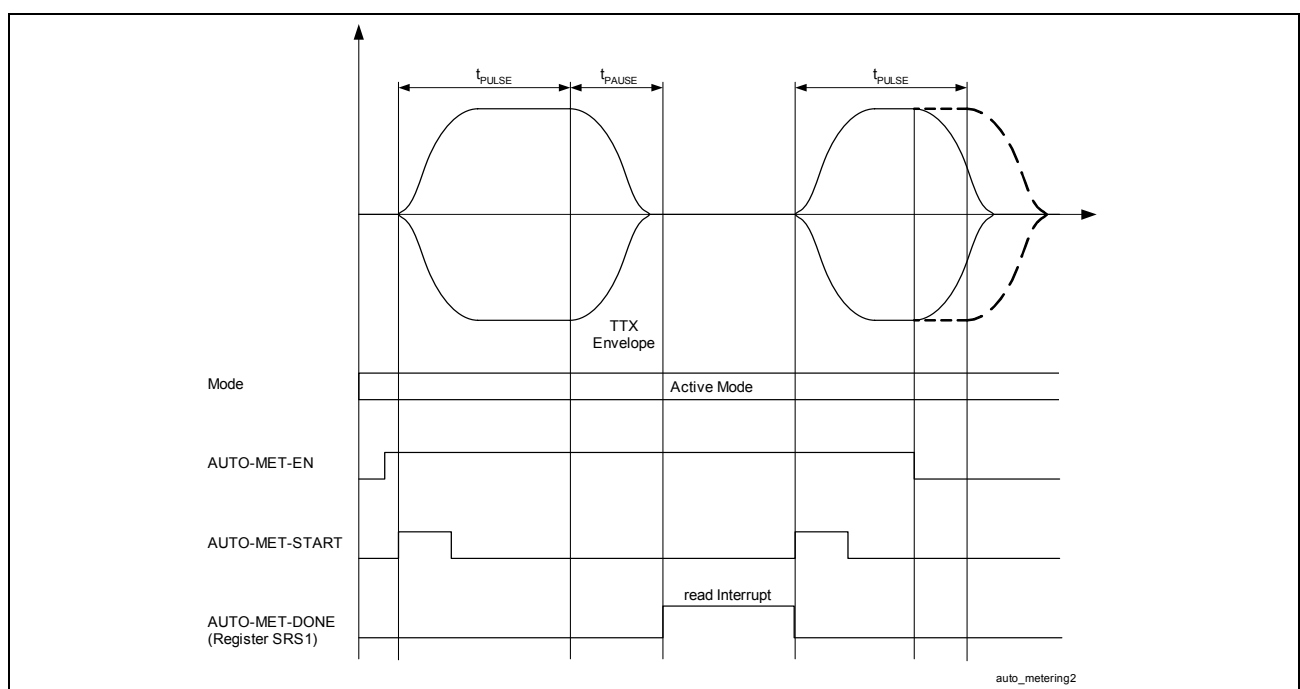
**CONFIDENTIAL**

*Note: Auto Metering is only available after a download of a micro program extension to the DCCTL!*

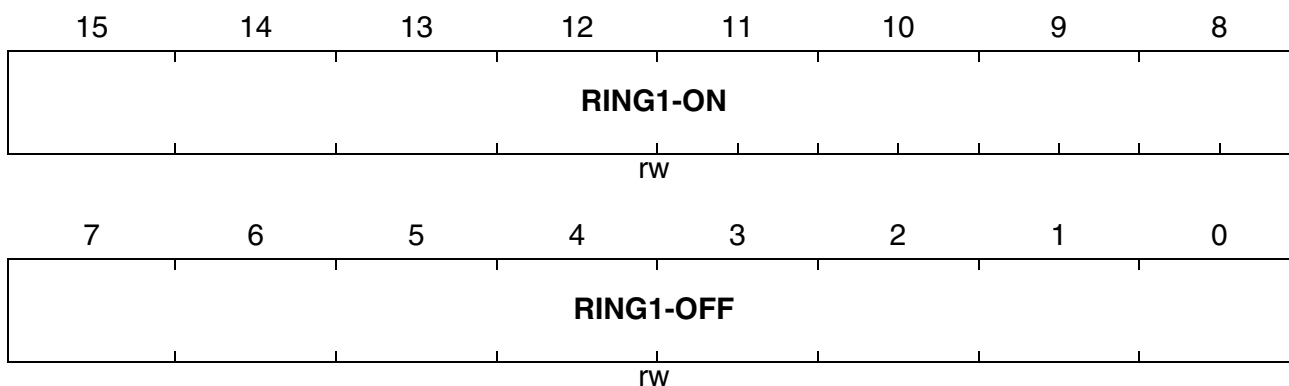
*The auto metering function will generate the 12/16kHz metering pulses only if the TTX-EN bit of register BCR2 is set to 1. For a detailed description of the TTX-EN bit see Preliminary User's Manual - Software Description.*



**Figure 31 Auto Metering Function - Termination by a Mode Change**



**Figure 32 Auto Metering Function - Termination by AUTO-MET-EN Bit**

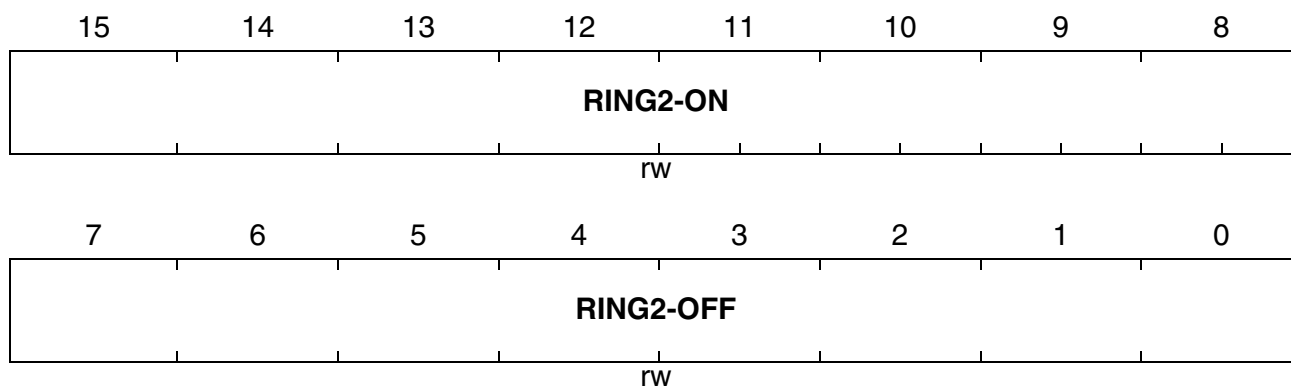
**CONFIDENTIAL**
**AUTORINGCONF1 (Allocation C)**
**Auto Ring Cadence 1**
**Configuration Register**
**(1B<sub>H</sub>)**
**Reset Value: xxxx<sub>H</sub>**


Field	Bits	Type	Description
<b>RING1-ON</b>	[15:8]	rw	<b>Auto Ring Cadence 1 On Time</b> Ring On Time for the 1 <sup>st</sup> ring cadence when Auto Ring Function is enabled. (AUTO-RING-EN = 1). 01 <sub>H</sub> 1/f <sub>R</sub> [Hz] ... RING1-ON time [s] 02 <sub>H</sub> 2/f <sub>R</sub> [Hz] ... RING1-ON time [s] . FF <sub>H</sub> 255/f <sub>R</sub> [Hz] ... RING1-ON time [s]
<b>RING1-OFF</b>	[7:0]	rw	<b>Auto Ring Cadence 1 Off Time</b> Ring Off Time for the 1 <sup>st</sup> ring cadence when Auto Ring Function is enabled (AUTO-RING-EN = 1). 01 <sub>H</sub> 1/f <sub>R</sub> [Hz] ... RING1-OFF time [s] 02 <sub>H</sub> 2/f <sub>R</sub> [Hz] ... RING1-OFF time [s] . FF <sub>H</sub> 255/f <sub>R</sub> [Hz] ... RING1-OFF time [s]

f<sub>R</sub>[Hz] corresponds to the VINETIC®-x ring frequency according to the used coefficient setting from CRAM or ROM.

*Note:*

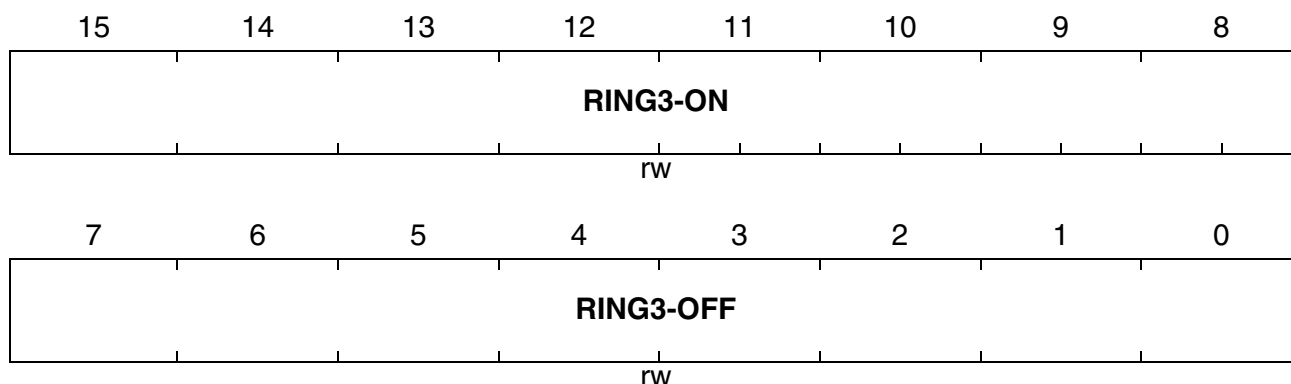
1. Before using the auto ring function valid values for RING1-ON/RING1-OFF.. RING4-ON/RING4-OFF and R1ON2CID have to be set by the host, as no appropriate reset values are provided. The time intervals are defined by multiple of the ring signal period (1/f<sub>R</sub>).
2. With VINETIC®-x Version 1.4 devices the Auto Ring Function is only available after a download of a micro program extension to the DCCTL!

**CONFIDENTIAL**
**AUTORINGCONF2 (Allocation C)**
**Auto Ring Cadence 2**
**Configuration Register**
**(1C<sub>H</sub>)**
**Reset Value: xxxx<sub>H</sub>**


Field	Bits	Type	Description
<b>RING2-ON</b>	[15:8]	rw	<b>Auto Ring Cadence 2 On Time</b> Ring On Time for the 2 <sup>nd</sup> ring cadence when Auto Ring Function is enabled (AUTO-RING-EN = 1). 01 <sub>H</sub> 1/f <sub>R</sub> [Hz] ... RING2-ON time [s] 02 <sub>H</sub> 2/f <sub>R</sub> [Hz] ... RING2-ON time [s] . FF <sub>H</sub> 255/f <sub>R</sub> [Hz] ... RING2-ON time [s]
<b>RING2-OFF</b>	[7:0]	rw	<b>Auto Ring Cadence 2 Off Time</b> Ring Off Time for the 2 <sup>nd</sup> ring cadence when Auto Ring Function is enabled (AUTO-RING-EN = 1). 01 <sub>H</sub> 1/f <sub>R</sub> [Hz] ... RING2-OFF time [s] 02 <sub>H</sub> 2/f <sub>R</sub> [Hz] ... RING2-OFF time [s] . FF <sub>H</sub> 255/f <sub>R</sub> [Hz] ... RING2-OFF time [s]

f<sub>R</sub>[Hz] ... VINETIC®-x Ring frequency according to the used coefficient setting from CRAM or ROM.

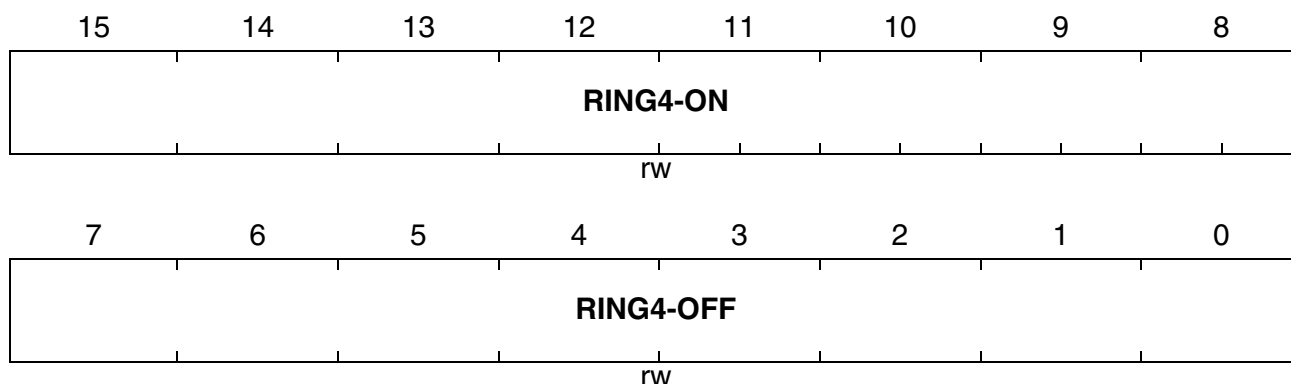
*Note: Before using the auto ring function valid values for RING1-ON/RING1-OFF.. RING4-ON/RING4-OFF and R1ON2CID have to be set by the host, as no appropriate reset values are provided. The time intervals are defined by multiple of the ring signal period (1/f<sub>R</sub>).*

**CONFIDENTIAL**
**AUTORINGCONF3 (Allocation C)**
**Auto Ring Cadence 3**
**Configuration Register**
**(1D<sub>H</sub>)**
**Reset Value: xxxx<sub>H</sub>**


Field	Bits	Type	Description
<b>RING3-ON</b>	[15:8]	rw	<b>Auto Ring Cadence 3 On Time</b> Ring On Time for the 3 <sup>rd</sup> ring cadence when Auto Ring Function is enabled (AUTO-RING-EN = 1). 01 <sub>H</sub> 1/f <sub>R</sub> [Hz] ... RING3-ON time [s] 02 <sub>H</sub> 2/f <sub>R</sub> [Hz] ... RING3-ON time [s] . FF <sub>H</sub> 255/f <sub>R</sub> [Hz] ... RING3-ON time [s]
<b>RING3-OFF</b>	[7:0]	rw	<b>Auto Ring Cadence 3 Off Time</b> Ring Off Time for the 3 <sup>rd</sup> ring cadence when Auto Ring Function is enabled (AUTO-RING-EN = 1). 01 <sub>H</sub> 1/f <sub>R</sub> [Hz] ... RING3-OFF time [s] 02 <sub>H</sub> 2/f <sub>R</sub> [Hz] ... RING3-OFF time [s] . FF <sub>H</sub> 255/f <sub>R</sub> [Hz] ... RING3-OFF time [s]

f<sub>R</sub>[Hz] ... VINETIC®-x Ring frequency according to the used coefficient setting from CRAM or ROM.

*Note: Before using the auto ring function valid values for RING1-ON/RING1-OFF.. RING4-ON/RING4-OFF and R1ON2CID have to be set by the host, as no appropriate reset values are provided. The time intervals are defined by multiple of the ring signal period (1/f<sub>R</sub>).*

**CONFIDENTIAL**
**AUTORINGCONF4 (Allocation C)**
**Auto Ring Cadence 4**
**Configuration Register**
**(1E<sub>H</sub>)**
**Reset Value: xxxx<sub>H</sub>**


Field	Bits	Type	Description
<b>RING4-ON</b>	[15:8]	rw	<b>Auto Ring Cadence 4 On Time</b> Ring On Time for the 4 <sup>th</sup> ring cadence when Auto Ring Function is enabled (AUTO-RING-EN = 1). 01 <sub>H</sub> 1/f <sub>R</sub> [Hz] ... RING4-ON time [s] 02 <sub>H</sub> 2/f <sub>R</sub> [Hz] ... RING4-ON time [s] . FF <sub>H</sub> 255/f <sub>R</sub> [Hz] ... RING4-ON time [s]
<b>RING4-OFF</b>	[7:0]	rw	<b>Auto Ring Cadence 4 Off Time</b> Ring Off Time for the 4 <sup>th</sup> ring cadence when Auto Ring Function is enabled (AUTO-RING-EN = 1). 01 <sub>H</sub> 1/f <sub>R</sub> [Hz] ... RING4-OFF time [s] 02 <sub>H</sub> 2/f <sub>R</sub> [Hz] ... RING4-OFF time [s] . FF <sub>H</sub> 255/f <sub>R</sub> [Hz] ... RING4-OFF time [s]

f<sub>R</sub>[Hz] ... VINETIC®-x Ring frequency according to the used coefficient setting from CRAM or ROM.

*Note: Before using the auto ring function valid values for RING1-ON/RING1-OFF.. RING4-ON/RING4-OFF and R1ON2CID have to be set by the host, as no appropriate reset values are provided. The time intervals are defined by multiple of the ring signal period (1/f<sub>R</sub>).*



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## AUTORINGCONF5 (Allocation C)

### Ring 1 On to Caller ID Time

#### Configuration Register

(1F<sub>H</sub>)

Reset Value: xxxx<sub>H</sub>

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x
rw							
7	6	5	4	3	2	1	0
R1ON2CID							
rw							

Field	Bits	Type	Description
x	[15:8]	rw	don't care (reserved)
R1ON2CID	[7:0]	rw	<b>Ring1 On to Caller ID Time</b> Time delay after start of the Auto Ring Function until automatic sending of CID. 00 <sub>H</sub> 0/f <sub>R</sub> [Hz] ... R1ON2CID time [s] 01 <sub>H</sub> 1/f <sub>R</sub> [Hz] ... R1ON2CID time [s] . FF <sub>H</sub> 255/f <sub>R</sub> [Hz] ... R1ON2CID time [s]

f<sub>R</sub>[Hz] ... VINETIC®-x Ring frequency according to the used coefficient setting from CRAM or ROM.

*Note: Before using the auto ring function valid values for RING1-ON/RING1-OFF.. RING4-ON/RING4-OFF and R1ON2CID have to be set by the host, as no appropriate reset values are provided. The time intervals are defined by multiple of the ring signal period (1/f<sub>R</sub>).*

## Auto Ring Function

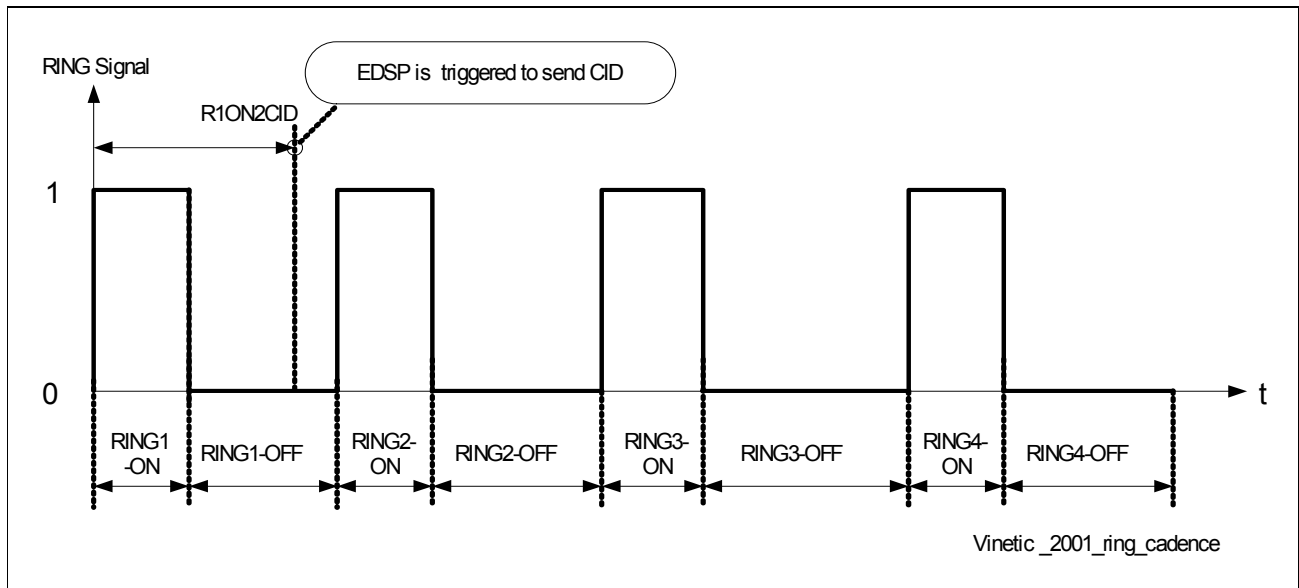
The auto ring function provides the possibility to generate a cadence of four consecutive Ring bursts as shown in **Figure 33**. The function is implemented in the Analog-Line-Module, thus the control from the host is done via SOP Commands.

Six SOP registers are relevant for the programming of the auto ring cadence.

- **AUTOMOD (Allocation C)** holding  
 AUTO-RING-EN (Enable/Disable auto ring cadence)

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- **AUTORINGCONF1 to AUTORINGCONF4 (Allocation C)** holding RINGx-ON, RINGx-OFF (On/Off Time for the four Ring ON/OFF Sequences)
- **AUTORINGCONF5 (Allocation C)** holding R1ON2CID (Duration from beginning of first ring burst to start sending of Caller ID)



**Figure 33 Auto Ring Function**

In case of auto ringing is enabled (**AUTO-RING-EN** = 1) and VINETIC®-x switches into Ringing mode, the VINETIC®-x starts automatically sending a ring cadence as shown in **Figure 33**, according to the programmed values (**RING1-ON**, **RING1-OFF** ... **RING4-ON**, **RING4-OFF**). If no termination criteria takes place (e.g. a mode change by the host because of a off-hook indication) until the completion of the 4<sup>th</sup> Ring On / Ring Off phase, the complete cadence is repeated. With the auto ring function VINETIC®-x transmits automatically a CID sequence after the delay defined in **R1ON2CID**. The timing of the delay starts with the beginning of the first Ring-On phase. In order that the CID-Sender accepts the trigger from the auto ring function, the AR bit (Auto Ring Mode On) has to be set with the EOP-Command "CID Sender".

An active auto ring function is stopped by:

- Setting **AUTO-RING-EN** bit to 0 or
- a mode change of VINETIC®-x to another mode than Ringing mode

In both cases the auto ringing will stop immediately, and a possibly ongoing CID transmission is aborted.

*Note:*

1. With VINETIC®-x Version 1.4 devices the Auto Ring Function is only available after a download of a micro program extension to the DCCTL!
2. With Version 1.4 devices RINGx-ON and RINGx-OFF must not be set to 0!

**CONFIDENTIAL****7.3 COP Command (for the Analog-Line-Module)<sup>1)</sup>**

The Analog Line Modules of the VINETIC are based on a programmable DSP, which can be controlled by coefficients. With COP commands these coefficients can be programmed to the **Coefficient RAM** (CRAM). The programming can be done individually for each channel.

Following functions can be adjusted by downloading coefficients:

- AC Impedance matching for different countries
- Relative receive and transmit level
- Tone generator (frequency, level)
- Metering (TTX and reverse polarity)
- DC (battery) feeding characteristic
- Ringing attributes (frequency, level, crest factor)
- Off-hook detection thresholds
- Ramp Generator
- Levelmeter AC filters

After reset default coefficients are taken from a coefficient ROM<sup>2)</sup>. This allows basic operation without the need of explicitly programming the coefficients. The filter structures are interdependent, and it is not recommended to change individual coefficients. If a different coefficient set is needed, it must be calculated with the coefficient calculation program VINETICOS which is supplied by Infineon. **Table 23 on Page 156** lists programming ranges and resolution of the coefficients, which can be programmed with VINETICOS.

With the COP command the coefficients set can be downloaded. The COP command syntax is described in **Chapter 4.4 on Page 63**. Depending on the values of the OFFSET-field and LENGTH-field in the command, either one single coefficient register (OFFSET = register address, LENGTH = 1) or many coefficient registers (LENGTH > 1) can be written or read.

**Table 24 on Page 157** lists the coefficients by name which can be downloaded. All Coefficient RAM locations marked with "Res." have to be set via VINETICOS. **Table 25 on Page 159** shows the register layout (address and mapping) of the CRAM.

<sup>1)</sup> With VINETIC®-x Version 1.4 ROM coefficients for the analog line channels (BCR2:CRAM-EN = 0) it is not possible to meet typical telecom standards for e.g. transhybrid loss. CRAM coefficients calculated with VINETICOS calculation core version 0.8.2.2 or newer should be used instead.

<sup>2)</sup> The default setting for the AC and DC characteristic (ROM coefficients) are listed in the *Preliminary User's Manual - System Reference*

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### Enabling of CRAM coefficients

CRAM coefficients are enabled by setting the bit CRAM-EN in register BCR2 to 1. exception are:

- Coefficients PTG1 are enabled by setting bit PTG in register DSCR to 1.
- CRAM coefficientt for the filter characteristic of the LPR/LPX filters are enabled via the LPRX-CR bit in register BCR2.
- The bit HIM-AN in BCR1 and the bit TTX-12k in BCR2 must be set with a SOP command to the value calculated by VINETICOS.

**Table 23 VINETICOS Programming Ranges**

Parameter	Range	Resolution
Constant Current $I_{K1}$	0..50 mA	0.5 mA
Power Down Current for Off-Hook	0..10 mA	0.5 mA
Off-Hook Detection in Active Mode	0..20 mA	0.5 mA
Hysteresis Off-Hook Detection in Active	0..10 mA	0.5 mA
DC Ring Trip Current Threshold	0..20 mA	0.5 mA
Current for Line Supervision (GND Start)	0..20 mA	0.5 mA
Current for Message Waiting	0..20 mA	0.5 mA
AC Ring Trip Threshold	0..70 mA	0.5 mA
Fast AC Ring Trip Threshold	0..70 mA	0.5 mA
Tip Ring Voltage Threshold	0..80 V	0.5 V
Ring Generator Frequency $f_{RING}$	2..300 Hz	1 Hz
Ring Generator Amplitude	0..85 V	0.1 V
Ring Offset RO1, RO2, RO3	0..150 V	0.1 V,
Crest Factor Ring	1.14 .. 1.73	0.01
Ring Delay	0..500 ms	1 ms
Ringing Output Impedance	0..6 k $\Omega$	10 $\Omega$
1 <sup>st</sup> DC Low Pass Corner Frequency 1	0.1..80 Hz	0.1 Hz
1 <sup>st</sup> DC Low Pass Corner Frequency 3		
1 <sup>st</sup> DC Low Pass Corner Frequency 2 <sup>1)</sup>	..160 Hz	0.1 Hz
2 <sup>nd</sup> DC Low Pass Corner Frequency 1 <sup>2)</sup>	..160 Hz	0.1 Hz
2 <sup>nd</sup> DC Low Pass Corner Frequency 2 <sup>3)</sup>	..160 Hz	0.1 Hz

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**Table 23 VINETICOS Programming Ranges (cont'd)**

Parameter	Range	Resolution
Boosted DC Gain	factor 0.8 ..3.2 (-1.94..10.1 dB)	0.01 dB
Ring Generator Low Pass Filter	2 .. 300 Hz,	1 Hz
Knee Voltage $V_{K1}$ , Open Circuit Voltage $V_{LIM}$	0..70 V	0.1V
Resistance in Resistive Zone $R_{K12}$	0..2000 $\Omega$	10 $\Omega$
Resistance in Constant Current Zone $R_I$	1.8..40 k $\Omega$	10 $\Omega$ ,
Programmable Tone Generator	-30..3 dBm0	0.1 dBm0
Programmable Tone Generator Frequency	1..3950 Hz,	1 Hz
TTX	12/16 kHz, up to 2.5 V on Tip/Ring,	0.1 V
Input Impedance Gain in Transmit and Receive Transhybrid Loss	Specification in accordance with ITU-T Recommendation G.712, ITU-T Recommendation Q.552 for interface Z and applicable LSSGR, fulfills all country specific requirements	

- 1) 1<sup>st</sup> DC Low Pass Corner Frequency 2 > 1<sup>st</sup> DC Low Pass Corner Frequency 1
- 2) 2<sup>nd</sup> DC Low Pass Corner Frequency 1 > 1<sup>st</sup> DC Low Pass Corner Frequency 2
- 3) 2<sup>nd</sup> DC Low Pass Corner Frequency 2 > 2<sup>nd</sup> DC Low Pass Corner Frequency 1

**Table 24 Coefficient Names**

Offset	Short Name	Long Name
00 <sub>H</sub>	Res.	Coefficient will be set via Coefficient RAM download
04 <sub>H</sub>	Res.	Coefficient will be set via Coefficient RAM download
08 <sub>H</sub>	AR	Amplification/Attenuation Stage Coefficients Receive
0C <sub>H</sub>	AX	Amplification/Attenuation Stage Coefficients Transmit
10 <sub>H</sub>	Res.	Coefficient will be set via Coefficient RAM download
14 <sub>H</sub>	Res.	Coefficient will be set via Coefficient RAM download

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**Table 24 Coefficient Names (cont'd)**

<b>Offset</b>	<b>Short Name</b>	<b>Long Name</b>
18 <sub>H</sub>	PTG1	Tone Generator Coefficients Part 1 (for TG1 and TG2)
1C <sub>H</sub>	PTG2	Tone Generator Coefficients Part 2 (for TG1 and TG2)
20 <sub>H</sub>	Res.	Coefficient will be set via Coefficient RAM download
24 <sub>H</sub>	Res.	Coefficient will be set via Coefficient RAM download
28 <sub>H</sub>	Res.	Coefficient will be set via Coefficient RAM download
2C <sub>H</sub>	Res.	Coefficient will be set via Coefficient RAM download
30 <sub>H</sub>	Res.	Coefficient will be set via Coefficient RAM download
34 <sub>H</sub>	Res.	Coefficient will be set via Coefficient RAM download
38 <sub>H</sub>	Res.	Coefficient will be set via Coefficient RAM download
3C <sub>H</sub>	TTX	Teletax Coefficients
40 <sub>H</sub>	LM_AC	Level Meter AC
44 <sub>H</sub>	Res.	Coefficient will be set via Coefficient RAM download
48 <sub>H</sub>	RINGF	Ringer Frequency and Amplitude Coefficients (DC loop)
4C <sub>H</sub>	RINGO	Ringer Offset Coefficients
50 <sub>H</sub>	RINGI	Ring DC Characteristic
54 <sub>H</sub>	DCF1	DC Characteristic Part 1
58 <sub>H</sub>	DCF2	DC Characteristic Part 2
5C <sub>H</sub>	DCF3	DC Characteristic Part 3
60 <sub>H</sub>	HF1	Hook Detection Thresholds Part 1
64 <sub>H</sub>	HF2	Hook Detection Thresholds Part 2
68 <sub>H</sub>	RAMPF	Ramp Generator Coefficients (DC loop)
6C <sub>H</sub>	Res.	Reserved
70 <sub>H</sub>	Res.	Coefficient will be set via Coefficient RAM download
74 <sub>H</sub>	Res.	Coefficient will be set via Coefficient RAM download
78 <sub>H</sub>	Res.	Coefficient will be set via Coefficient RAM download
7C <sub>H</sub>	Res.	Coefficient will be set via Coefficient RAM download

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**Table 25 COP Registers (Coefficient RAM of the Analog-Line-Module)**

		Word 3 (Offset+3)			Word 2 (Offset+2)			Word 1 (Offset+1)			Word 0 (Offset+0)		
Offset	Flag	Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0	Byte 1	Byte 0	Byte 1	Byte 0
08 <sub>H</sub>	AR			AR1				Res.			Res.		
0C <sub>H</sub>	AX		Res.	AX1				Res.			Res.		
18 <sub>H</sub>	PTG1		BP2F	TG2F				BP1F			TG1F		
1C <sub>H</sub>	PTG2				BPQ1	BPQ2		TG2A			TG1A		
3C <sub>H</sub>	TTX		Res.		Res.			Res.	Res.		TTXA		
40 <sub>H</sub>	LM_AC		LM_TH		Res.			LMAC		BP3Q	BP3F		
48 <sub>H</sub>	RINGF		CREST		RGTP			V1			RGFR		
4C <sub>H</sub>	RINGO		RGD		RO3			RO2			RO1		
50 <sub>H</sub>	RINGI		I2		Vd			RI			IK_SH	RA_SH	
54 <sub>H</sub>	DCF1		RIK		IK1			VK1			VLM		
58 <sub>H</sub>	DCF2		RR		Res.			Res.			Res.		
5C <sub>H</sub>	DCF3		VTRL		KB			Res.			Res.		
60 <sub>H</sub>	HF1		HACRT		HRING			HACT			HPD		
64 <sub>H</sub>	HF2		FRTR		HAHY			HMW			HLS		
68 <sub>H</sub>	RAMPF			Res.	Res.	Res.	CRAMP	Res.			LMDC		

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## 7.4 Register Accessed with IOP Commands (PHI)

### 7.4.1 Mask Registers

Two types of mask registers are available for each status register. One type (MF-xxxx) masks the generation of interrupts for the status bits that change from 1 to 0 (falling). One type (MR-xxxx) masks the generation of interrupts for the status bits that change from 0 to 1 (rising). If the mask is disabled, the host has to read the corresponding interrupt status register in order to ensure that no interrupt is pending.

*Note: The default value of all mask bits is one. Recommended values to set the corresponding status bits as event or change interrupt sources are given in [Chapter 7.4.2](#).*

#### MR-SRE1 (Allocation R)

##### Mask Register for Status Register

for EDSP Interrupts 1 [M-V-C,CPE]

(00<sub>H</sub>)

Reset Value: FFFF<sub>H</sub>

15	14	13	12	11	10	9	8
M-DTMFR-DT	M-DTMFR-PDT	M-DTMFR-DTC				M-UTD1-OK	M-UTD2-OK
rw							
7	6	5	4	3	2	1	0
M-CPT	M-CIDR-OF	M-DTMFG-BUF	M-DTMFG-REQ	M-DTMFG-ACT/ M-UTG-ACT	M-CIS-BUF	M-CIS-REQ	M-CIS-ACT
rw							

Field	Bits	Type	Description
M-DTMFR-DT	15	rw	<b>Mask for DTMFR-DT Bit</b> 0 Not masked 1 Masked
M-DTMFR-PDT	14	rw	<b>Mask for DTMFR-PDT Bit</b> 0 Not masked 1 Masked
M-DTMFR-DTC	[13:10]	rw	<b>Mask for DTMFR-DTC Bits</b>
M-UTD1-OK	9	rw	<b>Mask for UTD1-OK Bit</b> 0 Not masked 1 Masked



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Field	Bits	Type	Description
<b>M-UTD2-OK</b>	8	rw	<b>Mask for UTD2-OK Bit</b> 0 Not masked 1 Masked
<b>M-CPT</b>	7	rw	<b>Mask for CPT Bit</b> 0 Not masked 1 Masked
<b>M-CIDR-OF</b>	6	rw	<b>Mask for CIDR-OF Bit</b> 0 Not masked 1 Masked
<b>M-DTMFG-BUF</b>	5	rw	<b>Mask for DTMFG-BUF Bit</b> 0 Not masked 1 Masked
<b>M-DTMFG-REQ</b>	4	rw	<b>Mask for DTMFG-REQ Bit</b> 0 Not masked 1 Masked
<b>M-DTMFG-ACT</b>	3	rw	<b>Mask for DTMFG-ACT Bit</b> 0 Not masked 1 Masked  <i>Note: Bit UTG-ACT and DTMFG-ACT are using the same bit position in SRE1 (overlaid). The DTMF / AT Generator can not be used simultaneously with the universal tone generator. The host must ensure that a DTMF/AT Generator and an UTG with the same resource number are not active at the same time!</i>
<b>M-UTG-ACT</b>	3	rw	<b>Mask for UTG-ACT Bit</b> 0 Not masked 1 Masked
<b>M-CIS-BUF</b>	2	rw	<b>Mask for CIS-BUF Bit</b> 0 Not masked 1 Masked
<b>M-CIS-REQ</b>	1	rw	<b>Mask for CIS-REQ Bit</b> 0 Not masked 1 Masked
<b>M-CIS-ACT</b>	0	rw	<b>Mask for CIS-ACT Bit</b> 0 Not masked 1 Masked

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*Note: Recommended values to set the corresponding status bits as event or change interrupt sources are given in **Chapter 7.4.2**.*

**CONFIDENTIAL**
**MR-SRE2 (Allocation R)**
**Mask Register for Status Register**
**for EDSP Interrupts 2 [M-V-C, CPE] (01<sub>H</sub>)**
**Reset Value: FFFF<sub>H</sub>**

15		14		13		12		11		10		9		8	
M-ATD1-DT		M-ATD1-NPR				M-ATD1-AM		M-ATD2-DT		M-ATD2-NPR				M-ATD2-AM	
rw															
7		6		5		4		3		2		1		0	
M-EPOU-STAT		M-ETU-OF		M-PVPU-OF/ M-PFDP-ERR		M-VPOU-STAT		M-VPOU-JBL		M-VPOU-JBH		1		M-DEC-CHG/ M-FDP-REQ	
rw															

Field	Bits	Type	Description
M-ATD1-DT	15	rw	<b>Mask for ATD1-DT Bit</b> 0 Not masked 1 Masked
M-ATD1-NPR	[14:13]	rw	<b>Mask for ATD1-NPR Bit</b> 0 Not masked 1 Masked
M-ATD1-AM	12	rw	<b>Mask for ATD1-AM Bit</b> 0 Not masked 1 Masked
M-ATD2-DT	11	rw	<b>Mask for ATD2-DT Bit</b> 0 Not masked 1 Masked
M-ATD2-NPR	[10:9]	rw	<b>Mask for ATD2-NPR Bits</b> 0 Not masked 1 Masked
M-ATD2-AM	8	rw	<b>Mask for ATD2-AM Bit</b> 0 Not masked 1 Masked
M-EPOU-STAT	7	rw	<b>Mask for EPOU-STAT Bit</b> 0 Not masked 1 Masked
M-ETU-OF	6	rw	<b>Mask for ETU-OF Bit</b> 0 Not masked 1 Masked

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Field	Bits	Type	Description
<b>M-PVPU-OF</b>	5	rw	<b>Mask for PVPU-OF Bit</b> 0 Not masked 1 Masked  <i>Note: Coder Channel Speech Compression and FAX Data Pump can not be active at the same time for one and the same channel. Depending on which module is active for a channel, this bit positions indicates either the status of the Coder Channel Speech Compression (PVPU-OF) or the status of the FAX Data Pump (FDP-ERR)</i>
<b>M-FDP-ERR</b>	5	rw	<b>Mask for FDP-ERR Bit</b> 0 Not masked 1 Masked
<b>M-VPOU-STAT</b>	4	rw	<b>Mask for VPOU-STAT Bit</b> 0 Not masked 1 Masked
<b>M-VPOU-JBL</b>	3	rw	<b>Mask for VPOU-JBL Bit</b> 0 Not masked 1 Masked
<b>M-VPOU-JBH</b>	2	rw	<b>Mask for VPOU-JBH Bit</b> 0 Not masked 1 Masked
<b>M-DEC-CHG</b>	0	rw	<b>Mask for DEC-CHG Bit</b> 0 Not masked 1 Masked  <i>Note: Coder Channel Speech Compression and FAX Data Pump can not be active at the same time for one and the same channel. Depending on which module is active for a channel, this bit positions indicates either the status of the Coder Channel Speech Compression (DEC-CHG) or the status of the FAX Data Pump (FDP-REQ)</i>
<b>M-FDP-REQ</b>	0	rw	<b>Mask for FDP-REQ Bit</b> 0 Not masked 1 Masked

**CONFIDENTIAL**
**MR-SRS1 (Allocation C)**
**Mask Register for Status Register for**
**Analog-Line-Module Interrupts 1 (02<sub>H</sub>)**
**Reset Value: FFFF<sub>H</sub>**

15	14	13	12	11	10	9	8
M-AUTO-MET-DONE	M-RAMP-READY	M-HOOK	M-GNDK	M-GNKP	M-GNDKH	M-ICON	M-VTRLIM
rw							
7	6	5	4	3	2	1	0
1	M-LM-THRES	M-LM-OK	M-DU-IO				
rw							

Field	Bits	Type	Description
<b>M-AUTO-MET-DONE</b>	15	rw	<b>Mask for 0 Bit</b> 0 Not masked 1 Masked
<b>M-RAMP-READY</b>	14	rw	<b>Mask for RAMP-READY Bit</b> 0 Not masked 1 Masked
<b>M-HOOK</b>	13	rw	<b>Mask for HOOK Bit</b> 0 Not masked 1 Masked
<b>M-GNDK</b>	12	rw	<b>Mask for GNDK Bit</b> 0 Not masked 1 Masked
<b>M-GNKP</b>	11	rw	<b>Mask for GNKP Bit</b> 0 Not masked 1 Masked
<b>M-GNDKH</b>	10	rw	<b>Mask for GNDKH Bit</b> 0 Not masked 1 Masked
<b>M-ICON</b>	9	rw	<b>Mask for ICON Bit</b> 0 Not masked 1 Masked
<b>M-VTRLIM</b>	8	rw	<b>Mask for VTRLIM Bit</b> 0 Not masked 1 Masked

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Field	Bits	Type	Description
<b>M-LM-THRES</b>	6	rw	<b>Mask for LM-THRES Bit</b> 0 Not masked 1 Masked
<b>M-LM-OK</b>	5	rw	<b>Mask for LM-OK Bit</b> 0 Not masked 1 Masked
<b>M-DU-IO</b>	[4:0]	rw	<b>Mask for DU-IO Bits</b>

**CONFIDENTIAL**
**MR-SRS2 (Allocation C)**
**Mask Register for Status Register for**
**Analog-Line-Module Interrupts 2 (03<sub>H</sub>)**
**Reset Value: FFFF<sub>H</sub>**

15	14	13	12	11	10	9	8
1	1	1	1	1	1	1	1

rw

7	6	5	4	3	2	1	0
1	1	1	1	M-OTEMP	M-CS-FAIL-CRAM	M-CS-FAIL-DSP	M-CS-FAIL-DCCTL

rw

Field	Bits	Type	Description
<b>M-OTEMP</b>	3	rw	<b>Mask for OTEMP Bit</b> 0 Not masked 1 Masked
<b>M-CS-FAIL-CRAM</b>	2	rw	<b>Mask for CS-FAIL-CRAM Bit</b> 0 Not masked 1 Masked
<b>M-CS-FAIL-DSP</b>	1	rw	<b>Mask for CS-FAIL-DSP Bit</b> 0 Not masked 1 Masked
<b>M-CS-FAIL-DCCTL</b>	0	rw	<b>Mask for CS-FAIL-DCCTL Bit</b> 0 Not masked 1 Masked

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**MR-HWSR1 (Allocation D)**
**Mask Register for**
**Hardware Status Register 1**
**(12<sub>H</sub>)**
**Reset Value: F7F6<sub>H</sub>**

15	14	13	12	11	10	9	8
1	1	1	1	M-SYNC-FAIL	1	M-TXB-CRASH	M-TXA-CRASH

rw

7	6	5	4	3	2	1	0
M-EDSP-WD-FAIL	1	1	1	M-MCLK-FAIL	M-WOKE-UP	1	M-HW-ERR

rw

Field	Bits	Type	Description
M-SYNC-FAIL	11	rw	<b>Mask for SYNC-FAIL Bit</b> 0 Not masked 1 Masked
M-TXB-CRASH	9	rw	<b>Mask for TXB-CRASH Bit</b> 0 Not masked 1 Masked
M-TXA-CRASH	8	rw	<b>Mask for TXA-CRASH Bit</b> 0 Not masked 1 Masked
M-EDSP-WD-FAIL	7	rw	<b>Mask for EDSP-WD-FAIL Bit</b> 0 Not masked 1 Masked
M-MCLK-FAIL	3	rw	<b>Mask for MCLK-FAIL Bit</b> 0 Not masked 1 Masked
M-WOKE-UP	2	rw	<b>Mask for WOKE-UP Bit</b> 0 Not masked 1 Masked
M-HW-ERR	0	rw	<b>Mask for HW-ERR Bit</b> 0 Not masked 1 Masked



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**MR-HWSR2 (Allocation D)**
**Mask Register for**
**Hardware Status Register 2**
**(13<sub>H</sub>)**
**Reset Value: FEFF<sub>H</sub>**

15	14	13	12	11	10	9	8
1	1	1	1	1	1	1	M-DL-RDY

rw

7	6	5	4	3	2	1	0
1	1	1	1	1	M-CRC-RDY	M-CRC-ERR	M-EDSP-MIPS-OL

rw

Field	Bits	Type	Description
M-DL-RDY	8	rw	<b>Mask for DL-RDY Bit</b> 0 Not masked 1 Masked
M-CRC-RDY	2	rw	<b>Mask for CRC-RDY Bit</b> 0 Not masked 1 Masked
M-CRC-ERR	1	rw	<b>Mask for CRC-ERR Bit</b> 0 Not masked 1 Masked
M-EDSP-MIPS-OL	0	rw	<b>Mask for EDSP-MIPS-OL Bit</b> 0 Not masked 1 Masked

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**MR-BXSR1 (Allocation D)**

**Mask Register for**

**Mailbox Status Register 1**

**(16<sub>H</sub>)**

**Reset Value: FEFF<sub>H</sub>**

15	14	13	12	11	10	9	8
1	1	1	1	1	1	1	<b>M-CERR</b>

rw

7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1

rw

Field	Bits	Type	Description
<b>M-CERR</b>	8	rw	<b>Mask for CERR Bit</b> 0 Not masked 1 Masked

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**MR-BXSR2 (Allocation D)**
**Mask Register for**
**Mailbox Status Register 2**
**(17<sub>H</sub>)**
**Reset Value: FFC0<sub>H</sub>**

15	14	13	12	11	10	9	8
1	1	1	1	1	1	1	1

rw

7	6	5	4	3	2	1	0
1	1	M-HOST- ERR	M-POBX- DATA	M-COBX- DATA	M-PIBX- OF	M-CIBX- OF	M-MBX- EMPTY

rw

Field	Bits	Type	Description
M-HOST- ERR	5	rw	<b>Mask for HOST-ERR Bit</b> 0 Not masked 1 Masked
M-POBX- DATA	4	rw	<b>Mask for POBX-DATA Bit [M-V-CPE]</b> 0 Not masked 1 Masked
M-COBX- DATA	3	rw	<b>Mask for COBX-DATA Bit</b> 0 Not masked 1 Masked
M-PIBX- OF	2	rw	<b>Mask for PIBX-OF Bit [M-V-CPE]</b> 0 Not masked 1 Masked
M-CIBX- OF	1	rw	<b>Mask for CIBX-OF Bit</b> 0 Not masked 1 Masked
M-MBX- EMPTY	0	rw	<b>Mask for MBX-EMPTY Bit</b> 0 Not masked 1 Masked

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**MR-SRGPIO (Allocation D)**
**Mask Register for**
**Status Register for GPIO interrupts (1A<sub>H</sub>)**
**Reset Value: FFFF<sub>H</sub>**

15	14	13	12	11	10	9	8
1	1	1	1	1	1	1	1

rw

7	6	5	4	3	2	1	0
M-GPIO7	M-GPIO6	M-GPIO5	M-GPIO4	M-GPIO3	M-GPIO2	M-GPIO1	M-GPIO0

rw

Field	Bits	Type	Description
M-GPIO7	7	rw	<b>Mask for GPIO7 Bit</b> 0 Not masked 1 Masked
M-GPIO6	6	rw	<b>Mask for GPIO6 Bit</b> 0 Not masked 1 Masked
M-GPIO5	5	rw	<b>Mask for GPIO5 Bit</b> 0 Not masked 1 Masked
M-GPIO4	4	rw	<b>Mask for GPIO4 Bit</b> 0 Not masked 1 Masked
M-GPIO3	3	rw	<b>Mask for GPIO3 Bit</b> 0 Not masked 1 Masked
M-GPIO2	2	rw	<b>Mask for GPIO2 Bit</b> 0 Not masked 1 Masked
M-GPIO1	1	rw	<b>Mask for GPIO1 Bit</b> 0 Not masked 1 Masked
M-GPIO0	0	rw	<b>Mask for GPIO0 Bit</b> 0 Not masked 1 Masked

**CONFIDENTIAL**
**MF-SRE1 (Allocation R)**
**Mask Register for Status Register**
**for EDSP Interrupts 1 [M-V-C, CPE] (60<sub>H</sub>)**
**Reset Value: FFFF<sub>H</sub>**

15	14	13	12	11	10	9	8
M-DTMFR-DT	M-DTMFR-PDT	M-DTMFR-DTC				M-UTD1-OK	M-UTD2-OK
rw							
7	6	5	4	3	2	1	0
1	1	M-DTMFG-BUF	M-DTMFG-REQ	M-DTMFG-ACT/ M-UTG-ACT	M-CIS-BUF	M-CIS-REQ	M-CIS-ACT
rw							

Field	Bits	Type	Description
<b>M-DTMFR-DT</b>	15	rw	<b>Mask for DTMFR-DT Bit</b> 0 Not masked 1 Masked
<b>M-DTMFR-PDT</b>	14	rw	<b>Mask for DTMFR-PDT Bit</b> 0 Not masked 1 Masked
<b>M-DTMFR-DTC</b>	[13:10]	rw	<b>Mask for DTMFR-DTC Bits</b>
<b>M-UTD1-OK</b>	9	rw	<b>Mask for UTD1-OK Bit</b> 0 Not masked 1 Masked
<b>M-UTD2-OK</b>	8	rw	<b>Mask for UTD2-OK Bit</b> 0 Not masked 1 Masked
<b>M-DTMFG-BUF</b>	5	rw	<b>Mask for DTMFG-BUF Bit</b> 0 Not masked 1 Masked
<b>M-DTMFG-REQ</b>	4	rw	<b>Mask for DTMFG-REQ Bit</b> 0 Not masked 1 Masked

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Field	Bits	Type	Description
<b>M-DTMFG-ACT</b>	3	rw	<b>Mask for DTMFG-ACT Bit</b> 0 Not masked 1 Masked  <i>Note: Bit UTG-ACT and DTMFG-ACT are using the same bit position in SRE1 (overlaid).            The DTMF / AT Generator can not be used simultaneously with the universal tone generator.            The host must ensure that a DTMF/AT Generator and an UTG with the same resource number are not active at the same time!</i>
<b>M-UTG-ACT</b>	3	rw	<b>Mask for UTG-ACT Bit</b> 0 Not masked 1 Masked
<b>M-CIS-BUF</b>	2	rw	<b>Mask for CIS-BUF Bit</b> 0 Not masked 1 Masked
<b>M-CIS-REQ</b>	1	rw	<b>Mask for CIS-REQ Bit</b> 0 Not masked 1 Masked
<b>M-CIS-ACT</b>	0	rw	<b>Mask for CIS-ACT Bit</b> 0 Not masked 1 Masked

**CONFIDENTIAL**
**MF-SRE2 (Allocation R)**
**Mask Register for Status Register**
**for EDSP Interrupts 2 [M-V-C, CPE] (61<sub>H</sub>)**
**Reset Value: FFFF<sub>H</sub>**

15	14	13	12	11	10	9	8
<b>M-ATD1-DT</b>	<b>M-ATD1-NPR</b>		<b>M-ATD1-AM</b>	<b>M-ATD2-DT</b>	<b>M-ATD2-NPR</b>		<b>M-ATD2-AM</b>

rw

7	6	5	4	3	2	1	0
<b>1</b>	<b>M-ETU-OF</b>	<b>M-PVPU-OF/ M-FDP-ERR</b>	<b>M-VPOU-STAT</b>	<b>M-VPOU-JBL</b>	<b>M-VPOU-JBH</b>	<b>M-DEC-ERR</b>	<b>M-DEC-CHG/ M-FDP-REQ</b>

rw

Field	Bits	Type	Description
<b>M-ATD1-DT</b>	15	rw	<b>Mask for ATD1-DT Bit</b> 0 Not masked 1 Masked
<b>M-ATD1-NPR</b>	[14:13]	rw	<b>Mask for ATD1-NPR Bit</b> 0 Not masked 1 Masked
<b>M-ATD1-AM</b>	12	rw	<b>Mask for ATD1-AM Bit</b> 0 Not masked 1 Masked
<b>M-ATD2-DT</b>	11	rw	<b>Mask for ATD2-DT Bit</b> 0 Not masked 1 Masked
<b>M-ATD2-NPR</b>	[10:9]	rw	<b>Mask for ATD2-NPR Bits</b> 0 Not masked 1 Masked
<b>M-ATD2-AM</b>	8	rw	<b>Mask for ATD2-AM Bit</b> 0 Not masked 1 Masked
<b>M-ETU-OF</b>	6	rw	<b>Mask for ETU-OF Bit</b> 0 Not masked 1 Masked

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Field	Bits	Type	Description
<b>M-PVPU-OF</b>	5	rw	<b>Mask for PVPU-OF Bit</b> 0 Not masked 1 Masked  <i>Note: Coder Channel Speech Compression and FAX Data Pump can not be active at the same time for one and the same channel. Depending on which module is active for a channel, this bit positions indicates either the status of the Coder Channel Speech Compression (PVPU-OF) or the status of the FAX Data Pump (FDP-ERR)</i>
<b>M-FDP-ERR</b>	5	rw	<b>Mask for FDP-ERR Bit</b> 0 Not masked 1 Masked
<b>M-VPOU-STAT</b>	4	rw	<b>Mask for M-VPOU-STAT Bit</b> 0 Not masked 1 Masked
<b>M-VPOU-JBL</b>	3	rw	<b>Mask for VPOU-JBL Bit</b> 0 Not masked 1 Masked
<b>M-VPOU-JBH</b>	2	rw	<b>Mask for VPOU-JBH Bit</b> 0 Not masked 1 Masked
<b>M-DEC-ERR</b>	1	rw	<b>Mask for DEC-ERR Bit</b> 0 Not masked 1 Masked
<b>M-DEC-CHG</b>	0	rw	<b>Mask for DEC-CHG Bit</b> 0 Not masked 1 Masked  <i>Note: Coder Channel Speech Compression and FAX Data Pump can not be active at the same time for one and the same channel. Depending on which module is active for a channel, this bit positions indicates either the status of the Coder Channel Speech Compression (DEC-CHG) or the status of the FAX Data Pump (FDP-REQ)</i>
<b>M-FDP-REQ</b>	0	rw	<b>Mask for FDP-REQ Bit</b> 0 Not masked 1 Masked



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**MF-SRS1 (Allocation C)**
**Mask Register for Status Register for**
**Analog-Line-Module Interrupts 1 (62<sub>H</sub>)**
**Reset Value: FFFF<sub>H</sub>**

15	14	13	12	11	10	9	8
M-AUTO-MET-DONE	M-RAMP-READY	M-HOOK	M-GNDK	M-GNKP	M-GNDKH	M-ICON	M-VTRLIM
rw							
7	6	5	4	3	2	1	0
1	M-LM-THRES	M-LM-OK	M-DU-IO				
rw							

Field	Bits	Type	Description
<b>M-AUTO-MET-DONE</b>	15	rw	<b>Mask for 0 Bit</b> 0 Not masked 1 Masked
<b>M-RAMP-READY</b>	14	rw	<b>Mask for RAMP-READY Bit</b> 0 Not masked 1 Masked
<b>M-HOOK</b>	13	rw	<b>Mask for HOOK Bit</b> 0 Not masked 1 Masked
<b>M-GNDK</b>	12	rw	<b>Mask for GNDK Bit</b> 0 Not masked 1 Masked
<b>M-GNKP</b>	11	rw	<b>Mask for GNKP Bit</b> 0 Not masked 1 Masked
<b>M-GNDKH</b>	10	rw	<b>Mask for GNDKH Bit</b> 0 Not masked 1 Masked
<b>M-ICON</b>	9	rw	<b>Mask for ICON Bit</b> 0 Not masked 1 Masked
<b>M-VTRLIM</b>	8	rw	<b>Mask for VTRLIM Bit</b> 0 Not masked 1 Masked

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Field	Bits	Type	Description
<b>M-LM-THRES</b>	6	rw	<b>Mask for LM-THRES Bit</b> 0 Not masked 1 Masked
<b>M-LM-OK</b>	5	rw	<b>Mask for LM-OK Bit</b> 0 Not masked 1 Masked
<b>M-DU-IO</b>	[4:0]	rw	<b>Mask for DU-IO Bits</b>

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**MF-SRS2 (Allocation C)**
**Mask Register for Status Register for**
**Analog-Line-Module Interrupts 2 (63<sub>H</sub>)**
**Reset Value: FFFF<sub>H</sub>**

15	14	13	12	11	10	9	8
1	1	1	1	1	1	1	1

rw

7	6	5	4	3	2	1	0
1	1	1	1	M-OTEMP	M-CS-FAIL-CRAM	M-CS-FAIL-DSP	M-CS-FAIL-DCCTL

rw

Field	Bits	Type	Description
<b>M-OTEMP</b>	3	rw	<b>Mask for OTEMP Bit</b> 0 Not masked 1 Masked
<b>M-CS-FAIL-CRAM</b>	2	rw	<b>Mask for CS-FAIL-CRAM Bit</b> 0 Not masked 1 Masked
<b>M-CS-FAIL-DSP</b>	1	rw	<b>Mask for CS-FAIL-DSP Bit</b> 0 Not masked 1 Masked
<b>M-CS-FAIL-DCCTL</b>	0	rw	<b>Mask for CS-FAIL-DCCTL Bit</b> 0 Not masked 1 Masked

**CONFIDENTIAL**
**MF-HWSR1 (Allocation D)**
**Mask Register for**
**Hardware Status Register 1**
**(72<sub>H</sub>)**
**Reset Value: FFFF<sub>H</sub>**

15	14	13	12	11	10	9	8
1	1	1	1	M-SYNC-FAIL	1	M-TXB-CRASH	M-TXA-CRASH

rw

7	6	5	4	3	2	1	0
M-EDSP-WD-FAIL	1	1	1	M-MCLK-FAIL	M-WOKE-UP	1	M-HW-ERR

rw

Field	Bits	Type	Description
M-SYNC-FAIL	11	rw	<b>Mask for SYNC-FAIL Bit</b> 0 Not masked 1 Masked
M-TXB-CRASH	9	rw	<b>Mask for TXB-CRASH Bit</b> 0 Not masked 1 Masked
M-TXA-CRASH	8	rw	<b>Mask for TXA-CRASH Bit</b> 0 Not masked 1 Masked
M-EDSP-WD-FAIL	7	rw	<b>Mask for EDSP-WD-FAIL Bit</b> 0 Not masked 1 Masked
M-MCLK-FAIL	3	rw	<b>Mask for MCLK-FAIL Bit</b> 0 Not masked 1 Masked
M-WOKE-UP	2	rw	<b>Mask for WOKE-UP Bit</b> 0 Not masked 1 Masked
M-HW-ERR	0	rw	<b>Mask for HW-ERR Bit</b> 0 Not masked 1 Masked

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**MF-HWSR2 (Allocation D)**
**Mask Register for**
**Hardware Status Register 2**
**(73<sub>H</sub>)**
**Reset Value: FFFF<sub>H</sub>**

15	14	13	12	11	10	9	8
1	1	1	1	1	1	1	M-DL-RDY

rw

7	6	5	4	3	2	1	0
1	1	1	1	1	M-CRC-RDY	M-CRC-ERR	M-EDSP-MIPS-OL

rw

Field	Bits	Type	Description
M-DL-RDY	8	rw	<b>Mask for DL-RDY Bit</b> 0 Not masked 1 Masked
M-CRC-RDY	2	rw	<b>Mask for CRC-RDY Bit</b> 0 Not masked 1 Masked
M-CRC-ERR	1	rw	<b>Mask for CRC-ERR Bit</b> 0 Not masked 1 Masked
M-EDSP-MIPS-OL	0	rw	<b>Mask for EDSP-MIPS-OL Bit</b> 0 Not masked 1 Masked

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**MF-BXSR1 (Allocation D)**

**Mask Register for**

**Mailbox Status Register 1**

**(76<sub>H</sub>)**

**Reset Value: FFFF<sub>H</sub>**

15	14	13	12	11	10	9	8
1	1	1	1	1	1	1	<b>M-CERR</b>

rw

7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1

rw

Field	Bits	Type	Description
<b>M-CERR</b>	8	rw	<b>Mask for CERR Bit</b> 0 Not masked 1 Masked

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**MF-BXSR2 (Allocation D)**
**Mask Register for**
**Mailbox Status Register 2**
**(77<sub>H</sub>)**
**Reset Value: FFFF<sub>H</sub>**

15	14	13	12	11	10	9	8
1	1	1	1	1	1	1	1

rw

7	6	5	4	3	2	1	0
1	1	M-HOST- ERR	M-POBX- DATA	M-COBX- DATA	M-PIBX- OF	M-CIBX- OF	M-MBX- EMPTY

rw

Field	Bits	Type	Description
M-HOST- ERR	5	rw	<b>Mask for HOST-ERR Bit</b> 0 Not masked 1 Masked
M-POBX- DATA	4	rw	<b>Mask for POBX-DATA Bit [M-V-CPE]</b> 0 Not masked 1 Masked
M-COBX- DATA	3	rw	<b>Mask for COBX-DATA Bit</b> 0 Not masked 1 Masked
M-PIBX- OF	2	rw	<b>Mask for PIBX-OF Bit [M-V-CPE]</b> 0 Not masked 1 Masked
M-CIBX- OF	1	rw	<b>Mask for CIBX-OF Bit</b> 0 Not masked 1 Masked
M-MBX- EMPTY	0	rw	<b>Mask for MBX-EMPTY Bit</b> 0 Not masked 1 Masked

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**MF-SRGPIO (Allocation D)**
**Mask Register for**
**Status Register for GPIO interrupts (7A<sub>H</sub>)**
**Reset Value: FFFF<sub>H</sub>**

15	14	13	12	11	10	9	8
1	1	1	1	1	1	1	1

rw

7	6	5	4	3	2	1	0
M-GPIO7	M-GPIO6	M-GPIO5	M-GPIO4	M-GPIO3	M-GPIO2	M-GPIO1	M-GPIO0

rw

Field	Bits	Type	Description
M-GPIO7	7	rw	<b>Mask for GPIO7 Bit</b> 0 Not masked 1 Masked
M-GPIO6	6	rw	<b>Mask for GPIO6 Bit</b> 0 Not masked 1 Masked
M-GPIO5	5	rw	<b>Mask for GPIO5 Bit</b> 0 Not masked 1 Masked
M-GPIO4	4	rw	<b>Mask for GPIO4 Bit</b> 0 Not masked 1 Masked
M-GPIO3	3	rw	<b>Mask for GPIO3 Bit</b> 0 Not masked 1 Masked
M-GPIO2	2	rw	<b>Mask for GPIO2 Bit</b> 0 Not masked 1 Masked
M-GPIO1	1	rw	<b>Mask for GPIO1 Bit</b> 0 Not masked 1 Masked
M-GPIO0	0	rw	<b>Mask for GPIO0 Bit</b> 0 Not masked 1 Masked



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## 7.4.2 Recommended Values for Rising and Falling Edge Mask Registers

Depending on the Mask Register values the status bits in the Status Register can generate

- no interrupts
- interrupts on rising(0→ 1) or falling (1→ 0) events of these bits
- interrupts on all changes (i.e if the bit changes from 0→ 1 or 1→ 0) of these bits

In order to have reasonable behavior of interrupts, in [Table 26 on Page 185](#) a proposal for Mask Register values for enabled interrupts are given.

**Table 26 Recommended Mask Register Values for Enabled Interrupts**

Register	Offset	Reset Value	Recommended Enable Value
MR-HWSR1	12 <sub>H</sub>	F3F6 <sub>H</sub>	F072 <sub>H</sub>
MF-HWSR1	72 <sub>H</sub>	FFFF <sub>H</sub>	FFFF <sub>H</sub>
MR-HWSR2	13 <sub>H</sub>	FEFF <sub>H</sub>	FEFE <sub>H</sub>
MF-HWSR2	73 <sub>H</sub>	FFFF <sub>H</sub>	FFFF <sub>H</sub>
MR-BXSR1	16 <sub>H</sub>	FEFF <sub>H</sub>	FEFF <sub>H</sub>
MF-BXSR1	76 <sub>H</sub>	FFFF <sub>H</sub>	FFFF <sub>H</sub>
MR-BXSR2	17 <sub>H</sub>	FFC0 <sub>H</sub>	FFC0 <sub>H</sub>
MF-BXSR2	77 <sub>H</sub>	FFFF <sub>H</sub>	FFFF <sub>H</sub>
MR-SRGPIO	1A <sub>H</sub>	FFFF <sub>H</sub>	FF00 <sub>H</sub>
MF-SRGPIO	7A <sub>H</sub>	FFFF <sub>H</sub>	FF00 <sub>H</sub>
MR-SRS1	02 <sub>H</sub>	FFFF <sub>H</sub>	8080 <sub>H</sub>
MF-SRS1	62 <sub>H</sub>	FFFF <sub>H</sub>	C0A0 <sub>H</sub>
MR-SRS2	03 <sub>H</sub>	FFFF <sub>H</sub>	FFF0 <sub>H</sub>
MF-SRS2	63 <sub>H</sub>	FFFF <sub>H</sub>	FFFF <sub>H</sub>
MR-SRE1	00 <sub>H</sub>	FFFF <sub>H</sub>	00C0 <sub>H</sub>
MF-SRE1	60 <sub>H</sub>	FFFF <sub>H</sub>	03FF <sub>H</sub>
MR-SRE2	01 <sub>H</sub>	FFFF <sub>H</sub>	0080 <sub>H</sub>
MF-SRE2	61 <sub>H</sub>	FFFF <sub>H</sub>	11FF <sub>H</sub>

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### 7.4.3 Common Registers

#### OPMOD-SRC (Allocation C)

##### Operating Mode

##### Status Register Source

(20<sub>H</sub>)

Reset Value: 0000<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	MODE-SRC				SUBMODE-SRC				0	0	0	0

r

Field	Bits	Type	Description
MODE-SRC	[11:8]	r	<b>Operating Mode - Source</b> The source operating mode is the mode lastly written by the host (see also <a href="#">Table 6 on Page 57</a> )
SUBMODE-SRC	[7:4]	r	<b>Operating Submode - Source</b> The source operating sub-mode is the sub-mode lastly written by the host (see also <a href="#">Table 6 on Page 57</a> ).

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## OPMOD-CUR (Allocation C)

### Operating Mode

#### Status Register Current

(21<sub>H</sub>)

Reset Value: 0000<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	Res.	MODE-CUR				SUBMODE-CUR				0 <sub>H</sub>			

r

Field	Bits	Type	Description
Res	12	r	Reserved
MODE-CUR	[11:8]	r	<b>Current Operating Mode</b> Because of automatic modes the current operating mode may differ from the source operating mode lastly written by the host (see also <a href="#">Table 6 on Page 57</a> ).
SUBMOD E-CUR	[7:4]	r	<b>Current Operating Submode</b> Because of automatic modes the current sub-mode may differ from the source sub-mode lastly written by the host (see also <a href="#">Table 6 on Page 57</a> ).

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**REVISION (Allocation D)**

**Revision Number (read-only) (40<sub>H</sub>) Reset Value:2484<sub>H</sub>**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>TYPE</b>				<b>ANA-CHAN</b>				<b>REV</b>							

Field	Bits	Type	Description
<b>TYPE</b>	[15:12]	r	<b>Type Of Device</b> 0000 Reserved 0001 Reserved 0010 VIP-Version 0100 Reserved 1111 Reserved
<b>ANA-CHAN</b>	[11:8]	r	<b>Analog Channels</b> Number of analog channels which are supported by this device. 0000 Reserved 0001 Reserved 0010 Reserved 0011 Reserved 0100 Four channels 0101 Reserved 0110 Reserved 0111 Reserved 1000 Reserved . . . . Reserved 1111 Reserved
<b>REV</b>	[7:0]	r	<b>Revision</b> Current HW-/PHI-FW-revision of the VINETIC®-x bit 4 is reserved 01000010 for V1.1, V1.2, V1.3 10000100 for V1.4

*Note: The version for the EDSP firmware can be read by the EOP-Command "EDSP SW Version Register" (see Preliminary User's Manual - EDSP Firmware Description).*

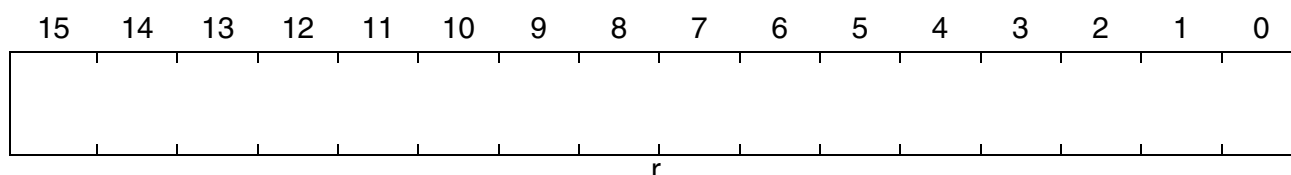
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**CHIPID1 (Allocation D)**

**Chip Identification 1 (read-only)**

**(41<sub>H</sub>)**

**Reset Value: hw**



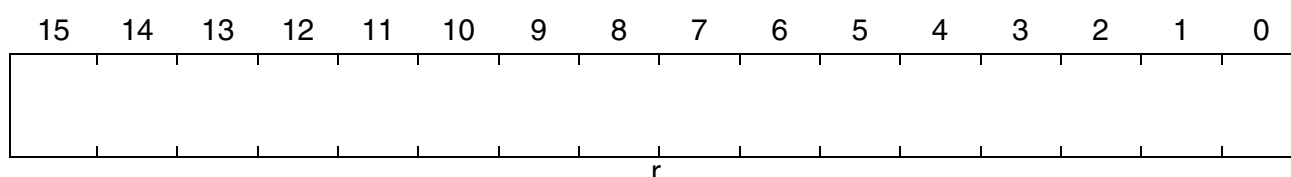
For internal use.

**CHIPID2 (Allocation D)**

**Chip Identification 2 (read-only)**

**(42<sub>H</sub>)**

**Reset Value: hw**



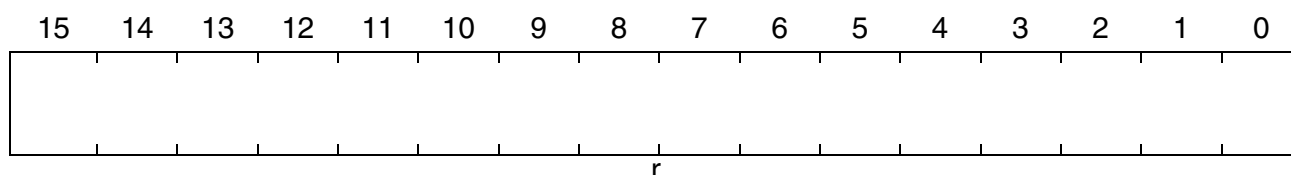
For internal use.

**CHIPID3 (Allocation D)**

**Chip Identification 3 (read-only)**

**(43<sub>H</sub>)**

**Reset Value: hw**



For internal use.

**CONFIDENTIAL**
**GCONF (Allocation D)**
**Global Configuration Register**
**(44<sub>H</sub>)**
**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0

rw

7	6	5	4	3	2	1	0
HOOKD-EN	HOOKC-EN	HOOKB-EN	HOOKA-EN	0	PP-EN-RDYQ	WDG-EN	PRG-FUSE

rw

Field	Bits	Type	Description
<b>HOOKD-EN</b>	7	rw	<b>Enable hardware hook indication for channel D</b> Enable onhook/offhook indication for channel D on GPIO7. GPIO7 has to be set as output. 0 Hardware hook indication disabled 1 Hardware hook indication enabled GPIO7 = 0 On-hook in channel D detected GPIO7 = 1 Off-hook in channel D detected
<b>HOOKC-EN</b>	6	rw	<b>Enable hardware hook indication for channel C</b> Enable onhook/offhook indication for channel C on GPIO6. GPIO6 has to be set as output. 0 Hardware hook indication disabled 1 Hardware hook indication enabled GPIO6 = 0 On-hook in channel C detected GPIO6 = 1 Off-hook in channel C detected
<b>HOOKB-EN</b>	5	rw	<b>Enable hardware hook indication for channel B</b> Enable onhook/offhook indication for channel B on GPIO5. GPIO5 has to be set as output. 0 Hardware hook indication disabled 1 Hardware hook indication enabled GPIO5 = 0 On-hook in channel B detected GPIO5 = 1 Off-hook in channel B detected

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Field	Bits	Type	Description
<b>HOOKA-EN</b>	4	rw	<b>Enable hardware hook indication for channel A c</b> Enable onhook/offhook indication for channel A on GPIO4. GPIO4 has to be set as output. 0     Hardware hook indication disabled 1     Hardware hook indication enabled GPIO4 = 0 On-hook in channel A detected GPIO4 = 1 Off-hook in channel A detected
<b>PP-EN-RDYQ</b>	2	rw	<b>Push-Pull Enable RDYQ</b> Push-pull enable for the RDYQ (IFC8) pin. 0     Output with open source (!) (Z/1) 1     Push-pull behavior (0/1)
<b>WDG-EN</b>	1	rw	<b>Enable Watchdog</b> 0     Watchdog disabled 1     Watchdog enabled
<b>PRG-FUSE</b>	0	rw	<b>Programmable Fuse</b> For internal use

**CONFIDENTIAL**

**EDSPFUSE (Allocation D)**

**EDSP Fuse Register**

**(45<sub>H</sub>)**

**Reset Value: hw**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

(rw)

For internal use.

**PLLCTRL (Allocation D)**

**PLL Control Register**

**(46<sub>H</sub>)**

**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

(rw)

For internal use.



**CONFIDENTIAL**

## 7.4.4 Other PHI Related Registers

### GCR1 (Allocation D)

#### GPIO Configuration Register 1

**(47<sub>H</sub>)**
**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
rw							
7	6	5	4	3	2	1	0
DD-GPIO7	DD-GPIO6	DD-GPIO5	DD-GPIO4	DD-GPIO3	DD-GPIO2	DD-GPIO1	DD-GPIO0
rw							

Field	Bits	Type	Description
<b>DD-GPIO7</b>	7	rw	<b>Output Value GPIO7</b> Value for the programmable I/O pin GPIO7 if programmed as an output pin. 0 Pin GPIO7 is driving a logic 0 1 Pin GPIO7 is driving a logic 1
<b>DD-GPIO6</b>	6	rw	<b>Output Value GPIO6</b> Value for the programmable I/O pin GPIO6 if programmed as an output pin. an output pin and PHI is master 0 Pin GPIO6 is driving a logic 0 1 Pin GPIO6 is driving a logic 1
<b>DD-GPIO5</b>	5	rw	<b>Output Value GPIO5</b> Value for the programmable I/O pin GPIO5 if programmed as an output pin. 0 Pin GPIO5 is driving a logic 0 1 Pin GPIO5 is driving a logic 1
<b>DD-GPIO4</b>	4	rw	<b>Output Value GPIO4</b> Value for the programmable I/O pin GPIO4 if programmed as an output pin. 0 Pin GPIO4 is driving a logic 0 1 Pin GPIO4 is driving a logic 1

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Field	Bits	Type	Description
<b>DD-GPIO3</b>	3	rw	<b>Output Value GPIO3</b> Value for the programmable I/O pin GPIO3 if programmed as an output pin. 0 Pin GPIO3 is driving a logic 0 1 Pin GPIO3 is driving a logic 1
<b>DD-GPIO2</b>	2	rw	<b>Output Value GPIO2</b> Value for the programmable I/O pin GPIO2 if programmed as an output pin. 0 Pin GPIO2 is driving a logic 0 1 Pin GPIO2 is driving a logic 1
<b>DD-GPIO1</b>	1	rw	<b>Output Value GPIO1</b> Value for the programmable I/O pin GPIO1 if programmed as an output pin. 0 Pin GPIO1 is driving a logic 0 1 Pin GPIO1 is driving a logic 1
<b>DD-GPIO0</b>	0	rw	<b>Output Value GPIO0</b> Value for the programmable I/O pin GPIO0 if programmed as an output pin. 0 Pin GPIO0 is driving a logic 0 1 Pin GPIO0 is driving a logic 1

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**GCR2 (Allocation D)**
**GPIO Configuration Register 2**
**(48<sub>H</sub>)**
**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
IEN-GPIO7	IEN-GPIO6	IEN-GPIO5	IEN-GPIO4	IEN-GPIO3	IEN-GPIO2	IEN-GPIO1	IEN-GPIO0

rw

7	6	5	4	3	2	1	0
OEN-GPIO7	OEN-GPIO6	OEN-GPIO5	OEN-GPIO4	OEN-GPIO3	OEN-GPIO2	OEN-GPIO1	OEN-GPIO0

rw

Field	Bits	Type	Description
<b>IEN-GPIO7</b>	15	rw	<b>Input Enable GPIO7</b> Enables input for programmable pin GPIO7. 0 Input driver disabled. The GPIO7 bit in register SRGPIO is always one. 1 Input driver enabled. The GPIO7 bit in register SRGPIO shows the current value of pin GPIO7.
<b>IEN-GPIO6</b>	14	rw	<b>Input Enable GPIO6</b> Enables input for programmable pin GPIO6. 0 Input driver disabled. The GPIO6 bit in register SRGPIO is always one. 1 Input driver enabled. The GPIO6 bit in register SRGPIO shows the current value of pin GPIO6.
<b>IEN-GPIO5</b>	13	rw	<b>Input Enable GPIO5</b> Enables input for programmable pin GPIO5. 0 Input driver disabled. The GPIO5 bit in register SRGPIO is always one. 1 Input driver enabled. The GPIO5 bit in register SRGPIO shows the current value of pin GPIO5.
<b>IEN-GPIO4</b>	12	rw	<b>Input Enable GPIO4</b> Enables input for programmable pin GPIO4. 0 Input driver disabled. The GPIO4 bit in register SRGPIO is always one. 1 Input driver enabled. The GPIO4 bit in register SRGPIO shows the current value of pin GPIO4.

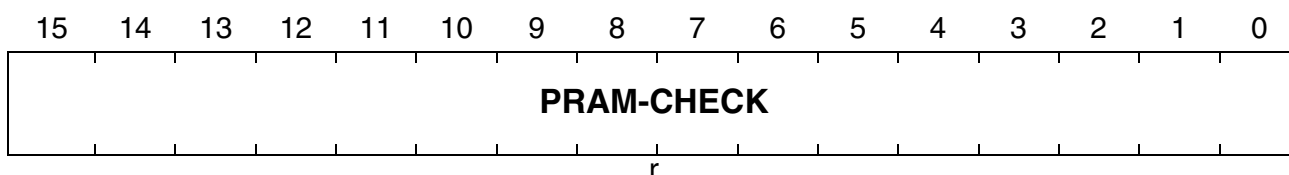
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Field	Bits	Type	Description
<b>IEN-GPIO3</b>	11	rw	<b>Input Enable GPIO3</b> Enable input for programmable pin GPIO3. 0 Input driver disabled. The GPIO3 bit in register SRGPIO is always one. 1 Input driver enabled. The GPIO3 bit in register SRGPIO shows the current value of pin GPIO3.
<b>IEN-GPIO2</b>	10	rw	<b>Input Enable GPIO2</b> Enables input for programmable pin GPIO2. 0 Input driver disabled. The GPIO2 bit in register SRGPIO is always one. 1 Input driver enabled. The GPIO2 bit in register SRGPIO shows the current value of pin GPIO2.
<b>IEN-GPIO1</b>	9	rw	<b>Input Enable GPIO1</b> Enables input for programmable pin GPIO1. 0 Input driver disabled. The GPIO1 bit in register SRGPIO is always one. 1 Input driver enabled. The GPIO1 bit in register SRGPIO shows the current value of pin GPIO1.
<b>IEN-GPIO0</b>	8	rw	<b>Input Enable GPIO0</b> Enables input for programmable pin GPIO0. 0 Input driver disabled. The GPIO0 bit in register SRGPIO is always one. 1 Input driver enabled. The GPIO0 bit in register SRGPIO shows the current value of pin GPIO0.
<b>OEN-GPIO7</b>	7	rw	<b>Output Enable GPIO7</b> Enables output driver for programmable pin GPIO7. 0 Output driver disabled 1 Output driver enabled
<b>OEN-GPIO6</b>	6	rw	<b>Output Enable GPIO6</b> Enables output driver for programmable pin GPIO6. 0 Output driver disabled 1 Output driver enabled
<b>OEN-GPIO5</b>	5	rw	<b>Output Enable GPIO5</b> Enables output driver for programmable pin GPIO5. 0 Output driver disabled 1 Output driver enabled

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Field	Bits	Type	Description
<b>OEN-GPIO4</b>	4	rw	<b>Output Enable GPIO4</b> Enables output driver for programmable pin GPIO4. 0     Output driver disabled 1     Output driver enabled
<b>OEN-GPIO3</b>	3	rw	<b>Output Enable GPIO3</b> Enables output driver for programmable pin GPIO3. 0     Output driver disabled 1     Output driver enabled
<b>OEN-GPIO2</b>	2	rw	<b>Output Enable GPIO2</b> Enables output driver for programmable pin GPIO2. 0     Output driver disabled 1     Output driver enabled
<b>OEN-GPIO1</b>	1	rw	<b>Output Enable GPIO1</b> Enables output driver for programmable pin GPIO1. 0     Output driver disabled 1     Output driver enabled
<b>OEN-GPIO0</b>	0	rw	<b>Output Enable GPIO0</b> Enables output driver for programmable pin GPIO0. 0     Output driver disabled 1     Output driver enabled

*Note: If input and output drivers are enabled, the written output value can be read back.*

**CONFIDENTIAL**
**PHICKR (Allocation D)**
**PHI PRAM Checksum Register**
**(49<sub>H</sub>)**
**Reset Value: 0000<sub>H</sub>**


Field	Bits	Type	Description
PRAM-CHECK	[15:0]	r	PHI PRAM Checksum

As an option, the PHI software can be downloaded to a Program RAM. To verify the download and to check the RAM during operation a checksum for the RAM based PHI software is calculated. The checksum calculation is executed once after the PHI Program RAM download. The Checksum calculation during normal operation can be started by issuing the wCHECKSUM command. The checksum calculation takes 15 frames (1,875 ms).

The checksum is generated in software by a 16-bit MISR algorithm. The used polynomial is:  $x^{16}+x^5+x^3+x^2+1$ .

The algorithm of the checksum generation is:

```

For (ram_adr=0; ram_adr < max; ram_adr++) {
ram_dat = ram[ram_adr];
if (csum[15:0] & 0x8000)
csum = csum<<1 XOR ram_dat XOR 0x002D;
else
csum = csum<<1 XOR ram_dat;
}

```

*Note: With IOP commands the checksum in this register can only be read after a successful EDSP firmware download and the short command wSTEDSP (start EDSP).*

**CONFIDENTIAL**
**7.5 Registers Read with Short Commands (PHI, ALM and EDSP)**

*Note: An explanation of the register formatting used on the following pages is given in [“Register Description Format” on Page 251](#)*

**7.5.1 Interrupt Register**
**IR (Allocation D)**
**Interrupt Status Register**
**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
ISRE7	ISRE6	ISRE5	ISRE4	ISR3	ISR2	ISR1	ISR0
r							
7	6	5	4	3	2	1	0
RDYQ	0	0	RESET	0	GPIO	MBX-EVT	HW-STAT
r							

*Note:*

- 1. If one of these bits is set to 1, the INTQ line is drawn to low level (except RDYQ-bit).*
- 2. The bits of the IR cannot be masked. All bits of the status registers (which contain the sources for the indicated interrupt) can be masked.*
- 3. If bits of the status registers are masked no interrupt will be generated and the corresponding bit in the IR will not be set!*
- 4. The RESET bit cannot be masked, it will always be set after a reset and the INTQ line will always be activated.*

Field	Bits	Type	Description
ISRE7	15	r	<b>Interrupt Status Channel 7 [M-V-CPE]</b> Interrupt status bit for EDSP status register for channel 7. This bit will be set, if at least one bit of the corresponding EDSP status register SRE1 or SRE2 has changed. It will be cleared by reading the corresponding EDSP interrupt status registers I-SRE1 and I-SRE2. 0 No interrupt detected 1 Interrupt detected in corresponding register SRE1 and/or SRE2.

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Field	Bits	Type	Description
<b>ISRE6</b>	14	r	<b>Interrupt Status Channel 6 [M-V-CPE]</b> Interrupt status bit for EDSP status register for channel 6. This bit will be set, if at least one bit of the corresponding EDSP status register SRE1 or SRE2 has changed. It will be cleared by reading the corresponding EDSP interrupt status registers I-SRE1 and I-SRE2. 0 No interrupt detected 1 Interrupt detected in corresponding register SRE1 and/or SRE2.
<b>ISRE5</b>	13	r	<b>Interrupt Status Channel 5 [M-V-CPE]</b> Interrupt status bit for EDSP status register for channel 5. This bit will be set, if at least one bit of the corresponding EDSP status register SRE1 or SRE2 has changed. It will be cleared by reading the corresponding EDSP interrupt status registers I-SRE1 and I-SRE2. 0 No interrupt detected 1 Interrupt detected in corresponding register SRE1 and/or SRE2.
<b>ISRE4</b>	12	r	<b>Interrupt Status Channel 4 [M-V-CPE]</b> Interrupt status bit for EDSP status register for channel 4. This bit will be set, if at least one bit of the corresponding EDSP status register SRE1 or SRE2 has changed. It will be cleared by reading the corresponding EDSP interrupt status registers I-SRE1 and I-SRE2. 0 No interrupt detected 1 Interrupt detected in corresponding register SRE1 and/or SRE2.



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Field	Bits	Type	Description
ISR3	11	r	<p><b>Interrupt Status Channel 3</b></p> <p><i>Note: in case of VINETIC®-4S no SRE1/2 register exists. Nevertheless, because of compatibility reasons within the VINETIC-family, four words have to be read</i></p> <p>Interrupt status bit for ALM and EDSP ([M-V-C, CPE]) status register for channel 3. This bit will be set, if at least one bit of the corresponding status registers SRE1, SRE2, SRS1 or SRS2 has changed. It will be cleared by reading the corresponding interrupt status registers I-SRE1, I-SRE2, I-SRS1 and I-SRS2.</p> <p>0 No interrupt detected 1 Interrupt detected in register SRE1 and/or SRE2 and/or SRS1 and/or SRS2.</p>
ISR2	10	r	<p><b>Interrupt Status Channel 2</b></p> <p><i>Note: in case of VINETIC®-4S no SRE1/2 register exists. Nevertheless, because of compatibility reasons within the VINETIC-family, four words have to be read</i></p> <p>Interrupt status bit for EDSP status register for channel 2. This bit will be set, if at least one bit of the corresponding status registers SRE1, SRE2, SRS1 or SRS2 has changed. It will be cleared by reading the corresponding interrupt status registers I-SRE1, I-SRE2, I-SRS1 and I-SRS2.</p> <p>0 No interrupt detected 1 Interrupt detected in register SRE1 and/or SRE2 and/or SRS1 and/or SRS2.</p>

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Field	Bits	Type	Description
ISR1	9	r	<b>Interrupt Status Channel 1</b> <i>Note: in case of VINETIC®-4S no SRE1/2 register exists. Nevertheless, because of compatibility reasons within the VINETIC-family, four words have to be read</i>  Interrupt status bit for EDSP status register for channel 1. This bit will be set, if at least one bit of the corresponding status registers SRE1, SRE2, SRS1 or SRS2 has changed. It will be cleared by reading the corresponding interrupt status registers I-SRE1, I-SRE2, I-SRS1 and I-SRS2. 0 No interrupt detected 1 Interrupt detected in register SRE1 and/or SRE2 and/or SRS1 and/or SRS2.
ISR0	8	r	<b>Interrupt Status Channel 0</b> <i>Note: in case of VINETIC®-4S no SRE1/2 register exists. Nevertheless, because of compatibility reasons within the VINETIC-family, four words have to be read</i>  Interrupt status bit for EDSP status register for channel 0. This bit will be set, if at least one bit of the corresponding status registers SRE1, SRE2, SRS1 or SRS2 has changed. It will be cleared by reading the corresponding interrupt status registers I-SRE1, I-SRE2, I-SRS1 and I-SRS2. 0 No interrupt detected 1 Interrupt detected in register SRE1 and/or SRE2 and/or SRS1 and/or SRS2.
RDYQ	7	r	<b>RDYQ Status</b> Shows the status of the RDYQ pin. A change of this bit doesn't affect the INTQ line. <i>Note: This bit reflects the status of the RDYQ pin only in case of a fast read (Direct IR Access (DIA)) via address 1100, otherwise it is 0.</i>  0 RDYQ <sup>-</sup> pin low. 1 RDYQ pin high.

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Field	Bits	Type	Description
<b>RESET</b>	4	r	<b>Reset</b> Indicates a hardware reset of the VINETIC®-x. It will be cleared by reading the IR register. 0 No reset occurred 1 Reset occurred
<b>GPIO</b>	2	r	<b>GPIO Change</b> This bit is set if at least one GPIOx bit of the SRGPIO register has changed. It is cleared by reading the I-SRGPIO register. 0 No GPIO change 1 GPIO change
<b>MBX-EVT</b>	1	r	<b>Mailbox Event</b> <i>Note: in case of VINETIC®-4S no BXSRI register exists. Nevertheless, because of compatibility reasons within the VINETIC-family, both words have to be read</i> This bit is set, if at least one of the BXSRI or BXSRII register bits has changed. It is cleared by reading the I-BXSRI and I-BXSRII register. 0 No mailbox event 1 Mailbox event
<b>HW-STAT</b>	0	r	<b>Hardware Status</b> <i>Note: in case of VINETIC®-4S no HWSRII register exists. Nevertheless, because of compatibility reasons within the VINETIC-family, both words have to be read</i> This bit is set if at least one of the HWSRI or HWSRII register bit has changed. It is cleared by reading I-HWSRI and I-HWSRII registers. 0 No hardware fail 1 Hardware fail

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**7.5.2 Status Register**
**SRE1 (Allocation R)**
**Status Register for EDSP Interrupts 1 [M-V-C, CPE]**
**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
DTMFR-DT	DTMFR-PDT	DTMFR-DTC				UTD1-OK	UTD2-OK
r							
7	6	5	4	3	2	1	0
CPT	CIDR-OF	DTMFG-BUF	DTMFG-REQ	DTMFG-ACT/ UTG_ACT	CIS-BUF	CIS-REQ	CIS-ACT
r							

Field	Bits	Type	Description
<b>DTMFR-DT</b>	15	r	<b>DTMF Receiver Key Detect</b> Valid DTMF key detected by the DTMF receiver. 0 No valid DTMF key was detected by the DTMF receiver. 1 A valid DTMF key was detected by the DTMF receiver.
<b>DTMFR-PDT</b>	14	r	<b>DTMF Receiver Probably Key Detect</b> Probably DTMF key detected by the DTMF receiver. 0 No DTMF key was detected by the DTMF receiver. 1 DTMF key was probably detected by the DTMF receiver.

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Field	Bits	Type	Description
DTMFR-DTC	[13:10]	r	<b>DTMF Receiver Key Decode</b>
			Valid DTMF keys decoded by the DTMF receiver.
			DG-KEY      DIGIT $f_{LOW}$ [Hz] $f_{HIGH}$ [Hz]
			0000      0      941      1336
			0001      1      697      1209
			0010      2      697      1336
			0011      3      697      1477
			0100      4      770      1209
			0101      5      770      1336
			0110      6      770      1477
			0111      7      852      1209
			1000      8      852      1336
			1001      9      852      1477
			1010      *      941      1209
			1011      #      941      1477
			1100      A      697      1633
			1101      B      770      1633
			1110      C      852      1633
			1111      D      941      1633
			<i>Note: The field DTMFR-DTC is updated, when the bit DTMFR-DT or DTMFR-PDT is set. If key codes are transmitted with the highest possible data rate, the host has to read the detected DTMF sign within 50 ms (40 ms for the pause and 10 ms for the early detection) after the DTMFR-DT or DTMFR-PDT has been set. If the host will not meet these timing constraints the actual key value stored in DTMFR-DTC may be overwritten by the following key.</i>

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Field	Bits	Type	Description
UTD1-OK	9	r	<p><b>Universal Tone Detection 1</b> (such as Fax/Modem tones). The interpretation of this status bit is dependent on the MD bit set with the <b>EOP-Command “UTD 1”</b>.  <b>If (MD = 00<sub>B</sub>) - Universal Tone Detect</b>  0 no tone detected.  1 Universal tone or tone end detected.  <b>If (MD = 01<sub>B</sub>) - V.18A Detect</b>  0 no V.18A detected.  1 V.18A or V.18A end detected.  <b>If (MD = 10<sub>B</sub>) - Signal Level Detect</b>  0 no Signal level detected.  1 Signal level or gap detected  <i>Note: MD can only be in the range of 00<sub>B</sub>..10<sub>B</sub>. A value of 11<sub>B</sub> are not allowed.</i></p>
UTD2-OK	8	r	<p><b>Universal Tone Detection 2</b> (such as Fax/Modem tones). The interpretation of this status bit is dependent on the MD bit set with the <b>EOP-Command “UTD 1”</b>.  <b>If (MD = 00<sub>B</sub>) - Universal Tone Detect</b>  0 no tone detected.  1 Universal tone or tone end detected.  <b>If (MD = 01<sub>B</sub>) - V.18A Detect</b>  0 no V.18A detected.  1 V.18A or V.18A end detected.  <b>If (MD = 10<sub>B</sub>) - Signal Level Detect</b>  0 no Signal level detected.  1 Signal level or gap detected  <i>Note: MD can only be in the range of 00<sub>B</sub>..10<sub>B</sub>. A value of 11<sub>B</sub> are not allowed.</i></p>
CPT	7	r	<p><b>Calling Progress Tone</b>  0 No CPT detected.  1 CPT detected.</p>

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Field	Bits	Type	Description
<b>CID-R</b>	6	r	<b>CID Receiver Overflow</b> This bit is set, if the CID Receiver could not send the last received byte or bytes per data packet to the host and therefore the data packet was discarded. This bit is cleared by an initialization or deactivation of the CID Receiver. 0 No overflow detected. 1 CID-Receiver Overflow detected.
<b>DTMFG-BUF</b>	5	r	<b>DTMF Generator Buffer</b> Underflow of the DTMF generator input buffer. The DTMF/AT generator has completely sent all signs. 0 No DTMF input buffer underflow. 1 DTMF input buffer underflow. <i>Note: DTMFG-BUF is only set if bit ET= 0 and bit MOD = 1 (see Preliminary User's Manual - EDSP Firmware Description EOP-Command "DTMF/AT Generator").</i>
<b>DTMFG-REQ</b>	4	r	<b>DTMF Generator Request</b> The DTMF/AT generator is sending the last two signs and requests a new sign. 0 No sign requested. 1 DTMF/AT generator is sending the last two signs and requests a new sign. <i>Note: DTMFG-REQ is only set if bit ET= 0 and bit MOD = 1 (see Preliminary User's Manual - EDSP Firmware Description EOP-Command "DTMF/AT Generator").</i>
<b>DTMFG-ACT</b>	3	r	<b>DTMF Generator Active</b> DTMF/AT generator is active. This is a status bit only. 0 DTMF/AT generator is not active. 1 DTMF/AT generator is active. <i>Note: Bit UTG-ACT and DTMFG-ACT are using the same bit position in SRE1 (overlaid).            The DTMF / AT Generator can not be used simultaneously with the universal tone generator.            The host must ensure that a DTMF/AT Generator and an UTG with the same resource number are not active at the same time!</i>

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Field	Bits	Type	Description
UTG-ACT	3	r	<b>Universal Tone Generator - UTG Active</b> UTG is active. This is a status bit only. 0     UTG is not active. 1     UTG is active.
CIS-BUF	2	r	<b>Caller ID Input Buffer Underflow</b> The generator has completely sent all data and inserts stop bits. 0     Data buffer for Caller ID generation is filled. 1     Data buffer for Caller ID generation is empty (underflow).
CIS-REQ	1	r	<b>Caller ID Request</b> Caller ID data buffer requests more data to transmit, when the amount of data stored in the buffer is less than the buffer request size. 0     Caller ID data buffer requests no data. 1     Caller ID data request.
CIS-ACT	0	r	<b>Caller ID Generator Active</b> Indicates activity of the Caller ID Generator. 0     Caller ID generator is not active. 1     Caller ID generator is active.

*Note: The bits supported within SRE1 and SRE2 are dependent on the EDSP firmware variant and version loaded. For details refer to the Firmware Overview EDSP.*



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**SRE2 (Allocation R)**
**Status Register for EDSP Interrupts 2 [M-V-CPE]**
**Reset Value: 0000<sub>H</sub>**

15		14		13		12		11		10		9		8	
ATD1-DT		ATD1-NPR				ATD1-AM		ATD2-DT		ATD2-NPR				ATD2-AM	
r															
7		6		5		4		3		2		1		0	
EPOU-STAT		ETU-OF		PVPU-OF/ FDP-ERR		VPOU-STAT		VPOU-JBL		VPOU-JBH		DEC-ERR		DEC-CHG/ FDP-REQ	
r															

Field	Bits	Type	Description
ATD1-DT	15	r	<b>ATD1 Detect</b> The interpretation of this status bit is dependent on the MD bit set with EOP Command "ATD 1" (see <i>Preliminary User's Manual - EDSP Firmware Description</i> ). <b>If (MD = 00<sub>B</sub> or MD = 01<sub>B</sub>) - Answering Tone Detect</b> 0 Answering tone end detected 1 Answering tone detected <b>If (MD = 10<sub>B</sub>) - DIS Signal Detect</b> 0 No detection (Bit is set to 0 when DIS Signal Detection is switched off) 1 DIS signal detected <b>If (MD = 11<sub>B</sub>) - Signal Level Detect</b> 0 gap detected (broadband energy below threshold) 1 Signal level detected (broadband energy above threshold)
ATD1-NPR	[14:13]	r	<b>ATD1 Phase Reversals</b> Number of phase reversal if (MD = 00 <sub>B</sub> or MD = 01 <sub>B</sub> ) 00 No phase reversal 01 1 phase reversal 10 2 phase reversals 11 3 phase reversals
ATD1-AM	12	r	<b>ATD1 Amplitude Modulation</b> Amplitude modulation detection for ADT1 if (MD = 01 <sub>B</sub> ) 0 No detection 1 Amplitude modulation detected

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Field	Bits	Type	Description
<b>ATD2-DT</b>	11	r	<b>ATD2 Detect</b> The interpretation of this status bit is dependent on the MD bit set with EOP Command "ATD 2" (see <i>Preliminary User's Manual - EDSP Firmware Description</i> ). <b>If (MD = 00<sub>B</sub> or MD = 01<sub>B</sub>) - Answering Tone Detect</b> 0 Answering tone end detected 1 Answering tone detected <b>If (MD = 10<sub>B</sub>) - DIS Signal Detect</b> 0 No detection (Bit is set to 0 when DIS Signal Detection is switched off) 1 DIS signal detected <b>If (MD = 11<sub>B</sub>) - Signal Level Detect</b> 0 gap detected (broadband energy below threshold) 1 Signal level detected (broadband energy above threshold)
<b>ATD2-NPR</b>	[10:9]	r	<b>ATD2 Phase Reversals</b> Number of phase reversal if (MD = 00 <sub>B</sub> or MD = 01 <sub>B</sub> ) 00 No phase reversal 01 1 phase reversal 10 2 phase reversals 11 3 phase reversals
<b>ATD2-AM</b>	8	r	<b>ATD2 Amplitude Modulation</b> Amplitude modulation detection for ADT1 if (MD = 01 <sub>B</sub> ) 0 No detection 1 Amplitude modulation detected
<b>EPOU-STAT</b>	7	r	<b>Event Play Out Unit Status</b> The Event Play Out Unit has executed a re synchronization or has discarded an event packet, which means it has detected an invalid, late or early event. The host can read the event statistic via the EOP-command "Signaling Channel Event Statistic". The bit will be cleared automatically when the host reads the statistic.

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Field	Bits	Type	Description
<b>ETU-OF</b>	6	r	<b>Event Transmit Unit Overflow</b> The event transmit unit couldn't send the event to the data manager. The event was discarded. 0 No change. 1 Event transmit unit overflow. <i>Note: This bit can be reset by reading the EOP-Command "Status Error Acknowledge" (see Preliminary User's Manual - EDSP Firmware Description).</i>
<b>PVPU-OF</b>	5	r	<b>Packetized Voice Protocol Unit Overflow</b> Overflow of the data manager. Indicates that the packetized voice protocol unit could not write the encoder output packet into the data manager. The data packet was discarded. This could occur if the controller doesn't read the data packets and therefore the data mailbox as well as the data manager is totally filled. 0 No overflow 1 Overflow <i>Note: Coder Channel Speech Compression and FAX Data Pump can not be active at the same time for one and the same channel. Depending on which module is active for a channel, this bit positions indicates either the status of the Coder Channel Speech Compression (PVPU-OF) or the status of the FAX Data Pump (FDP-ERR).  This bit can be reset by reading the EOP-Command "Status Error Acknowledge".(see Preliminary User's Manual - EDSP Firmware Description).</i>
<b>FDP-ERR</b>	5	r	<b>FAX Data Pump Error</b> This bit indicates an error situation of the fax data pump to the host. If this bit is set the host should deactivate the fax data pump and stop the fax transmission. 0 No error 1 Error <i>Note: The bit is cleared in the case of an activation of the modulator or demodulator respectively or in the case of a channel deactivation.</i>

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Field	Bits	Type	Description
<b>VPOU-STAT</b>	4	r	<b>Voice Play Out Unit Status</b> Voice Play Out Unit has modified the coder channel jitter buffer statistic. A voice packet has been received which was invalid or was classified as late or early or a resynchronization has been carried out.  <i>Note: This bit can be cleared via the EOP command "Coder Channel JB Statistics" (see Preliminary User's Manual - EDSP Firmware Description).</i>
<b>VPOU-JBL</b>	3	r	<b>Voice Play Out Unit Jitter Buffer Low</b> Jitter buffer low limit has been reached. This bit is set if the measured packet play out delay drops below the lower limit (see <i>Preliminary User's Manual - EDSP Firmware Description</i> EOP-command "Coder Channel JB Configuration", MIN_JB_POD). Otherwise the bit will be cleared. The bit VPOU-JBL is supported only in fixed jitter buffer mode (ADAP == 0). 0 Low limit not reached 1 Low limit reached
<b>VPOU-JBH</b>	2	r	<b>Voice Play Out Unit Jitter Buffer High</b> Jitter buffer high limit has been reached. This bit is set if the measured packet play out delay exceeds the initial limit (see <i>Preliminary User's Manual - EDSP Firmware Description</i> EOP-Command "Coder Channel JB Configuration", INIT_JB_POD). Otherwise the bit will be cleared. The bit VPOU-JBH is supported only in fixed jitter buffer mode (ADAP == 0). 0 High limit not reached 1 High limit reached
<b>Res</b>	1	r	<b>Reserved</b>

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Field	Bits	Type	Description
<b>DEC-CHG</b>	0	r	<p><b>Decoder Change</b> The decoder type or the packet time has been changed.</p> <p>0 No change 1 Change</p> <p><i>Note:</i></p> <ol style="list-style-type: none"> <li><i>Coder Channel Speech Compression and FAX Data Pump can not be active at the same time for one and the same channel. Depending on which module is active for a channel, this bit positions indicates either the status of the Coder Channel Speech Compression (DEC-CHG) or the status of the FAX Data Pump (FDP-REQ)</i></li> <li><i>This bit can be cleared by the EOP-Command “Coder Channel Decoder Status” (see Preliminary User’s Manual - EDSP Firmware Description).</i></li> </ol>
<b>FDP-REQ</b>	0	r	<p><b>FAX Data Pump Data Request</b> This bit is set if the modulator of the FAX data pump requests new data.</p> <p>0 No data requested 1 Data requested</p> <p><i>Note: This bit is cleared both in case of a modulator or demodulator activation and in case of the deactivation of the fax data pump.</i></p>

*Note: The bits supported within SRE1 and SRE2 are dependent on the EDSP firmware variant and version loaded. For details refer to the Firmware Overview EDSP.*

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## SRS1 (Allocation C)

### Status Register for

### Analog-Line-Module Interrupts 1

Reset Value: 0000<sub>H</sub>

15	14	13	12	11	10	9	8
AUTO-MET-DONE	RAMP-READY	HOOK	GNDK	GNKP	GNDKH	ICON	VTRLIM
r							
7	6	5	4	3	2	1	0
0	LM-THRES	LM-OK	DU-IO				
r							

Field	Bits	Type	Description
AUTO-MET-DONE	15	r	<p><b>Auto Metering Done</b></p> <p>Indicates the end of a metering pulse which has been generated by the auto metering function.</p> <p>The auto metering function will set AUTO-MET-DONE when the metering pulse time (<math>t_{pulse}</math>) and the consecutive pause time (<math>t_{pause}</math>) have passed.</p> <p>Auto metering can be terminated by setting bit AUTO-MET-EN to 0 or by a mode change to another mode than an Active mode. In the later case the AUTO-MET-DONE bit is not set.</p> <p>0 Auto Metering function has not terminated.</p> <p>1 Auto Metering function has terminated.</p> <p><i>Note: AUTO-MET-DONE is reset to 0 when a new auto metering pulse is started or the auto metering function is disabled.</i></p>
RAMP-READY	14	r	<p><b>Ramp Ready</b></p> <p>Indication whether the ramp generator has finished.</p> <p>Upon a new start of the ramp generator, the bit is set to 0.</p> <p>0 Ramp generator active.</p> <p>1 Ramp generator not active.</p>

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Field	Bits	Type	Description
<b>HOOK</b>	13	r	<b>Hook</b> Indicates on-hook or off-hook for the loop in all operating modes (via the ITx pin); filtered by the DUP (Data Upstream Persistence) counter. Indicates ground start in case of ground start mode is selected. 0 On-hook. 1 Off-hook detected.
<b>GNDK</b>	12	r	<b>Ground Key</b> Indicates ground key information (threshold 17 mA) in all active modes via ILx pin; filtered for AC suppression by the DUP-GNDK counter. 0 No ground key indicated. 1 Ground key indication; longitudinal current (threshold 17 mA) detected.
<b>GNKP</b>	11	r	<b>Ground Key Polarity</b> Indicates polarity of the ground key threshold level; This bit can be used to obtain information about interference voltage influence. 0 Negative ground key threshold level active. 1 Positive ground key threshold level active.
<b>GNDKH</b>	10	r	<b>Ground Key High</b> Indicates ground key information (threshold 40 mA) in all active modes via ILx pin. 0 No ground key high indicated. 1 Ground key high indication; longitudinal current (threshold 40 mA) detected.
<b>ICON</b>	9	r	<b>Constant Current Feeding</b> Indicates constant current feeding method; filtered by DUP-IO counter. 0 Resistive or constant voltage feeding. 1 Constant current feeding.

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Field	Bits	Type	Description
<b>VTRLIM</b>	8	r	<b>Voltage Threshold Limit</b> Indication whether a programmed voltage threshold for the TIP/RING voltage is exceeded; filtered by the DUP-IO counter. The voltage threshold for the TIP/RING voltage is set in CRAM (calculated with VINETICOS DC Control Parameter Tip Ring-Voltage Threshold, Detection). 0 Voltage at Tip/Ring is below the limit. 1 Voltage at Tip/Ring is above the limit.
<b>LM-THRES</b>	6	r	<b>Level Metering Threshold</b> Indication whether the level metering result is above or below the threshold set by the CRAM coefficients. 0 Level metering result is below threshold. 1 Level metering result is above threshold.
<b>LM-OK</b>	5	r	<b>Level Metering OK</b> Indication if level metering sequence is finished. 0 Level metering result not ready. 1 Level metering result ready.
<b>DU-IO</b>	[4:0]	r	<b>Data Upstream IO Pins</b> Data on I/O pins 0 to 4; filtered by DUP-IO counter.



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**SRS2 (Allocation C)**
**Status Register for**
**Analog-Line-Module Interrupts 2**
**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0

r

7	6	5	4	3	2	1	0
0	0	0	0	OTEMP	CS-FAIL-CRAM	CS-FAIL-DSP	CS-FAIL-DCCTL

r

Field	Bits	Type	Description
<b>OTEMP</b>	3	r	<b>Overtemperature</b> Thermal overload warning from the SLIC line drivers. 0 Temperature at SLIC is below the limit. 1 Temperature at SLIC is above the limit. In case of bit PDOT-DIS = 0 (register BCR2) the affected channel is switched automatically into PDH mode and OTEMP is hold at 1 until the channel is set to PDH by a CIOP/CIDD command.
<b>CS-FAIL-CRAM</b>	2	r	<b>CRAM Checksum Failure</b> 0 No failure 1 Failure <i>Note: This bit shows valid information only after a DCCTL micro program download and activation of the downloaded program (BCR1:PRAM-DCC = 1). If this is not the cases this bit should be masked!</i>

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Field	Bits	Type	Description
<b>CS-FAIL-DSP</b>	1	r	<p><b>DSP PRAM Checksum Failure</b></p> <p>Failure of the Analog-Line-Module DSP PRAM checksum. In case of a checksum error always the CS-FAIL-DSP bit of both channels of the affected Analog-Line-Module will be set.</p> <p>0      No failure 1      Failure</p> <p><i>Note: This bit shows valid information only after a DCCTL micro program download and activation of the downloaded program (BCR1:PRAM-DCC = 1). If this is not the cases this bit should be masked!</i></p>
<b>CS-FAIL-DCCTL</b>	0	r	<p><b>DCCTL PRAM Checksum Failure</b></p> <p>Failure of the Analog-Line-Module DCCTL PRAM checksum. In case of a checksum error always the CS-FAIL-DCCTL bit of both channels of the affected Analog-Line-Module will be set.</p> <p>0      No failure 1      Failure</p>

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**HWSR1 (Allocation D)**  
**Hardware Status Register 1**
**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
0	0	0	0	SYNC-FAIL	Res	TXB-CRASH	TXA-CRASH
r							
7	6	5	4	3	2	1	0
EDSP-WD-FAIL	0	0	0	MCLK-FAIL	WOKE-UP	0	HW-ERR
r							

Field	Bits	Type	Description
<b>SYNC-FAIL</b>	11	r	<b>Synchronization Failure</b> Checks if multiples of MCLK cycles fit in a FSC frame (PLL divider mismatch). Resynchronization of the PCM interface can be done with the short command “Re-synchronize PCM clock” (see <a href="#">Page 55</a> ). 0 $f_{MCLK}/f_{FSC} = \text{OK}$ 1 $f_{MCLK}/f_{FSC} = \text{invalid}$
<b>Res</b>	10		<b>Reserved</b>
<b>TXB-CRASH</b>	9	r	<b>Transmit Highway B Crash</b> Indication of multiple access of PCM transmit time slot of highway B. 0 Normal operation. 1 PCM transmit time slot of highway B is accessed multiple.
<b>TXA-CRASH</b>	8	r	<b>Transmit Highway A Crash</b> Indication of multiple access of PCM transmit time slot of highway A. 0 Normal operation. 1 PCM transmit time slot of highway A is accessed multiple.

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Field	Bits	Type	Description
<b>EDSP-WD-FAIL</b>	7	r	<b>EDSP Watchdog Failure [M-V-CPE]</b> Indication of EDSP failure after watchdog activation. This bit will be set, if the watchdog timer hasn't be reset timely. It is cleared by disabling the watchdog. 0 EDSP normal operation. 1 EDSP failure. The EDSP must be downloaded and/or restarted from the host.
<b>MCLK-FAIL</b>	3	r	<b>Masterclock Failure</b> The PLL clock is not locked. 0 Synchronization OK. 1 Synchronization failure.
<b>WOKE-UP</b>	2	r	<b>Woke Up</b> Indicates that the VINETIC®-x is ready for programming after deep sleep. 0 Normal operation. 1 VINETIC®-x is ready for programming.
<b>HW-ERR</b>	0	r	<b>Hardware Error [M-V-CPE]</b> Internal EDSP hardware error. This bit will be set if an EDSP internal hardware error has been detected (e.g. bus conflict). This leads to a software reset. 0 No error detected 1 Error detected

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**HWSR2 (Allocation D)**
**Hardware Status Register 2 [M-V-CPE]**
**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	DL-RDY
r							
7	6	5	4	3	2	1	0
0	0	0	0	0	CRC-RDY	CRC-ERR	EDSP-MIPS-OL
r							

Field	Bits	Type	Description
DL-RDY	8	r	<b>EDSP Download Ready</b> This bit will be set, after a download has been completed and the VINETIC®-x is ready for the short command wSTEDSP (Start EDSP see <a href="#">Table 5</a> ). DL-RDY will be reset to 0 after 500µs after the Short Command wLEMP (Load EDSP Micro Program) has been sent. It will be also cleared by sending the short command wSTEDSP (Start EDSP see <a href="#">Table 5</a> ). 0 Download not ready. 1 Download ready.
CRC-RDY	2	r	<b>EDSP Reference CRC Value Calculation Ready<sup>1)</sup></b> When the EDSP has calculated the reference CRC value the status bit CRC-RDY is set. This indicates to the host that from that point on a modification within the program will be detected by the background CRC check. If the host wants, it could double check the downloaded program after the EDSP has set the CRC-RDY bit. This would ensure, that between download and end of CRC calculation the program memory has not changed. The CRC-RDY status bit is only cleared, when the reference CRC value is not valid within the EDSP reset function 0 CRC calculation not ready. 1 CRC calculation ready.

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Field	Bits	Type	Description
<b>CRC-ERR</b>	1	r	<b>EDSP Error Background CRC check</b> If the EDSP has detected a mismatch between the reference and the actual calculated CRC value the status bit CRC-ERR is set to 1. This indicates to the host, that a program and/or data memory modification was detected and therefore the EDSP program execution should be stopped and a new download has to be made. The CRC-ERR status bit is automatically cleared within the EDSP reset function. 0 No CRC error detected. 1 CRC error detected.
<b>EDSP-MIPS-OL</b>	0	r	<b>EDSP MIPS Overload [M-V-CPE]</b> MIPS overload, indicates in case of speech compression, that the start of the encoder or decoder was delayed due to a MIPS overload. In conjunction with the fax data pump bit EDSP-MIPS-OL indicates that due to an MIPS overload situation the start of the modulator or demodulator was delayed. This bit can be cleared by reading the EOP-Command "Mips Overload Acknowledge" (see <i>Preliminary User's Manual - EDSP Firmware Description</i> ). 0 EDSP normal operation. 1 EDSP failure. <i>Note: There is only one EDSP-MIPS-OL status bit available for all channels!</i>

<sup>1)</sup> The CRC background check is only supported in connection with VINETIC® Idle Mode

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**BXSR1 (Allocation D)**

**Mailbox Status Register 1 [M-V-CPE]**

**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	<b>CERR</b>

r

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

r

Field	Bits	Type	Description
<b>CERR</b>	8	r	<b>Command Error</b> The EDSP detected a wrong command. The command in-box will be cleared and the EDSP waits for the EOP-Command "CERR Acknowledge" (see <i>Preliminary User's Manual - EDSP Firmware Description</i> ). 0 No error 1 Error

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**BXSR2 (Allocation D)**
**Mailbox Status Register 2**
**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
r							
7	6	5	4	3	2	1	0
0	0	HOST-ERR	POBX-DATA	COBX-DATA	PIBX-OF	CIBX-OF	MBX-EMPTY
r							

Field	Bits	Type	Description
<b>HOST-ERR</b>	5	r	<b>Host Error</b> Detection of an error during interface command decoding. The programming sequence is aborted and the wrong command has been ignored. This bit will be cleared if the error condition is acknowledged with the short command wPHIERR. 0 Normal operation 1 Detection of an error during interface command decoding
<b>POBX-DATA</b>	4	r	<b>Packet Out-Box Data [M-V-CPE]</b> Data in packet out-box ready for reading. This bit is set if the EDSP has transferred a packet or a signaling information to the packet out-box. 0 No packet(s) in the packet out-box 1 Packet(s) in the packet out-box
<b>COBX-DATA</b>	3	r	<b>Command Out-Box Data</b> Data in command out-box. This bit is set if the EDSP has transferred the requested data of a read command to the command out-box. 0 No data in the command out-box 1 Data in the command out-box



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Field	Bits	Type	Description
<b>PIBX-OF</b>	2	r	<b>Packet In-Box Overflow [M-V-CPE]</b> This bit is set if the host writes more data to the packet in-box as allowed within the FIBXMS register (FREE-PBOX-SPACE[7:0]). The current packet will be discarded. This bit will be cleared if the error condition is acknowledged with the short command wPHIERR. 0 No overflow 1 Overflow
<b>CIBX-OF</b>	1	r	<b>Command In-Box Overflow</b> This bit is set if the host writes more data to the command in-box as stated in the FIBXMS register (FREE-CBOX-SPACE[7:0]). This bit will be cleared if the error condition is acknowledged with the short command wPHIERR. 0 No overflow 1 Overflow
<b>MBX-EMPTY</b>	0	r	<b>Mailbox Empty</b> (only packet and command in-box). This bit is needed for dynamic change of the in-box sizes (packet/command) with the short commands wMAXCBX and wMINCBX because a change of the in-boxes is only allowed if the in-boxes are empty. It is set if the command- and packet boxes are empty. 0 At least one of the in-boxes is not empty 1 Packet and command in-box are empty and thus it is possible to change the mailbox sizes via the short commands wMAXCBX and wMINCBX.

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**SRGPIO (Allocation D)**
**Status Register for GPIO interrupts**
**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0

r

7	6	5	4	3	2	1	0
GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

r

Field	Bits	Type	Description
GPIO7	7	r	<b>Current Status GPIO7</b> See also GCR2 0 Low level on GPIO7. 1 High level on GPIO7.
GPIO6	6	r	<b>Current Status GPIO6</b> See also GCR2 0 Low level on GPIO6. 1 High level on GPIO6.
GPIO5	5	r	<b>Current Status GPIO5</b> See also GCR2 0 Low level on GPIO5. 1 High level on GPIO5.
GPIO4	4	r	<b>Current Status GPIO4</b> See also GCR2 0 Low level on GPIO4. 1 High level on GPIO4.
GPIO3	3	r	<b>Current Status GPIO3</b> See also GCR2 0 Low level on GPIO3. 1 High level on GPIO3.
GPIO2	2	r	<b>Current Status GPIO2</b> See also GCR2 0 Low level on GPIO2. 1 High level on GPIO2.

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Field	Bits	Type	Description
<b>GPIO1</b>	1	r	<b>Current Status GPIO1</b> See also GCR2 0 Low level on GPIO1. 1 High level on GPIO1.
<b>GPIO0</b>	0	r	<b>Current Status GPIO0</b> See also GCR2 0 Low level on GPIO0. 1 High level on GPIO0.

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**7.5.3 Interrupt Status Register**

For detailed description about the interpretation of the Interrupt Status Register see [“Interrupt Handling” on Page 28](#).

**I-SRE1 (Allocation R)**
**Interrupt Status Register for EDSP Interrupts 1 [M-V-CPE]**
**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
DTMFR-DT	DTMFR-PDT	DTMFR-DTC				UTD1-OK	UTD2-OK
r							
7	6	5	4	3	2	1	0
CPT	CIDR-OF	DTMFG-BUF	DTMFG-REQ	DTMFG-ACT/ UTG-ACT	CIS-BUF	CIS-REQ	CIS-ACT
r							

Field	Bits	Type	Description
DTMFR-DT	15	r	<b>DTMF Receiver Key Detect</b> 0 No change. 1 Change.
DTMFR-PDT	14	r	<b>DTMF Receiver Probably Key Detect</b> 0 No change. 1 Change.
DTMFR-DTC	[13:10]	r	<b>DTMF Receiver Key Decode</b> 0000 No change. 1111 Change.
UTD1-OK	9	r	<b>Universal Tone Detection Receive</b> 0 No change. 1 Change.
UTD2-OK	8	r	<b>Universal Tone Detection Transmit</b> 0 No change. 1 Change.
CPT	7	r	<b>Calling Progress Tone</b> 0 No change. 1 Change.
CIDR-OF	6	r	<b>CID Receiver Overflow</b> 0 No change. 1 Change.

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Field	Bits	Type	Description
<b>DTMFG-BUF</b>	5	r	<b>DTMF Generator Buffer</b> 0 No change. 1 Change.
<b>DTMFG-REQ</b>	4	r	<b>DTMF Generator Request</b> 0 No change. 1 Change.
<b>DTMFG-ACT</b>	3	r	<b>DTMF Generator Active</b> 0 No change. 1 Change.  <i>Note: Bit UTG-ACT and DTMFG-ACT are using the same bit position in SRE1 (overlaid).  The DTMF / AT Generator can not be used simultaneously with the universal tone generator.  The host must ensure that a DTMF/AT Generator and an UTG with the same resource number are not active at the same time!</i>
<b>UTG-ACT</b>	3	r	<b>Universal Tone Generator - UTG Active</b> 0 No change. 1 Change..
<b>CIS-BUF</b>	2	r	<b>Caller ID Input Buffer Underflow</b> 0 No change. 1 Change.
<b>CIS-REQ</b>	1	r	<b>Caller ID Request</b> 0 No change. 1 Change.
<b>CIS-ACT</b>	0	r	<b>Caller ID Generator Active</b> 0 No change. 1 Change.

*Note: The bits supported within I-SRE1 and I-SRE2 are dependent on the EDSP firmware variant and version loaded. For details refer to the Firmware Overview EDSP.*

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**I-SRE2 (Allocation R)**
**Interrupt Status Register for EDSP Interrupts 2 [M-V-CPE]**
**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
ATD1-DT	ATD1-NPR		ATD1-AM	ATD2-DT	ATD2-NPR		ATD2-AM
r							
7	6	5	4	3	2	1	0
EPOU-STAT	ETU-OF	PVPU-OF/ FDP-ERR	VPOU-STAT	VPOU-JBL	VPOU-JBH	Res	DEC-CHG/ FDP-REQ
r							

Field	Bits	Type	Description
ATD1-DT	15	r	<b>ATD1 Detect</b> 0 No change. 1 Change.
ATD1-NPR	[14:13]	r	<b>ATD1 Phase Reversals</b> 0 No change. 1 Change.
ATD1-AM	12	r	<b>ATD1 Amplitude Modulation</b> 0 No change. 1 Change.
ATD2-DT	11	r	<b>ATD2 Detect</b> 0 No change. 1 Change.
ATD2-NPR	[10:9]	r	<b>ATD2 Phase Reversals</b> 00 No change. 11 Change.
ATD2-AM	8	r	<b>ATD2 Amplitude Modulation</b> 0 No change. 1 Change.
EPOU-STAT	7	r	<b>Event Play Out Unit Status</b> 0 No change. 1 Change.
ETU-OF	6	r	<b>Event Transmit Unit Overflow</b> 0 No change. 1 Change.

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Field	Bits	Type	Description
<b>PVPU-OF</b>	5	r	<b>Packetized Voice Protocol Unit Overflow</b> 0 No change. 1 Change. <i>Note: Coder Channel Speech Compression and FAX Data Pump can not be active at the same time for one and the same channel. Depending on which module is active for a channel, this bit positions indicates either the status of the Coder Channel Speech Compression (PVPU-OF) or the status of the FAX Data Pump (FDP-ERR)</i>
<b>FDP-ERR</b>	5	r	<b>Fax Data Pump Error</b> 0 No change. 1 Change.
<b>VPOU-STAT</b>	4	r	<b>Voice Play Out Unit Status</b> 0 No change. 1 Change.
<b>VPOU-JBL</b>	3	r	<b>Voice Play Out Unit Jitter Buffer Low</b> 0 No change. 1 Change.
<b>VPOU-JBH</b>	2	r	<b>Voice Play Out Unit Jitter Buffer High</b> 0 No change. 1 Change.
<b>Res</b>	1	r	<b>Reserved</b>
<b>DEC-CHG</b>	0	r	<b>Decoder Change</b> 0 No change. 1 Change. <i>Note: Coder Channel Speech Compression and FAX Data Pump can not be active at the same time for one and the same channel. Depending on which module is active for a channel, this bit positions indicates either the status of the Coder Channel Speech Compression (DEC-CHG) or the status of the FAX Data Pump (FDP-REQ)</i>
<b>FDP-REQ</b>	0	r	<b>FAX Data Pump Data Request</b> 0 No change. 1 Change.

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*Note: The bits supported within I-SRE1 and I-SRE2 are dependent on the EDSP firmware variant and version loaded. For details refer to the Firmware Overview EDSP.*



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**I-SRS1 (Allocation C)**  
**Interrupt Status Register for**  
**Analog-Line-Module Interrupts 1**
**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
AUTO-MET-DONE	RAMP-READY	HOOK	GNDK	GNKP	GNDKH	ICON	VTRLIM
r							
7	6	5	4	3	2	1	0
0	LM-THRES	LM-OK	DU-IO				
r							

Field	Bits	Type	Description
<b>AUTO-MET-DONE</b>	15	r	<b>Auto Metering Done</b> 0 No change. 1 Change.
<b>RAMP-READY</b>	14	r	<b>Ramp Ready</b> 0 No change. 1 Change.
<b>HOOK</b>	13	r	<b>Hook</b> 0 No change. 1 Change.
<b>GNDK</b>	12	r	<b>Ground Key</b> 0 No change. 1 Change.
<b>GNKP</b>	11	r	<b>Ground Key Polarity</b> 0 No change. 1 Change.
<b>GNDKH</b>	10	r	<b>Ground Key High</b> 0 No change. 1 Change.
<b>ICON</b>	9	r	<b>Constant Current Feeding</b> 0 No change. 1 Change.
<b>VTRLIM</b>	8	r	<b>Voltage Threshold Limit</b> 0 No change. 1 Change.

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Field	Bits	Type	Description
<b>LM-THRES</b>	6	r	<b>Level Metering Threshold</b> 0 No change. 1 Change.
<b>LM-OK</b>	5	r	<b>Level Metering OK</b> 0 No change. 1 Change.
<b>DU-IO</b>	[4:0]	r	<b>Data Upstream IO Pins</b> 0 No change. 1 Change.

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**I-SRS2 (Allocation C)**

**Interrupt Status Register for  
Analog-Line-Module Interrupts 2**

**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0

r

7	6	5	4	3	2	1	0
0	0	0	0	OTEMP	CS-FAIL-CRAM	CS-FAIL-DSP	CS-FAIL-DCCTL

r

Field	Bits	Type	Description
<b>OTEMP</b>	3	r	<b>Overtemperature</b> 0 No change. 1 Change.
<b>CS-FAIL-CRAM</b>	2	r	<b>CRAM Checksum Failure</b> 0 No change. 1 Change.
<b>CS-FAIL-DSP</b>	1	r	<b>DSP PRAM Checksum Failure</b> 0 No change. 1 Change.
<b>CS-FAIL-DCCTL</b>	0	r	<b>DCCTL PRAM Checksum Failure</b> 0 No change. 1 Change.

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**I-HWSR1 (Allocation D)**
**Interrupt Hardware Status Register 1**
**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
0	0	0	0	SYNC-FAIL	Res	TXB-CRASH	TXA-CRASH

r

7	6	5	4	3	2	1	0
EDSP-WD-FAIL	0	0	0	MCLK-FAIL	WOKE-UP	0	HW-ERR

r

Field	Bits	Type	Description
SYNC-FAIL	11	r	<b>Synchronization Failure</b> 0 No change. 1 Change.
Res	10		<b>Reserved</b>
TXB-CRASH	9	r	<b>Transmit Highway B Crash</b> 0 No change. 1 Change.
TXA-CRASH	8	r	<b>Transmit Highway A Crash</b> 0 No change. 1 Change.
EDSP-WD-FAIL	7	r	<b>EDSP Watchdog Failure</b> 0 No change. 1 Change.
MCLK-FAIL	3	r	<b>Masterclock Failure</b> 0 No change. 1 Change.
WOKE-UP	2	r	<b>Woke Up</b> 0 No change. 1 Change.
HW-ERR	0	r	<b>Hardware Error</b> 0 No change. 1 Change.

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**I-HWSR2 (Allocation D)**

**Interrupt Hardware Status Register 2 [M-V-CPE]**

**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	<b>DL-RDY</b>

r

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	<b>EDSP-MIPS-OL</b>

r

Field	Bits	Type	Description
<b>DL-RDY</b>	8	r	<b>Download Ready</b> 0 No change. 1 Change.
<b>EDSP-MIPS-OL</b>	0	r	<b>EDSP MIPS Overload</b> 0 No change. 1 Change.

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**I-BXSR1 (Allocation D)**

**Interrupt Mailbox Status Register 1 [M-V-CPE]**

**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	<b>CERR</b>

r

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

r

Field	Bits	Type	Description
<b>CERR</b>	8	r	<b>Command Error</b> 0 No change. 1 Change.

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**I-BXSR2 (Allocation D)**

**Interrupt Mailbox Status Register 2**

**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
r							
7	6	5	4	3	2	1	0
0	0	HOST-ERR	POBX-DATA	COBX-DATA	PIBX-OF	CIBX-OF	MBX-EMPTY
r							

Field	Bits	Type	Description
<b>HOST-ERR</b>	5	r	<b>Host Error</b> 0 No change. 1 Change.
<b>POBX-DATA</b>	4	r	<b>Packet Out-Box Data [M-V-CPE]</b> 0 No change. 1 Change.
<b>COBX-DATA</b>	3	r	<b>Command Out-Box Data</b> 0 No change. 1 Change.
<b>PIBX-OF</b>	2	r	<b>Packet In-Box Overflow [M-V-CPE]</b> 0 No change. 1 Change.
<b>CIBX-OF</b>	1	r	<b>Command In-Box Overflow</b> 0 No change. 1 Change.
<b>MBX-EMPTY</b>	0	r	<b>Mailbox Empty</b> 0 No change. 1 Change.

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**I-SRGPIO (Allocation D)**
**Interrupt Status Register for GPIO interrupts**
**Reset Value: 0000<sub>H</sub>**

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0

r

7	6	5	4	3	2	1	0
GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

r

Field	Bits	Type	Description
GPIO7	7	r	<b>Current Status GPIO7</b> 0 No change. 1 Change.
GPIO6	6	r	<b>Current Status GPIO6</b> 0 No change. 1 Change.
GPIO5	5	r	<b>Current Status GPIO5</b> 0 No change. 1 Change.
GPIO4	4	r	<b>Current Status GPIO4</b> 0 No change. 1 Change.
GPIO3	3	r	<b>Current Status GPIO3</b> 0 No change. 1 Change.
GPIO2	2	r	<b>Current Status GPIO2</b> 0 No change. 1 Change.
GPIO1	1	r	<b>Current Status GPIO1</b> 0 No change. 1 Change.
GPIO0	0	r	<b>Current Status GPIO0</b> 0 No change. 1 Change.

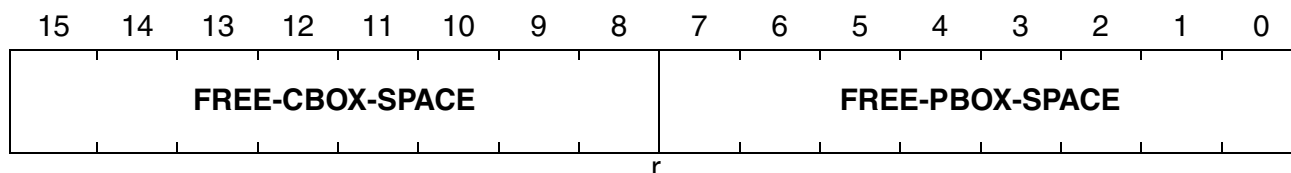


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## 7.5.4 Handshake Registers

### FIBXMS (Allocation D)

#### Free In-Box-Memory Space Register

**Reset Value: 1FFF<sub>H</sub>**


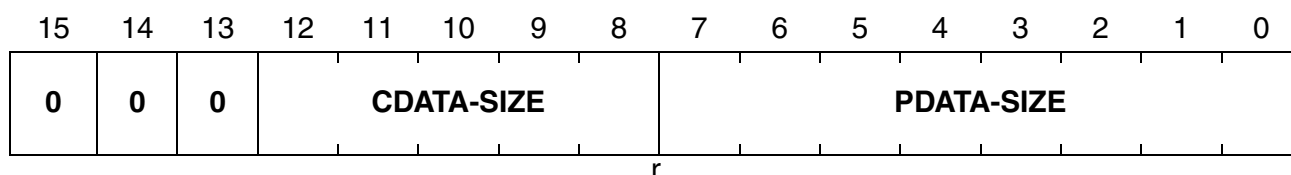
Field	Bits	Type	Description
<b>FREE-CBOX-SPACE</b>	[15:8]	r	<b>Free Command In-Box Space</b> Indicates the free command in-mailbox size in words. The free command mailbox size can be increased/decreased with the short commands wMAXCBX (→ FREE-CBOX-SPACE[7:0] <sub>max</sub> = 255 words) and wMINCBX (→ FREE-CBOX-SPACE[7:0] <sub>max</sub> = 31 words). Default value is 31.
<b>FREE-PBOX-SPACE</b>	[7:0]	r	<b>Free Packet In-Box Space [M-V-CPE]</b> Indicates the free packet in-mailbox size in words. The free packet mailbox size can be increased/decreased with the corresponding short commands wMAXCBX (→ FREE-PBOX-SPACE[7:0] <sub>max</sub> = 31 words) and wMINCBX (→ FREE-PBOX-SPACE[7:0] <sub>max</sub> = 255 words). Default value is 255.

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**OBXML (Allocation D)**

**Packet Out-Box Message Length Register**

**Reset Value: 0000<sub>H</sub>**



Field	Bits	Type	Description
CDATA-SIZE	[12:8]	r	<b>Command Data Size</b> Indicates the number of data words in the command out-mailbox which are ready for reading (0 - 31).
PDATA-SIZE	[7:0]	r	<b>Packet Data Size [M-V-CPE]</b> Indicates the number of data words in the packet out-mailbox which are ready for reading (0 - 255).

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## **Terminology**

### **A**

A/D	Analog to digital
AAL2	ATM Adaptation Layer 2
AC	Alternative Current
ACTH	Active High
ACTL	Active Low
ACTR	Active Ring
ADC	Analog Digital Converter
AGC	Automatic Gain Control
AITDF	Advanced Integrated Test and Diagnosis Functions
ALM	Analog Line Module
ATD	Answering Tone Detector
ATM	Asynchronous Transfer Mode

### **B**

BC	Broadcast
BFM	Bad Frame Manipulation
BN	Background noise

### **C**

CAS	Channel Associated Signaling
CIBX	Command In BoX
CID	Caller IDentification
CMD	CoMmanD
CNG	Comfort Noise Generation
COBX	Command Out BoX
Codec	Coder Decoder
COP	Coefficient Operation
CPE	Customer Premises Equipment
[CPE]	Feature or description only valid for VINETIC®-2CPE.
CPS	Common Part Sublayer
CRAM	Coefficient RAM

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CRC	Cyclic Redundancy Check
CSRC	Contributing Synchronization Source
<b>D</b>	
DAC	Digital Analog Converter
DC	Direct Current
DCCTL	DC- Controller
DIA	Direct Address mode
DIOP	Direct IO Processor command
DIS	Digital Identification Signal
DMA	Direct Memory Access
Downstream	Direction to the customer NT, synonymous to Receive
DRAM	Data RAM
DSP	Digital Signal Processor
DTMF	Dual Tone Multi Frequency
<b>E</b>	
EDSP	Enhanced Digital Signal Processor
EOM	End Of Message (in command address)
EOP	EDSP Operation
ERL	Echo Return Loss
EVT	EVenT (Package)
EXP	Expander
<b>F</b>	
FIR	Finite Impulse Response filter
FPI	Flexible Peripheral Interface bus
FRR	Frequency Response Receive filter
FRX	Frequency Response Transmit filter
FSK	Frequency Shift Keying
<b>G</b>	
GPIO	General Purpose Input / Output
<b>H</b>	
HEC	Header Error Control
HP	High Pass

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HPR	High Pass Receive
HPX	High Pass Transmit
HW	Hardware
<b>I</b>	
I/O	Input/Output
IAD	Integrated Access Device
IOP	Interface Operation
IP	Internet Protocol
ISDN	Integrated Services Digital Network
ITU	International Telecommunication Union
<b>J</b>	
JTAG	Joint Test Action Group
<b>L</b>	
LEC	Line Echo Cancellation
LP	Low Pass
LPF	Low Pass Filter
LPR	Low Pass Receive
LPX	Low Pass Transmit
LSB	Least Significant Bit
LSSGR	Local area transport access Switching System Generic Requirements
<b>M</b>	
μC	Micro Controller
MF	Multi Frequency
MISR	Multiple Input Signature Register
MSB	Most Significant Bit
[M-V]	Feature or description only valid for VINETIC®-4M, VINETIC®-2VIP and VINETIC®-4VIP.
<b>N</b>	
NLP	Non Linear Processing
NT	Network Terminal
NWD	Next Word (in command address)
<b>P</b>	

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PBX	Private Branch eXchange
PCM	Pulse Code Modulation
PDH	Power Down High Impedance
PDRH	Power Down Resistive High
PDRHL	Power Down Resistive High Load
PDRR	Power Down Resistive Ring
PDRRL	Power Down Resistive Ring Load
PDU	Protocol Data Unit
PHI	Programmable Host Interface
PIBX	Packet In BoX
POBX	Packet Out BoX
POTS	Plain Old Telephone Service
PRAM	Program RAM
PTE	Packet Time Encoder
<b>Q</b>	
QoS	Quality of Service
<b>R</b>	
RAM	Random Access Memory
RBS	Robbed Bit Signaling
rBXSr	Read mailBoX Status Register
RDY	Ready
Receive	Direction to the customer NT, synonymous to Downstream
rFIBXMS	Read Free In-BoX-Memory Space register
rISR	Read Interrupt Status Register
rOBXML	Read Out-Box Message Length register
ROM	Read Only Memory
rPOBX	Read Packet Out-BoX
rSRGPIO	Read Status Register GPIO
RTCP	Real-time Transport Control Protocol
RTP	Real-time Transport Protocol
<b>S</b>	
SC	Short Command

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SCI	Serial Control Interface
SID	Silence InDication
SLIC	Subscriber Line Interface Circuit (same for all versions)
SLIC-E/-E2	Subscriber Line Interface Circuit Enhanced Feature Set PEB 4265/PEB 4265-2
SLIC-P	Subscriber Line Interface Circuit Enhanced Power Management PEB 4266
SLIC-S/-S2	Subscriber Line Interface Circuit Standard Feature Set PEB 4264/PEB 4264-2
SOHO	Small Office / Home Office
SOP	Status Operation
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSCS	Service Specific Convergence Sublayer
SSRC	Synchronization Source
SW	Software
<b>T</b>	
TG	Tone Generator
TH	Transhybrid Balancing
Transmit	Direction from the customer NT, synonymous to Upstream
TS	Time Slot
TSLIC-E	Twin Subscriber Line Interface Circuit Enhanced Feature Set PEB 4365
TSLIC-S	Twin Subscriber Line Interface Circuit Standard Feature Set PEB 4364
TTX	Teletax
<b>U</b>	
Upstream	Direction from the customer NT, synonymous to Transmit
UTD	Universal Tone Detection
UUI	User to User Indicator
<b>V</b>	
VAD	Voice Activity Detection
VF	Voice Frequency

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VG	Voice Gateway
VINETIC®	Voice and Internet Enhanced Telephony Interface Concept
VINETIC®-4VIP	Voice and Internet Enhanced Telephony Interface Concept PEB 3324
VINETIC®-2VIP	Voice and Internet Enhanced Telephony Interface Concept PEB 3322
VINETIC®-2CPE	Voice and Internet Enhanced Telephony Interface Concept PEB 3332
VINETIC®-0	Voice and Internet Enhanced Telephony Interface Concept PEB 3320
VINETIC®-4M	Voice and Internet Enhanced Telephony Interface Concept PEB 3314
VINETIC®-4C	Voice and Internet Enhanced Telephony Interface Concept PEB 3394
VINETIC®-4S	Voice and Internet Enhanced Telephony Interface Concept PEB 3304
VINETICOS	Voice and Internet Enhanced Telephony Interface Concept Coefficients Software
VoATM	Voice over ATM
VoDSL	Voice over DSL
VoIP	Voice over IP
VOP	Voice over Packet
[V]	Feature or description only valid for VINETIC®-4VIP
<b>X</b>	
xDSL	(all flavors of) Digital Subscriber Line



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## 8 Appendix

### 8.1 Register Description Format

Every register description contains the following information:

- Register short name
- Register long name
- Register offset address (hex value in brackets above the register)
- Register reset value (hex)
- Bit/bit-field names and their detailed description
- Bit/bit-field access types (r ... read, w ... write, rw ...read/write)

***Attention: Do not write to registers, which are marked as read only, because this can cause unexpected behavior of the VINETIC®-x***

- Allocation: This field gives information about the specific usage of a register. If it corresponds to channels, modules or resources it exists several times and the desired register is “sub”-addressed via the CHAN-bits of first command word:
  - “D” – device (chip) specific register, (one register). For reading/writing the register the CHAN-bits of the first command word has to indicate zero. Valid value: 0.
  - “M” – Analog-Line-Module specific register, (two registers). For reading/writing the register the CHAN-bits of the first command word has to indicate zero, if the first Analog-Line-Module (corresponds to channel 0 and 1) should be addressed and two, if the second Analog-Line-Module (corresponds to channel 2 and 3) should be addressed. Valid values: 0, 2.
  - “C” – channel specific register, (four registers). For reading/writing the register the CHAN-bits of the first command word has to indicate the number of the desired channel. Valid values: 0 - 3.
  - “R” – resource specific register (eight registers). This type of register corresponds to internal and external channels. For reading/writing the register the CHAN-bits of the first command word has to indicate the number of the desired channel. Valid values: 0 - 7<sup>1)</sup>.

<sup>1)</sup> Exception is made by the PCM configuration registries, which allow values 0-15

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**Appendix**

The line is organized as follows (with example):

**EXR (Allocation C)**

**Example Register**

**(003C<sub>H</sub>)**

**Reset Value: 00A1<sub>H</sub>**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABC							Res								
rw															

Field	Bits	Type	Description
ABC	15	rw	<b>Extended Capabilities</b> 0 Does not support 1 Supports
...			
Res	[10:6]	rw	<b>Reserved</b> Returns 0 upon read; must be written with 0.
...			

## 8.2 List of Standards

The following list contains all referenced standards within this document:

**Table 27 List of Standards**

<b>Standard</b>	<b>Description</b>
ITU-T G.164	Echo suppressors
ITU-T G.711	Pulse code modulation (PCM) of voice frequencies
ITU-T G.711, Appendix 1	A high quality low-complexity algorithm for packet loss concealment with G.711
ITU-T G.711, Appendix 2	A comfort noise payload definition for ITU-T G.711 use in packet-based multimedia communication systems
ITU-T G.712	Transmission performance characteristics of pulse code modulation channels
ITU-T G.723	Extensions of Recommendation G.721 adaptive differential pulse code modulation to 24 and 40 kbit/s for digital circuit multiplication equipment application
ITU-T G.723.1	Dual rate speech coder for multimedia communications transmitting at 5.3 and 6.3 kbit/s
ITU-T G.726	40, 32, 24, 16 kbit/s adaptive differential pulse code modulation (ADPCM)
ITU-T G.728	Coding of speech at 16 kbit/s using low-delay code excited linear prediction
ITU-T G.728, Annex 1	Frame or packet loss concealment for the LD-CELP decoder
ITU-T G.729	Coding of speech at 8 kbit/s using conjugate-structure algebraic-code-excited linear-prediction (CS-ACELP)
ITU-T G.729 Annex A	Reduced complexity 8 kbit/s CS-ACELP speech codec
ITU-T G.729 Annex B	A silence compression scheme for G.729 optimized for terminals conforming to Recommendation V.70
ITU-T G.729 Annex E	11.8 kbit/s CS-ACELP speech coding algorithm
ITU-T I.366.2	AAL type 2 service specific convergence sublayer for narrow-band services
ITU-T Q.23	Technical features of push-button telephone sets
ITU-T Q.24	Multi frequency push-button signal reception

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**Appendix**
**Table 27 List of Standards (cont'd)**

<b>Standard</b>	<b>Description</b>
ITU-T Q.552	Transmission characteristics at 2-wire analogue interfaces of digital exchanges
ITU-T V.8	Procedures for starting sessions of data transmission over the public switched telephone network
ITU-T V.23	600/1200-baud modem standardized for use in the general switched telephone network
Bellcore GR-30-CORE	Voice band Data Transmission Interface
British Telecom SIN 227	Calling Line Identification Service: Service Description
British Telecom SIN 242	Calling Line Identification Service: Idle State, Downstream Signalling; Loop State Signalling
Deutsche Telekom BAPT 223 ZV5	Type approval specification for terminal equipment intended for connection to analogue accesses (with exception of emergency telephony and direct dialling-in accesses) in the telephone network / ISDN of Deutsche Bundespost Telekom

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